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Optimization of a low noise amplifier with two technology nodes using an interactive evolutionary approach

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Abstract
Nowadays, wireless communications at frequencies of gigahertz have an increasing demand due to the ever-increasing number of electronic devices that uses this type of communication. However, the design of Radio Frequency (RF) circuits is difficult, time-consuming and based on designer knowledge and experience. This work proposes an interactive evolutionary approach based on genetic algorithm, implemented in the in-house iMTGSPICE optimization tool, to perform the optimization process of a Low-Power Low Noise Amplifier (LNA) dedicated to Wireless Sensor Networks (WSN), which is robust through the corner and Monte Carlo analyses and implemented in two Bulk CMOS technology nodes: 130 nm and 65 nm. Regarding each technology node, we performed two experimental studies to optimize the LNA. The first one used the conventional non-interactive approach of iMTGSPICE, which was not assisted by a designer during the optimization process. The second one used the interactive approach of iMTGSPICE, which was monitored and assisted by a beginner designer during the optimization process. The obtained results demonstrated that the interactive approach of iMTGSPICE performed the optimization process of the robust LNA from 16 to 94% faster than the non-interactive evolutionary approach. The design regarding the technology node of 130 nm took 341 min for the non-interactive and 20 min for the interactive optimization process, whereas the design in the 65 nm took 537 min for the non-interactive and 454 min for the interactive approach.

Keywords Electronic design automation (EDA) · Interactive genetic algorithm · Design of robust analog CMOS ICs · Low noise amplifier (LNA)

1 Introduction

The demand for applications using wireless communication has grown significantly. Recent concepts such as Internet of Things (IoT) and Industry 4.0 are very promising due to the possibility of monitoring and controlling applications without using wire connections. In a wireless communication network, radio frequency (RF) Complementary Metal–Oxide–Semiconductor (CMOS) Integrated Circuits (ICs) are essential elements. As a front-end of wireless transceivers, RF circuits are responsible by processing the analog signal in order to ensure the integrity of information exchanges between electronic devices. Unlike digital CMOS ICs, RF circuits are traditionally designed by hand, based on circuit behavioral equations, followed by an iterative manual process using classical electrical circuit simulators. This process is often very laborious, costly and time-consuming [1], [2], [3]. Besides,

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the optimization processes of CMOS RFICs are performed by manual methods and need much knowledge and experience of the designers to reach the additional metrics required by this kind of ICs. Therefore, the complexity presented by CMOS RFICs complicates its automation task, and, consequently, its design has remained dependent on the expertise of RF designers.

In this scenario, evolutionary computation techniques to solve multi-objective problems in the artificial intelligence area are appropriate and have been successfully used in the optimization processes of analog and CMOS RFICs robust through corner and Monte Carlo analyses[1], [4], [5]- [8]. Despite the recent advances in tools to assist the design of analog and RF ICs, the design of these ICs has depended on the designer's experience. Thus, one of the ways to increase the effectiveness of optimization tools is to integrate the artificial and human intelligences to perform the optimization process. The artificial intelligence area that incorporates interaction between the humans and the computational tool is the interactive evolutionary computation (IEC) [9]. The IEC approach is typically applied when an analytical fitness function is very difficult or impossible to be elaborated, as for example in several areas, such as musical [10], aesthetic [9], ergonomic [11], automotive, graphic art and animation, food engineering [12], among others, in which subjective evaluations are applied. However, this technique have not been explored for the CMOS RFICs optimization. To overcome this complex and challenging issue, this work proposes the use of an in-house electronic design automation (EDA) tool to optimize CMOS RFICs, named iMTGSPICE [13], [14], [15]. It is capable of reducing the optimization cycle times of these circuits due to its heuristic processes of artificial intelligence and IEC techniques. Therefore, designers can optionally interact with the optimization process at any time to stop and change design parameters, such as bias conditions, transistors sizes, specifications to be achieved, etc., and evolutionary process parameters, which are usually the priorities of searching, sigma of the fitness functions, number of iterations, etc., inserting the designers' expertise to reach robustness in desired specifications. It is important to highlight that iMTGSPICE is capable of producing robust solutions of analog and CMOS RFICs in hours. Moreover, it performs the corner and Monte Carlo analyses in the loop of optimization process without reducing the sample space of searching. Interestingly, by the proposed approach, the optimization cycle time is feasible, taking into account all time considered for the optimization of these types of circuits. Therefore, by using iMTGSPICE, the designers are able to meet severe specifications in a reduced optimization cycle time, while guaranteeing the robustness of analog and CMOS RFICs, taking into account the manufacturing process, supply voltage and temperature variations.

In order to demonstrate the proposed computational tool, a classical RF IC is designed: the low-noise amplifier (LNA). The LNA is the first active building-block in a reception chain [16], [17]. It is responsible for amplifying the small RF input signal from the antenna and for assuring a low noise factor for the remaining blocks of the receiver. The main metrics of the ultra-low power LNA for wireless sensor network applications [17], such as power consumption, area, impedance matching, gain and noise figure, are optimized by using the proposed design automation tool (iMTGSPICE). Two experiments are performed for the optimization process of this LNA using the GA. The first one uses the conventional non-interactive approach and the second uses the proposed interactive evolutionary approach, which is compared to the conventional non-interactive approach. These experiments are also performed considering two Bulk CMOS technology nodes: 130 nm and 65 nm. The obtained results are compared in terms of robustness, regarding the manufacturing process, supply voltage and temperature variations, and optimization cycle time.

This paper is organized as follows: Sect. 2 presents the interactive evolutionary approach proposed in this work. Next, in Sect. 3, the LNA topology used in this work is presented. The LNA specifications and configuration parameters of the optimization EDA tool and robustness analyses are provided in Sect. 4. Section 5 discusses the results obtained by the proposed approach. Finally, Sect. 6 concludes this paper.

2 Interactive evolutionary approach of the optimization tool

Fig. 1 illustrates the block diagram of the interactive evolutionary approach with the GA implemented in the optimization tool [13], [14], [15]. It is developed in C + + language and manages the Spice Opus simulator [18]. Moreover, it performs robustness analyses through corner analysis and Monte Carlo analysis in the loop of the optimization process [19].

Designers need to configure the iMTGSPICE before starting the optimization process (Block A) [14], [20]: the description of the circuit (SPICE *netlist*); input variables with their specified ranges, such as the transistors sizes (channel width, W, and channel length, L), bias conditions (voltage and current sources), values of passive components (resistors, capacitors and inductors); the output variables, which are the desired specifications or figures of merit (FoMs) with their respective tolerance ranges, such as the forward gain (S_{21}), input reflection coefficient (S_{11}),

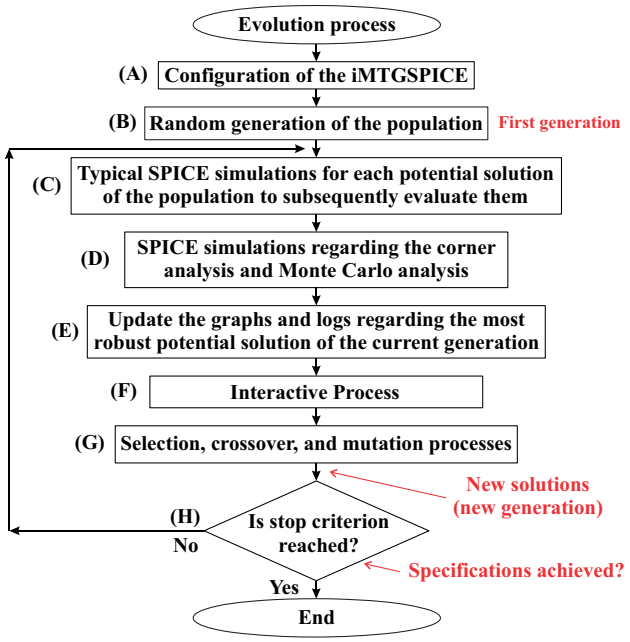

Fig. 1 Block diagram of the interactive evolutionary process implemented in the iMTGSPICE

output reflection coefficient (S_{22}), noise figure (NF), power consumption (P_{TOT}), and total gate area of MOSFETs (A_G); the GA parameters, such as population size (N_P), crossover and mutation rates (P_C and P_M), the weight (priority) applied for each FoM of the fitness function (We_i), where i is an index that represents a FoM, the standard deviation of the Gaussian fitness functions (σ) [20], and N_{Rob} is the desired number of solutions contained in the population that fully meet the design specifications taking into account the robustness analyses, which is used as the stop criterion.

The iMTGSPICE performs the evolution process in two stages [20], [21], which are based on the procedure commonly adopted by the analog CMOS IC designer. The first stage is responsible for evolving functional constraints of the analog IC, such as the direct current (DC) bias conditions of the MOSFETs to ensure that all of them operate in the desired saturation region. The second stage is responsible for making the evolution process of the alternating current (AC) analysis of the analog CMOS IC with the aim of obtaining the final required solutions. It is important to emphasize that the DC stage is performed before the AC stage and they follow the same general block diagram illustrated in Fig. 1. The first stage (DC stage) starts generating randomly a set of potential solutions (Block B), which evolve to obtain one or more solutions, defined by the designer, that meet the functional constraints. The second stage (AC stage) also starts generating randomly a set of N_P potential solutions (defined by the designer) and then one or more of them are replaced by the best solutions found in the first stage of the evolution process.

Next, in Block C, each potential solution is simulated in SPICE [20]. Then, the FoMs (desired specifications) of each potential solution (S_{21}, S_{11}, S_{22}, NF, P_{TOT}, A_G) are obtained and evaluated by minimization, center value, and maximization fitness functions [20] considering a range from 0 to 100 and the value of the fitness function of a potential solution is represented by $Eval_{Sol}$, which is the weighted sum considering the values of the FoMs.

Afterwards, in Block D, the robustness of the best potential solutions evaluated by the fitness functions are calculated, until the evolution process find the N_{Rob} robust potential solutions. The robustness calculation regarding a potential solution is performed as follows:

I- The minimum and maximum performance values of each FoM are obtained through robustness analyses (corner or Monte Carlo). The deviations of the different FoMs found are determined considering their minimum and maximum values relative to the desired specifications;
II- The average value of the deviations found of item I (ε_{sol}) is calculated regarding the worst performance of each FoM, considering their minimum and maximum performance values [19]. Next, the value of the fitness function of each potential solution is calculated considering the value of its ε_{sol}. Afterwards, the population is reordered, giving the highest priority for the most robust potential solutions, which are identified by those that improve more the FoMs (highest ε_{sol} values).

Moreover, the relative deviations are calculated depending on the profile type of the fitness function (central value, minimization, and maximization [20]):

I- "central value": as this specification is defined by the minimum, nominal, maximum values, two deviations are calculated. The first (second) one is calculated considering the maximum (minimum) FoM value subtracted from the nominal desired specification;
II- "maximization": this specification is defined by only one value (value of the desired minimum specification);
III- "minimization": this specification is defined by only one value (value of the desired maximum specification).

In addition, the relative deviation can be positive or negative, when the performance of the FoM is higher or lower in relation to the desired specification, respectively. Therefore, in the case of the "central value" profile of the fitness function, the relative deviation considered for the FoM (worst case) is the one that presents the smallest value between the two relative deviations found.

The FoMs, MOSFETs' sizes, values of bias voltages, and values of the passive components of the most robust potential solution obtained are displayed in the screen of iMTGSPICE (Block E). Fig. 2 presents one of the screens,

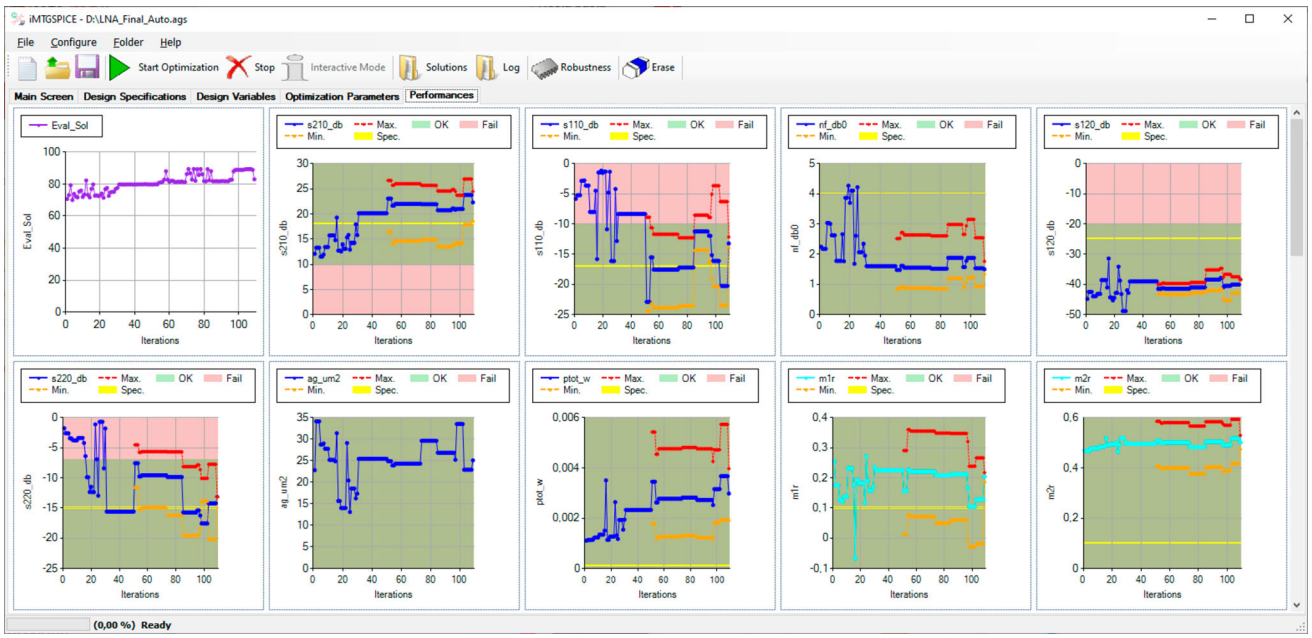

Fig. 2 Screen of iMTGSICE showing the monitoring of the the $Eval_{Sol}$ and FoMs obtained by the best potential solution in each iteration of the optimization process

which monitors the $Eval_{Sol}$ and FoMs found (S_{21}, S_{11}, S_{12}, S_{22}, NF, P_{TOT}), taking into account the corner analysis and Monte Carlo analysis in the loop of the optimization process as a function of the number of iterations (generations).

Next, in Block F, the interactive procedure can be carried out by the designer. Then, based on the real-time monitoring of the design variables and FoMs displayed in the iMTGSPICE screen, optionally, the designer can pause the evolution process and interact with it. The interaction with the system can be performed by changing the dimensions and values ranges regarding the design variables, such as the channel width and length of the MOSFETs, bias conditions of the LNA, passive components (resistors, capacitors and inductors), as well as parameters of the evolution process.

Furthermore, in Block G, genetic operators are applied to generate a new population to be evolved. Each potential solution in iMTGSPICE is represented by a binary chromosome [21]. Each chromosome contains the design variables (transistors dimensions, bias conditions and values of resistors, capacitors and inductors), in which the length of the chromosome is calculated according to the accuracy required for the design variables [21]. The selection process of the best robust potential solutions is performed by the binary tournament. The reason for choosing this method is that it demonstrated to be faster and more effective than other methods, such as the roulette wheel in the experiments performed in this work. Afterwards, the single-point crossover is applied for the selected individuals in population to generate a new set of individuals for the next generation. The use of this type of crossover is due to the best average performance achieved in several experiments considering other types of crossover, such as two points and uniform. Finally, a bit flip mutation is applied for this new generation to further explore the search process of potential solutions [14, 21], which was chosen due to the binary chromosome representation of the GA. The stop criterion is verified in Block H. If the desired number of robust solutions (N_{Rob}) is achieved the optimization process finalizes, otherwise it continues until reaching N_{Rob} or the maximum number of iterations defined by the designer [19].

3 Topology of the LNA

Among the RF receiver building-blocks, the LNA is one of the most critical. In addition to increase the amplitude of the weak incoming signal from the antenna, this circuit needs to operate with severe targets of noise figure and linearity. Focusing in Wireless Sensor Network (WSN) applications, the power consumption of such RF circuit is also a crucial objective. For comparison reasons, the LNA proposed in this work was designed in two different technological nodes: 65 nm and 130 nm CMOS. The LNA topology used is presented in Fig. 3. It is based on an ultra-low power LNA first presented by [17]. Targeting low-power applications, topologies using active load are preferred. So, the proposed circuit presented in Fig. 3 implements a modified self-biased inverter [17]. It is composed

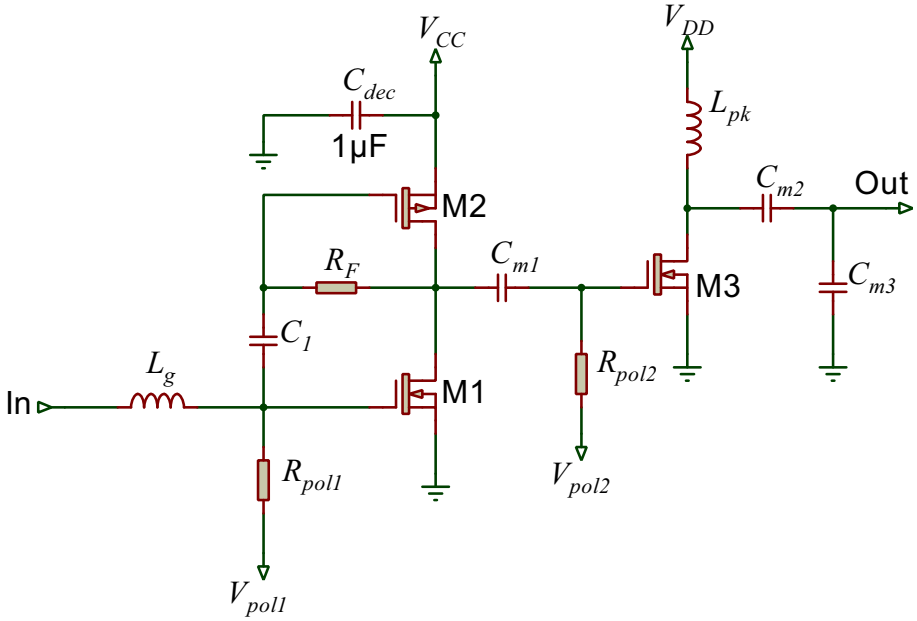

Fig. 3 Topology of the LNA

of two stages: amplification stage and buffering stage. The amplification stage is the LNA core, designed to amplify the input signal linearly using M1 (nMOSFET), M2 (pMOSFET), inductor L_g, capacitor C_1 and resistor R_F. In order to improve gain and reduce noise figure, a biasing voltage V_{pol1} is applied to M1 through resistor R_{pol1}. The buffering stage, composed by M3 (nMOSFET) and the inductor L_{pk}, is used for measurement purposes, in order to comply with 50 Ohms input impedance of test equipment. The required output matching (50 Ohms) is obtained thanks to the capacitive divider of C_{m2} and C_{m3}. On the other hand, C_{m1} contributes to the inter-stage impedance matching, as well as to allow the biasing of transistor M3 through V_{pol2} connected to the resistor R_{pol2}. Two different supply voltages are presented in Fig. 3: V_{CC} and V_{DD}. For the LNA designed in a 65 nm technology, the V_{DD} is reduced to 0.5 V, while the V_{CC} is kept in the nominal voltage of 1 V. The main goal is to reduce the power consumption of the LNA core. However, for the LNA designed in a 130 nm technology, V_{CC} and V_{DD} are connected to the same voltage of 1.2 V. In the next section, based on the proposed LNA topology, an interactive evolutionary approach is applied in order to best define the biasing voltages and devices sizing, according to required specifications.

In addition, the input terminal is represented by *in* node and the output terminal by the *out* node. Finally, the large decoupling capacitor, C_{dec}, ensures AC ground at the source of M2.

4 LNA Specifications and configuration parameters of iMTGSPICE and robustness analyses

In this work, we have considered the required specifications of the LNA according Table 1.

Table 1 presents the seven different figures of merit (specification parameters) considered for the LNA design. Moreover, all MOSFETs (M1, M2 and M3) are set to operate in the saturation region (functional constraints).

Two CMOS Bulk manufacturing technologies are used to design the LNA: the 130 nm technology from the GlobalFoundries [22], which will be referred to as LNA_130, and the 65 nm technology from TSMC [23], which will be identified as LNA_65. The standard supply voltage of both technologies (GlobalFoundries and TSMC) used in this work is 1.2 V. The LNA_130 operates at 2.4 GHz and supply voltages V_{CC} and V_{DD} of 1.2 V. The LNA_65 operates at the same frequency, but different

Table 1 The desired specifications of the LNA

Figures of merit	Specifications
Forward gain ($\|S_{21}\|$)	$\geq$ 15 dB
Input reflection coefficient ($\|S_{11}\|$)	$\leq$ -10 dB
Reverse isolation ($\|S_{12}\|$)	$\leq$ -20 dB
Output reflection coefficient ($\|S_{22}\|$)	Minimize (dB)
Noise figure (NF)	$\leq$ 4 dB
Power consumption (P_{TOT})	$\leq$ 6 mW
Gate area of the MOSFETs (A_G)	$\leq$ 1500 µm^2

supply voltages V_{CC} and V_{DD}, which were fixed in 1 V and 0.5 V, respectively. For the LNA_130 the standard supply voltage of the technology was applied, which enabled the optimization process to achieve the desired specifications. However, for the LNA_65, supply voltages below the maximum allowed by the technology were applied due to power consumption constraints. Additionally, the nominal operating temperature of the LNAs is 27 °C.

Table 2 presents the ranges of values adopted for the design parameters (minimum, maximum, and step size values) for the evolution processes of the LNA_130 and LNA_65. Furthermore, W and L represent the channel width and channel length of the MOSFETs, respectively, and m_1, m_2, m_3 represent the multiplicity of each transistor, that is, the number of parallel transistors regarding each MOSFET (M1, M2 and M3). It is important to mention that no expert knowledge was used to define the ranges of values adopted for the design parameters. The range of values of the parameters in Table 2 are based on the literature [17]. For instance, the minimum value of a given parameter can be adopted smaller than that of the reference and the maximum value can be adopted greater than that of the reference.

Initially, regarding both LNAs, the default values for the weights (We_i) of the fitness function of all FoMs were considered the same to perform the evolution process regarding the DC evolution process (first stage), that is, 50% for P_{TOT} and A_G. Similarly, for the AC evolution process (second stage), we considered the same weights (14.3%) for the FoMs ($|S_{21}|$, $|S_{11}|$, $|S_{12}|$, $|S_{22}|$, NF, P_{TOT}, and A_G). Moreover, the σ parameter of the Gaussian fitness function was set to 0.2 for all profiles considered (minimization and maximization) and the two evolution processes, which is related to a maximum tolerance of 25% for the desired specifications [20].

Table 2 Design parameters of the LNA_130 and LNA_65

Design Parameter	Range	
	LNA_130	LNA_65
W	[0.13, 100, 0.1] µm	[0.6, 6, 0.065] µm
L	[0.13, 50, 0.1] µm	[0.06, 0.24, 0.01] µm
R_F	[100, 20 k, 1] Ω	[1 k, 100 k, 10] Ω
R_{pol1}	[100, 30 k, 1] Ω	[1 k, 100 k, 10] Ω
R_{pol2}	[100, 15 k, 1] Ω	[1 k, 100 k, 10] Ω
L_g	[5, 20, 0.1] nH	[5, 20, 0.1] nH
L_{pk}	[1, 10, 0.1] nH	[1, 10, 0.1] nH
C_{m1}	[0.1, 5, 0.05] pF	[0.1, 5, 0.05] pF
C_{m2}	[0.5, 5, 0.05] pF	[0.5, 5, 0.05] pF
C_{m3}	[0.5, 5, 0.05] pF	[0.5, 5, 0.05] pF
C_1	[5, 20, 0.05] pF	[5, 20, 0.05] pF
V_{pol1}	[0.4, 1.2, 0.05] V	[0.3, 1, 0.05] V
V_{pol2}	[0.4, 1.2, 0.05] V	[0.3, 0.5, 0.05] V
m_1	[1, 1, 1]	[1, 30, 1]
m_2	[1, 1, 1]	[1, 30, 1]
m_3	[1, 1, 1]	[1, 30, 1]

The ranges of the parameters means [minimum value, maximum value, and step size value].

Regarding the LNA_130, the parameters related to the DC and AC evolution processes initially are set as follows: N_P is set to 50, the maximum number of iterations (N_{Iter}) was set to 3,000, however, the number of iterations used in each optimization run is not fixed due to the other applied stop criterion (N_{Rob}) considered in this work, which is set to 2 (number of robust solutions to be found by the optimization process by using the corner analysis and Monte Carlo analysis), regarding the DC and AC evolution processes. For the LNA_65, the initial parameters are set as follows: N_P are set to 50 and 100, regarding the DC and AC evolution processes, respectively; N_{Iter} was set to 10,000 (DC and AC evolution processes); N_{Rob} is set to 1 for the DC and AC evolution processes.

Furthermore, it is important to emphasize that after the DC optimization process is ended, the best DC potential solutions, given by N_{Rob}, are used to compose the initial population that will be used to perform the AC evolution process of the LNA. Consequently, at the end of the AC evolution process, N_{Rob} robust potential solutions are generated, which are obtained from each optimization run. The most robust potential solutions are identified by the highest average deviations regarding all deviations of each FoM in relation the desired specifications, that is, the most robust solution is the one which maximizes the desired specifications. In the iMTGSPICE implementation, P_C is set to 70%, and P_M is set to 3% for both (DC and AC) evolution processes and both LNAs.

It is important to highlight that all the initial values of the iMTGSPICE configuration parameters can be changed by the designer during the iMTGSPICE search process.

In the experiments carried out in this work, the robustness analyses are performed by both, the corner analysis and Monte Carlo analysis. It is important to mention that the corner analyses are performed first, and subsequently, the Monte Carlo analyses are performed only for those potential solutions that met all desired specifications found by the corner analyses. This procedure is performed to avoid waste of time in the Monte Carlo analysis when a certain potential solution is not robust by the corner analysis, considering that the aim of the optimization process is to ensure the design robustness by both analyses simultaneously (corner analysis and Monte Carlo analysis).

During the optimization process, the robustness of the LNA_130 in relation to global process variations is verified by the corner analysis. Regarding the corner analysis, we

have considered the threshold voltages (V_{th}) and mobility of the charge carriers along the channel length (μ_0) of MOSFETs. These parameters are responsible for affecting the main analog parameters of the MOSFETs, such as the transconductance (g_m). The extreme global variations of V_{th} and μ_0 were set to ± 10% and ± 6%, respectively, for the nMOSFETs, and ± 12% and ± 10%, respectively, for the pMOSFETs [24]. Therefore, the extreme operating conditions of the nMOSFETs and pMOSFETs were considered during the corner analysis. In the operating condition named *Fast–Fast* (FF), the nMOSFETs and pMOSFETs operate at the maximal g_m. In the operating condition named *Slow-Slow* (SS), the nMOSFETs and pMOSFETs operate at the minimal g_m. In the operating condition named *Fast-Slow* (FS), the nMOSFETs operate at the maximal g_m and the pMOSFETs at minimal g_m. Finally, in the operating condition named *Slow-Fast* (SF), the nMOSFETs operate at the minimal g_m and the pMOSFETs at maximal g_m. Moreover, the lowest value of the V_{th} and the highest value of μ_0 define the maximal g_m, and the highest value of the V_{th} and the lowest value of μ_0 define the minimal g_m referring to the nMOSFETs and pMOSFETs. Furthermore, variations of the temperature (environmental) are taken into account, i.e. 0 °C and 75 °C, respectively. The Monte Carlo analysis is also performed during the optimization process. It takes into account the local and global variations of manufacturing process parameters, besides environmental conditions. As we considered 50 global variations (N_{GLob} = 50), 50 local variations (N_{Loc} = 50) and two different temperatures (0 °C and 75 °C), each Monte Carlo analysis performs 5000 simulations (N_{GLob}·N_{Loc}·2), according to the procedure described in [20]. Moreover, the desired yield value of the potential solutions by the proposed approach is 100%, as all the Monte Carlo sample results regarding the desired specifications must be inside the tolerance ranges, which are defined by the designer. For the optimization process of the LNA_65, the corner analysis considered the same settings of the LNA_130, however, an additional environmental variation is considered. For this case, the supply voltages (V_{CC} and V_{DD}) are varied in ± 3%. The Monte Carlo analysis performed during the optimization process of the LNA_65 takes into account only the local and global variations of manufacturing process parameters. As we considered 25 global variations (N_{GLob} = 25), 50 local variations (N_{Loc} = 50), each Monte Carlo analysis performs 1250 simulations, according to the procedure described in [24].

5 Results

The iMTGSPICE was run in a 3.4 GHz IBM-PC with 24 GB RAM and Windows 10 (operating system). The optimization processes of the LNA_130 and LNA_65 in this work were performed regarding two different conditions: (1) Automatic optimization processes by using the conventional GA (non-interactive) of iMTGSPICE; (2) Interactive optimization processes by using the iMTGSPICE assisted by a beginner designer during the optimization processes. It is important to mention that, in the case of the interactive approach, the designer's experience in analog integrated circuit design is not important due to the design approach used in the experiment, which limits the designer's intervention to only a few basic optimization parameters, as will be detailed later in this work. Moreover, both experiments were performed to optimize the LNAs, considering a single run (number of times that the iMTGSPICE was run to obtain the results). Therefore, these experiments with the LNAs are just examples of application of the interactive approach using the GA instead of a statistical validation. However, these experiments are still valid by the usage history of the iMTGSPICE tool [13], which demonstrate that although different results are possible, in their average, the interactive approach of iMTGSPICE can reduce significantly the design cycle time.

The optimization processes can be severely affected by the random generation of the initial population (set of solutions) and by the behavior of the selection, crossover and mutation genetic operators, which are driven by the random generator used by the GA. Therefore, in order to perform a fair comparison between the two experiments, the random generator used by the GA in each experiment was started with the same seed, so that the same initial population is used by each experiment, that is, both experiments have the same starting point. This procedure ensures that the differences in the performance of the interactive method in relation to the non-interactive are only due to the effectiveness of the genetic operators (selection, crossover and mutation) which act with the aid of human intelligence in the interactive approach.

Regarding the second experimental condition, as the researcher is not an expert in RF design, he was oriented not to change the design parameters, which are the MOSFETs dimensions (W, L), bias voltages of the LNAs (V_{pol1} and V_{pol2}) and values of passive components (resistors, indictors and capacitors). The interactive process allowed changes in design specifications as long as they comply with the values specified in Table 1. In addition, basic GA parameters, such as the weights of the design specifications (We_i) and the standard deviation of the Gaussian fitness

functions (σ) were also allowed to be changed during the optimization processes.

Table 3 presents the design variables obtained by the non-interactive and interactive approaches for the LNA_130 and LNA_65, respectively. Table 4 presents the desired specifications (Specs.) of the figures of merit (FoMs) and the average values of the FoMs obtained by the non-interactive and interactive approaches for the LNA_130 and LNA_65, respectively.

The threshold values in Table 4, which were defined for the specifications, are required by the application of the LNAs. As the threshold values are the minimum specifications considered for the application, the minimization ($<$) or maximization ($>$) profile set for each specification aims to improve the respective figure of merit whenever possible. Because there are tradeoffs among the several specifications to be met simultaneously, achieve all required specifications is a very difficult task. Therefore, the criterion used to identify that one approach is better than the other is the one which is the able to improve the greatest number of specifications. We can observe in Table 4 that both non-interactive and interactive approaches of the iMTGSPICE used for the design of the LNA_130 and LNA_65 successfully achieved the specifications within the desired tolerance range. Regarding the LNA_130, the interactive approach with a non-expert designer obtained the best results for most FoMs: S_{21}, S_{11}, S_{12}, P_{TOT}, and A_G with differences of 97%, 59%, 14%, 30%, and 11%, respectively. Only for two FoMs, S_{22} and NF, the interactive approach obtained inferior results in relation to the non-interactive, with differences of 86% and 75%, respectively. As a non-specific value was set for S_{22} and the NF value obtained by the interactive approach met the required specification, the designer prioritized the improvement of the other FoMs as the most positive approach. Despite the large relative difference regarding the NF, which is an important FoM for a LNA, the results obtained by both methods, interactive and non-interactive are very good, as they are considerably smaller than the required specification of 4 dB. Furthermore, considering the LNA_65, the interactive approach with a non-expert designer also obtained the best results for most FoMs: S_{21}, S_{11}, S_{22}, NF, and A_G (5%, 72%, 26%, 19%, and 52%). Only for two FoMs, S_{12} and P_{TOT}, the interactive approach obtained worse results than the non-interactive, with differences of 7% and 41%, respectively. As the two aforementioned parameters were met by the interactive method, the designer prioritized the improvement of the largest possible number of FoMs evaluated for the LNA. It is observed that the interactive approach can be used to guide the optimization process in such a way to meet faster the required specifications and in a given direction, prioritizing certain specifications. These results demonstrate the advantage of using the interactive approach to improve the performance of the LNAs.

Table 3 Design variables obtained for the LNA_130 and LNA_65

Design Variables			
LNA_130		LNA_65	
Non-interactive	Interactive	Non-interactive	Interactive
W = 58.8 µm	W = 68.3 µm	W = 4.225 µm	W_1= 3.38 µm
W = 16.5 µm	W = 1.1 µm	W = 5.98 µm	W = 5.98 µm
W = 8.9 µm	W = 6.5 µm	W = 5.785 µm	W = 4.485 µm
L = 4.7 µm	L = 2.2 µm	L = 0.21 µm	L = 0.07 µm
L = 1.4 µm	L = 39.9 µm	L = 0.21 µm	L = 0.08 µm
L = 29.6 µm	L = 48.0 µm	L = 0.06 µm	L = 0.07 µm
R = 19,366 Ω	R = 19,540 Ω	R = 90,690 Ω	R = 81,160 Ω
R = 26,103 Ω	R = 19,939 Ω	R = 63,500 Ω	R = 83,390 Ω
R = 1439 Ω	R = 13,548 Ω	R = 37,410 Ω	R = 93,580 Ω
L = 5.2 nH	L = 5.8 nH	L = 5.4 nH	L = 5.2 nH
L = 8.7 nH	L = 7.6 nH	L = 7.2 nH	L = 8.8 nH
C = 3.7 pF	C = 4.7 pF	C = 3.05 pF	C = 4.1 pF
C = 0.55 pF	C = 0.65 pF	C = 0.7 pF	C = 0.55 pF
C = 4.9 pF	C = 4.7 pF	C = 0.7 pF	C = 1.25 pF
C = 10.9 pF	C = 19.7 pF	C = 13.2 pF	C = 12.95 pF
V = 0.5 V	V = 0.9 V	V = 0.65 V	V = 0.65 V
V = 0.94 V	V = 0.53 V	V = 0.5 V	V = 0.45 V
m = 1	m = 1	m = 20	m = 26
m = 1	m = 1	m = 28	m = 30
m = 1	m = 1	m = 26	m = 30

It is important to note some important results in Table 4 related to the LNA_130. The interactive approach achieved 32.1 dB for the forward gain (S_{21}) of the LNA_130, whereas the non-interactive approach obtained a value of only 16.3 dB, a difference around 16 dB. As the operation frequency of the LNA is 2.4 GHz, the S_{21} parameter is measured in this frequency. As can be seen in Fig. 4 (a), the S_{21} parameter obtained by the interactive approach is better centered in the operation frequency than the non-interactive approach. This is the main reason by the huge difference in this parameter. Despite the remarkable difference, by the beginner approach of the interactive method, no expert knowledge was necessary. During the optimization process, the user observed in real time that this parameter was improving very slowly. Therefore the user increased the weight (priority) of the S_{21} parameter in the iMTGSPICE tool and reduced the weight of other parameters, which achieved more easily the required specifications, for example P_{TOT} and A_G. Other remarkable results are observed in Table 4 regarding both LNAs. The interactive approach improved in more than 10 dB the input reflection coefficient (S_{11}) of the LNA_130 and

Table 4 Average values of the figures of merit obtained for the LNA_130 and LNA_65

FoMs	Specifications	Obtained FoMs			
		LNA_130		LNA_65	
		Non-interactive	Interactive	Non-interactive	Interactive
$\|S_{21}\|$	≥ 15 dB	16.3 dB	32.1 dB	20.6 dB	21.6 dB
$\|S_{11}\|$	≤ -10 dB	− 20.8 dB	− 33.0 dB	− 14.7 dB	− 25.3 dB
$\|S_{12}\|$	≤ -20 dB	− 65.4 dB	− 74.3 dB	− 36.5 dB	− 33.8 dB
$\|S_{22}\|$	Minimize (dB)	− 1.4 dB	− 0.2 dB	− 11.0 dB	− 13.9 dB
NF	≤ 4 dB	1.2 dB	2.1 dB	1.2 dB	1.3 dB
P_{TOT}	≤ 6 mW	62.9 µW	44.2 µW	2.5 mW	3.52 mW
A_G	≤ 1500 µm^2	564.4 µm^2	504.1 µm^2	61.9 µm^2	29.9 µm^2

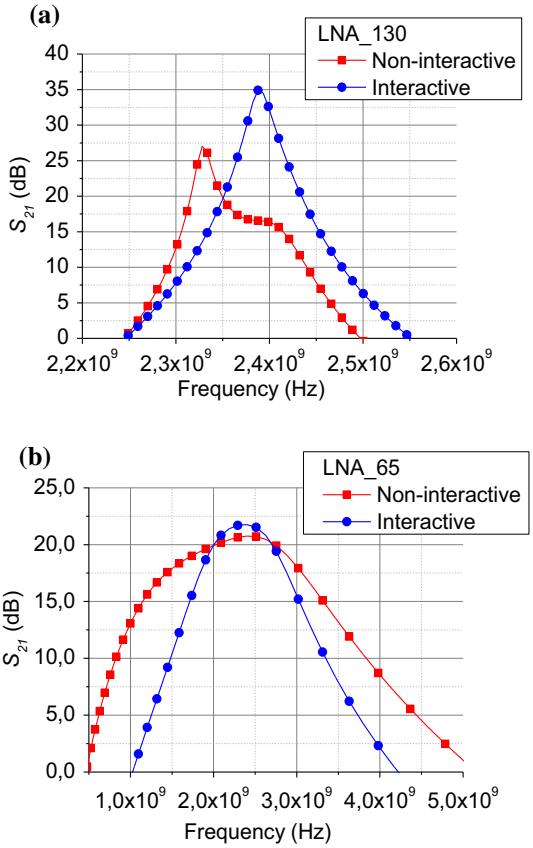

Fig. 4 Forward gain obtained by the non-interactive and interactive approaches for the LNA_130 (**a**) and LNA_65 (**b**)

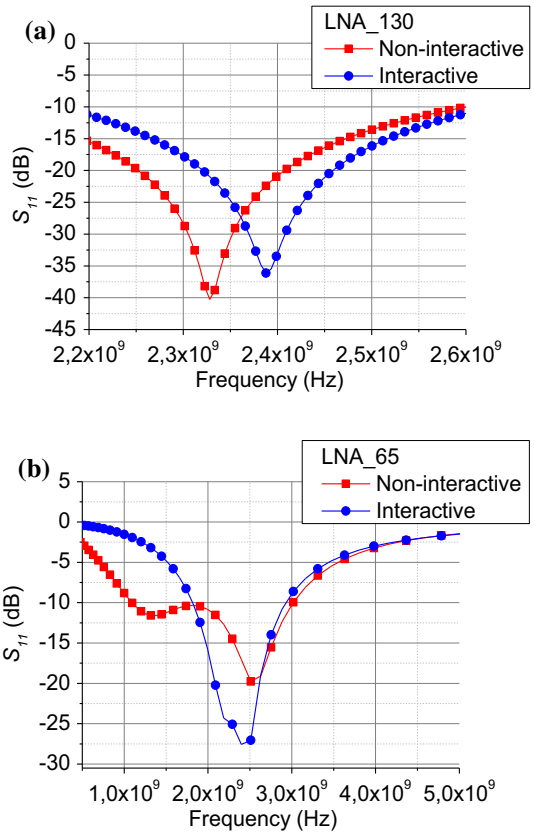

Fig. 5 Input reflection coefficient obtained by the non-interactive and interactive approaches for the LNA_130 (**a**) and LNA_65 (**b**)

LNA_65. For example, the interactive approach obtained the value of − 25.3 dB for the S_{11} parameter of the LNA_65, whereas the non-interactive approach obtained a value of -14.7 dB. Similarly to the previous case, as can be seen in Fig. 5 (a) and Fig. 5 (b), the S_{11} parameter obtained by the interactive approach is better centered in the operation frequency than the non-interactive approach. This is the main reason by the huge difference in this parameter. Again, no expert knowledge was needed to achieve such improvement. During the optimization process, the user observed that the S_{11} parameter, similarly to the parameter S_{21}, was improving very slowly. Therefore the user also increased the weight (priority) of the S_{11} parameter in the iMTGSPICE tool and reduced the weight of other parameters, which achieved more easily the desired specifications. The weight redistribution was carried out a few times, for example, after the user observed the stagnation of the parameters aforementioned by dozens of iterations of the genetic algorithm. Fig. 4 illustrates the forward gain (S_{21}) achieved by solutions obtained by the non-interactive

and interactive approaches for the LNA_130 (a) and LNA_65 (b).

Regarding the LNA_130 in Fig. 4 (a), it is observed that the solution obtained by the interactive approach achieved a higher forward gain than the other one obtained by the non-interactive approach, which is also better centered in the operation frequency of 2.4 GHz. Analyzing the LNA_65 [Fig. 4 (b)], the interactive approach also obtained a higher forward gain in the operation frequency in relation the non-interactive method. Although both solutions of the LNA_65 are accurately tuned in the operation frequency, the solution obtained by the interactive approach better rejects frequencies out of the operation frequency, that is, it is more selective than the solution obtained by the non-interactive method.

The input reflection coefficient (S_{11}) obtained by solutions obtained by the non-interactive and interactive approaches are illustrated in Fig. 5, regarding the LNA_130 (a) and LNA_65 (b).

Regarding the LNA_130 and LNA_65, we can observe in Fig. 5 that the solution obtained by the interactive approach achieved the best profile, that is, in the operation frequency of 2.4 GHz the S_{11} parameter is better minimized and better tuned than in the profile obtained by the non-interactive approach.

Fig. 6 illustrates the noise figure achieved by solutions obtained by the non-interactive and interactive approaches for the LNA_130 (a) and LNA_65 (b).

Analyzing the LNA_130 in Fig. 6 (a), we can observe that the solutions obtained by both approaches achieved similar profiles, although the non-interactive approach obtained a *NF* smaller (better) than the interactive approach in the operation frequency of 2.4 GHz. Regarding the LNA_65 in Fig. 6 (b), it is observed that the solutions obtained by both approaches, interactive and non-interactive, achieved proper profiles for the *NF* curve, that is, at frequencies around 2.4 GHz both approaches obtained similar values for the *NF* parameter, which comply with the required specifications.

It is important to note that, during the optimization process, the user can redistribute weights (priorities) of the specifications, assigning higher weight values for the specifications that are more difficult to achieve. This weight adjustment can be carried out several times during the search process until reaching all specifications at the same time and with robustness in relation to the manufacturing process, supply voltage and temperature variations. In addition, it was observed through Figs. 4 and 5 that this interactive process usually also improves the profile of these curves, since the user guides the optimization process for the design regions that maximize the performance of the specifications, which contributes for achieving the best profile of the curves obtained by the

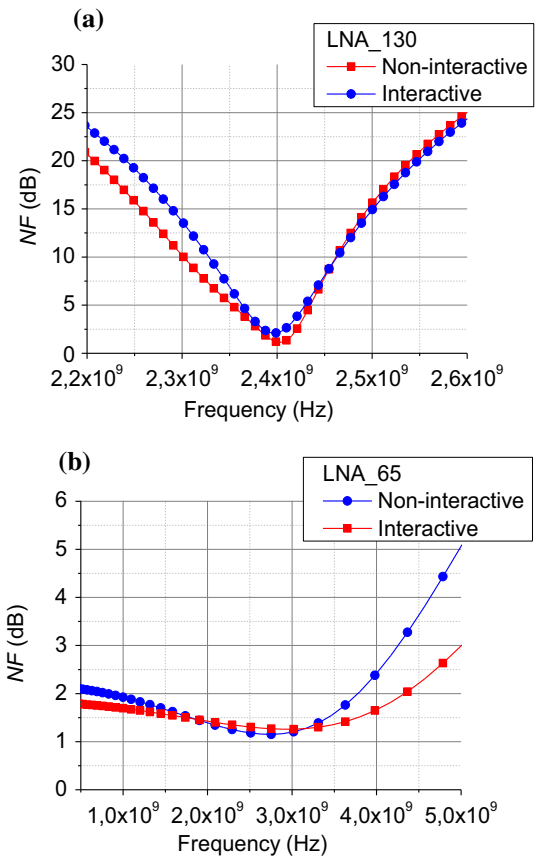

Fig. 6 Noise figure obtained by the non-interactive and interactive approaches for the LNA_130 (**a**) and LNA_65 (**b**)

interactive method in relation to the conventional non-interactive.

Based on the results presented previously, we can conclude that the interactive approach with the GA was capable of significantly improving most FoMs in relation to the conventional non-interactive approach. The superiority of the interactive method is due to the combination of the human and artificial intelligences during the optimization process. A non-expert designer was able to tune the optimization process by changing weight values (priorities) of the design specifications in real time during the optimization process in the iMTGSPICE tool in order to prioritize the optimization of the parameters that have greater difficulty in meeting the required specifications.

5.1 The design optimization cycle times

The optimization cycle times for the design of the LNA_130 are: 341 min. for the non-interactive approach and 19.8 min. for the interactive approach. In addition, the optimization cycle times for the design of the LNA_65 are: 536.5 min. and 453.6 min. for non-interactive and interactive approaches, respectively. Each optimization cycle

time value represent the time necessary to perform the LNA design, encompassing the time required to obtain the best robust solution in relation to the manufacturing process, supply voltage and temperature variations, considering typical and robustness analyses (corner analysis and Monte Carlo analysis). Moreover, for the interactive approach, the optimization cycle times also take into consideration the time spent by the designer.

We observed that the optimization processes regarding the interactive approach of iMTGSPICE are capable of reducing the optimization cycle times of the LNA_130 and LNA_65 designs in relation to the other ones found by using the conventional non-interactive optimization processes with the GA in 94% and 16%, respectively.

It is important to observe that the optimization times of the LNA_65 are higher than those obtained by the LNA_130 because the SPICE simulation models used by the LNA_65 are far more complex than the models used by the LNA_130. The 130 nm technology has 114 parameters (BSIM 3), whereas the 65 nm technology has 1863 parameters (BSIM 4).

Therefore, the interactive optimization process by using the iMTGSPICE might be a useful approach to help not only experts in RF design, but also non specialists in RF design to achieve the desired specifications in a very reduced design cycle time [13], [14], [15].

5.2 The LNA robustness

To perform a detailed robustness analysis regarding the solutions obtained by each approach (automatic optimization with conventional GA and interactive optimization using iMTGSPICE assisted by a non-expert designer), we performed the Monte Carlo analysis for each solution obtained by each approach of each LNA. Afterwards, we have obtained the minimum and maximum values of each FoM of the LNAs, regarding one potential solution obtained by the automatic optimization process with the conventional GA and one potential solution obtained by the non-expert designer by using the interactive optimization process with the iMTGSPICE. Next, the robustness value (ε_{Sol}) of each potential solution was calculated. The criterion used to identify the most robust solution was the one that presented the highest maximization of the desired specifications (highest ε_{Sol}). Table 5 presents the values of the deviations regarding the main FoMs of the LNA_130 and LNA_65 in relation to the desired specifications in Table 1 and the corresponding values of ε_{Sol} regarding each approach considered in this study.

It is important to note that a relative deviation greater than 100% means that the FoM value obtained by the optimization process is more than twice the value of the desired specification considered. Similarly, if a FoM obtained by the optimization process were worse than the specification in Table 1, the relative deviation would result negative.

Analyzing Table 5, regarding the LNA_130 and LNA_65, respectively, we can observe that the interactive optimization processes using the iMTGSPICE assisted by a non-expert designer obtained the values ε_{Sol} 29.9%, and 50.6% higher than those obtained by the non-interactive approach. It means that the interactive approach achieved the highest average deviations regarding the maximization (improvement) of the main FoMs after the Monte Carlo analysis, i.e. they achieved the most robust design solutions.

The higher performance of the proposed interactive evolutionary approach in relation to the non-interactive in terms of optimization cycle time and robustness is due to the consideration of a beginner designer knowledge in the optimization process. These results demonstrate that the interactive approach of the iMTGSPICE is capable of helping not only expert but also non-expert designers of RF circuits to find robust potential solutions [13], [14], [15]. However, it is necessary to emphasize that the user needs to have a basic training about the use of the iMTGSPICE to be aware of how the parameters of the genetic algorithm interfere in the search process and that the design of an analog IC has specifications that are competitive with each other (for example, voltage gain and unit voltage gain frequency), that is, it is not possible to improve all specifications at the same time. Nevertheless, this does not mean that the user of the optimization tool needs to know how the tradeoffs among the specifications work. He can acquire this knowledge by analyzing the optimization

Table 5 The average values of the ε_{Sol} in percentage for each approach and each LNA considered in this work

Method	LNA_130					LNA_65				
	$\lvert S_{21}\rvert$ (%)	$\lvert S_{11}\rvert$ (%)	NF (%)	P_{TOT} (%)	ε_{Sol} (%)	$\lvert S_{21}\rvert$ (%)	$\lvert S_{11}\rvert$ (%)	NF (%)	P_{TOT} (%)	ε_{Sol} (%)
Non-Interactive	2.6	124.9	46.7	98.7	68.2	17.3	17.5	43.5	42.7	30.3
Interactive	59.0	150.2	46.1	99.2	88.6	16.1	104.0	40.4	22.0	45.6

process in real time and in this way he may be able to optimize an analog IC even without being an expert.

6 Conclusion

This paper proposed an interactive approach using the genetic algorithm to optimize CMOS RFICs, which was integrated to the in-house optimization tool named iMTGSPICE. This computational tool includes corner and Monte Carlo analyses in the loop of the optimization processes. Two experiments were carried out aiming the optimization of a LNA optimized in two technology nodes (130 nm and 65 nm) in order to evaluate this innovative evolutionary optimization approach. The first optimization process used the interactive approach of the iMTGSPICE, which was assisted by a beginner designer, who has not specific knowledge in CMOS RFICs designs. The second one was performed by the conventional non-interactive approach with the GA. The experimental results demonstrated that the interactive approach with the GA was capable of remarkably reducing the optimization cycle times of the LNA design, from 16 to 94%, in relation to the conventional GA approach. Moreover, the interactive approach with the GA obtained the most robust potential solutions taking into account the manufacturing process, supply voltage and temperature variations, with improvement in their average robustness values from 30% to 51% in relation to the non-interactive approach with the GA, regarding the values of the deviations of the main FoMs of the LNA in relation to the desired specifications. These results demonstrate that the iMTGSPICE is capable of exploiting expert knowledge to obtain robust potential solutions in a reduced design cycle time.

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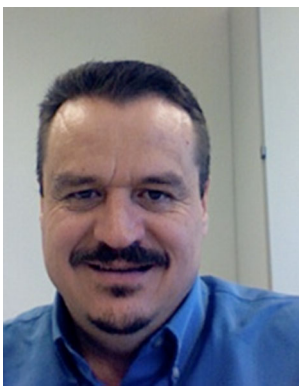

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