



A low-power 10-bit 0.01-to-12-MS/s asynchronous SAR ADC in 65-nm CMOS

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Abstract

During the last decades we have witnessed the performance improvement and the aggressive growth of the complexity of integrated circuits (ICs). The progressive size reduction of transistors in recent technological nodes has allowed and even compelled IC designers to perform analog tasks in the digital domain, increasing the demand for analog-to-digital converters (ADCs). This work presents the design and implementation of a low power, differential, asynchronous successive approximation register analog-to-digital converter (SAR ADC) in a 65-nm CMOS technology. The ADC works in a flexible range of sampling rates, from a few kS/s up to 12.0 MS/s, being suitable for application in a wide spectrum of low power systems and subsystems, such as biosignal recorder interfaces and frontend of wireless receivers. At maximum sampling rate, the post-layout simulated circuit achieved an effective number of bits (ENOB) of 9.65 and a power consumption of 151.4 μ W, leading to a Figure of Merit of 15.8 fJ/Conversion-step; at 10.0 kS/s sampling rate, the ENOB is almost the same, 9.63, but the power consumption is reduced to only 0.26 μ W. The occupied area of the implemented ADC is 0.074 mm².

Keywords Analog-to-digital converter (ADC) · Successive approximation register (SAR) · Low power consumption · Asynchronous SAR ADC

1 Introduction

A trend observed in the last decades in the area of nano-electronics is the continuous replacement of analog functions for digital ones, what has contributed to the current predominance of digital circuits in the implementation of practically all functions found in integrated circuits. The reasons for this replacement are various, among them the

size reduction of transistors, which allows the development of sophisticated digital circuits, the high level of development of CAD tools to support digital designs, not observed with tools for analog designs, the difficult with the re-use of analog circuits, and the smaller benefits that analog circuitries enjoy with the new technological nodes [1, 2].

Despite this trend, there are some typical functions that remain analog. They are those that generate references, like oscillators and voltage reference sources, those functions that handle power voltages, those functions that work with the input/output side of systems, like amplifiers and drivers, and those functions that work with mixed analog/digital circuits interface, like analog-to-digital and digital-to-analog converters (ADC and DAC). ADCs and DACs, more than any other function, hardly can be replaced. Their main performance parameters are resolution, sampling rate, and power consumption, that assume values that vary widely from application to application, giving scope to the development of dozens of different converter topologies.

This work presents the design and implementation of a low power, differential, asynchronous successive

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approximation register analog-to-digital converter (SAR ADC) in a 65-nm CMOS technology, with a flexible sampling rate ranging from a few kS/s up to 12 MS/s. The SAR architecture, which presents few analog blocks (only switches and one comparator) and a simple design, is well suited for moderate resolution and low-to-medium data rate applications [3]. The designed converter is fit for use in a wide spectrum of low power systems and subsystems, such as neural signal recorders and frontend of wireless receivers.

Technologies that enable neurologists and clinicians to observe the simultaneous activity of many neurons have a great demand [4]. A single neuronal signal needs, for its capture, an ADC with no more than 20 kS/s, at least 10 bits, and minimum power consumption in order to not damage the living cells and extend batteries life. In the case of simultaneous neural recording, with multi-electrodes sharing a single ADC, the sampling rate will increase by hundreds of times. The proposed ADC can handle from a single neural signal, with power consumption lower than 1.0 μ W, up to almost 500 diverse neural signals.

At the other side of the spectrum, the development of wireless network standards defining the physical layer of low data rate and very long battery life frontends, like IEEE 802.15.4 and Bluetooth Low Energy (BLE), has triggered the evolution of wireless hardware for applications like the internet of things (IoT). Solutions based on IoT for a wide range of applications, such as transportation, manufacturing, and consumer electronics, have increased over the past few years due to its potential for cost reduction and business processes improvement [5]. Although the demand for software development is predominant in these fields, the hardware must also evolve, otherwise it will become a bottleneck for the IoT systems. The designed ADC can also be employed in the frontend of IEEE 802.15.4 standard receivers, like Zigbee and Thread, working in bandwidths ranging from 200 kHz up to 5.0 MHz.

In this paper, a more comprehensive account of the SAR ADC first presented in [6] is done. In the current design a few improvements were introduced, such as a circuitry that avoids short circuit of the power sources due to switches driving simultaneously, and a circuitry that prevents a metastability event from stopping the ADC operation. In the ADC description, more circuits are shown and explained, and the full ADC operation is detailed. Because of the modifications, all the results were reviewed. Additionally, new results about power consumption of ADC parts and the evaluation of the Conversion Error Rate (CER) are included.

This paper is organized as follow. Section 2 shows the ADC main blocks and their operation. Section 3 presents the ADC layout and what care has been taken with its

design. Simulation results for different conditions are presented and analyzed in Sect. 4. Finally, in Sect. 5, conclusions are drawn.

2 ADC architecture and design

In this work, an asynchronous implementation of the SAR ADC was employed. Typical synchronous implementations [2] make use of two synchronized clock sources, one to control the data sampling (the sampling clock) and other to control the converter iterations (the SAR iteration clock). On the other hand, asynchronous SAR ADCs [7, 8] require only one clock signal to control the sampling. This feature relaxes the clock distribution requirements. Additionally, the designed ADC has a differential architecture to minimize the effects of common-mode noise and to reduce the even order harmonics distortion [2]. A block diagram of the differential asynchronous SAR ADC is presented in Fig. 1.

The ADC is composed by a pair of input switches, implemented using the bootstrapped technique to improve linearity [9], by a capacitive DAC, by a dynamic comparator, by an asynchronous logic, and by output registers. An external sampling clock (*sample_clk*) controls the bootstrapped switches and the asynchronous logic circuit that sets the ADC to either sampling or conversion phase. When the sampling clock is set to low (sampling phase), the bootstrapped switches turn on and the capacitor array of the DAC is charged according to the differential input signal. In this phase, the power consumption of the ADC is very low because there is no digital circuit activity and the analog circuits present low current consumption.

When the sampling clock is set to high (conversion phase), the bootstrapped switches turn off and the SAR procedure is triggered, starting the binary search process which takes N iterations, where N is the resolution of the ADC. In the first iteration, *vdac_p* and *vdac_n* signals

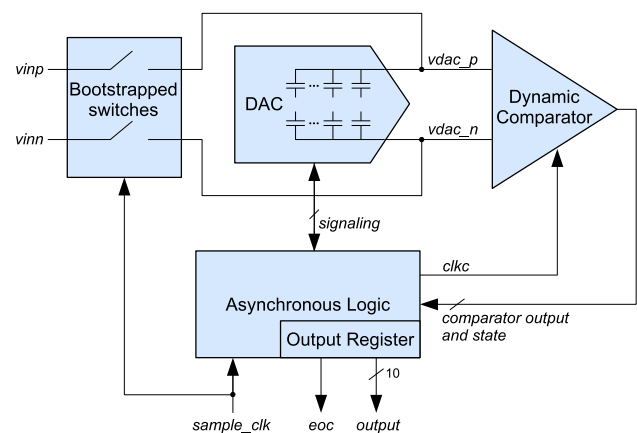


Fig. 1 The asynchronous SAR ADC block diagram

remain constant. From the second iteration on, the $vdac_p$ and $vdac_n$ signals themselves have their values modified by $(N - 1)$ additions/subtractions of $V_{FS}/2^i$, where V_{FS} is the single full-scale voltage (V_{DD}) and i is the iteration number, ranging from 2 up to N .

The timing diagram of the asynchronous SAR ADC is shown in Fig. 2 [10]. In the diagram are pointed out the $sample_clk$, the internal clock with variable frequency that controls the search process iterations (clk_c), and the time intervals at which the signal sampling (t_{track}), the comparator evaluation or regeneration (t_{reg}), the comparator reset, and the DAC charge redistribution (t_{fix}) are performed. In Fig. 3, the behavior of the $sample_clk$, clk_c , $vdac_p$, $vdac_n$, and the end of conversion flag (eoc) are shown with details during the evaluation of the three least significant bits.

For each one of the iterations presented in Fig. 3, the DAC charge redistribution and the comparator reset are first triggered. After a fixed time interval t_{fix} , the clk_c signal falls, indicating that a new differential input is provided for the comparator and that the comparator itself is ready. Next, a comparison (regeneration) is performed in a variable interval t_{reg} and, when the result is ready, a signal is sent to the asynchronous logic circuit, causing the rising of clk_c . At the end of the current iteration, the asynchronous logic commands the storage of the result and the beginning of a new iteration.

The eoc flag indicates that all the SAR iterations were successfully performed, and the conversion result is available at the output registers. The time delay between the beginning of the conversion phase and the rise of the eoc flag is variable and is mostly limited by the sum of the different regeneration times of the N comparisons and the fixed combinational circuits delays. For the iteration in which $|vdac_p - vdac_n| = \Delta V_i$ is the smallest, the regeneration time, $t_{reg,hard}$, can be much higher than the regeneration time of the other iterations. Conveniently, the conversion phase interval is not evenly distributed between the N iterations, but the time is allocated according to the degree of difficulty of the comparison, preventing, as far as possible, the comparator from remaining in metastability.

Most of the ADC current consumption is observed to occur in the interval between the rising of the sampling

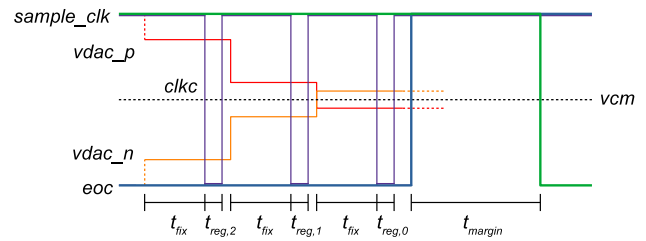


Fig. 3 Internal signal waveforms during the SAR procedure for the three least significant bits

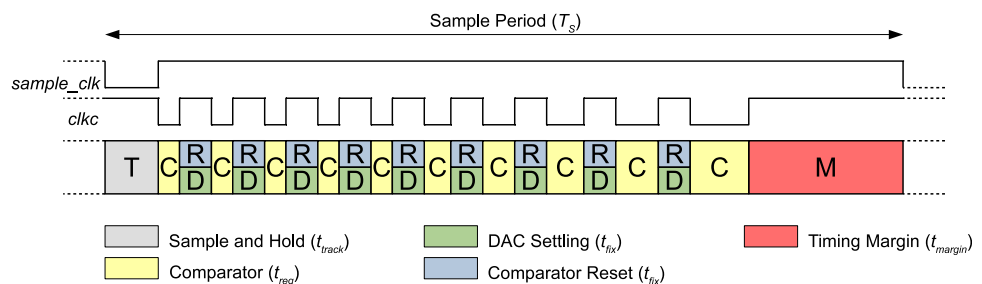
clock signal (triggering of the asynchronous logic circuit) and the rising of the eoc flag. Since the size of this time interval and the amount of operations performed in it do not scale with the sampling frequency, it is expected an almost linear relation between power consumption and sampling frequency [8]. This relation is compromised for very low sampling frequencies, once in this case the ADC power consumption is dominated by the static power consumption.

2.1 The switched capacitor network

The DAC capacitor array of a SAR ADC is also the capacitor responsible for tracking the input voltage during the sampling phase and for holding the charge throughout the conversion phase. Due to charge redistributions, different voltage values are set in the capacitor array, according to a defined switching scheme, and applied to the comparator.

The capacitive DAC structure employed in our design is shown in Fig. 4. A pair of identical capacitor arrays is placed in $vdac_p$ and $vdac_n$ inputs (the p array and the n array). To improve the capacitor matching, capacitors of different sizes within the capacitor arrays are implemented by using multiple unitary capacitors of value C_u . A split binary-weighted capacitive array structure [11] was applied in this design to considerably reduce the required number of unitary capacitors in the DAC. In the structure, M binary-weighted capacitors are placed in the left side of a bridge capacitor and compose the called main DAC, and L binary-weighted capacitors are placed in the right side of the bridge capacitor and compose the sub DAC.

Fig. 2 Timing diagram of an asynchronous SAR ADC



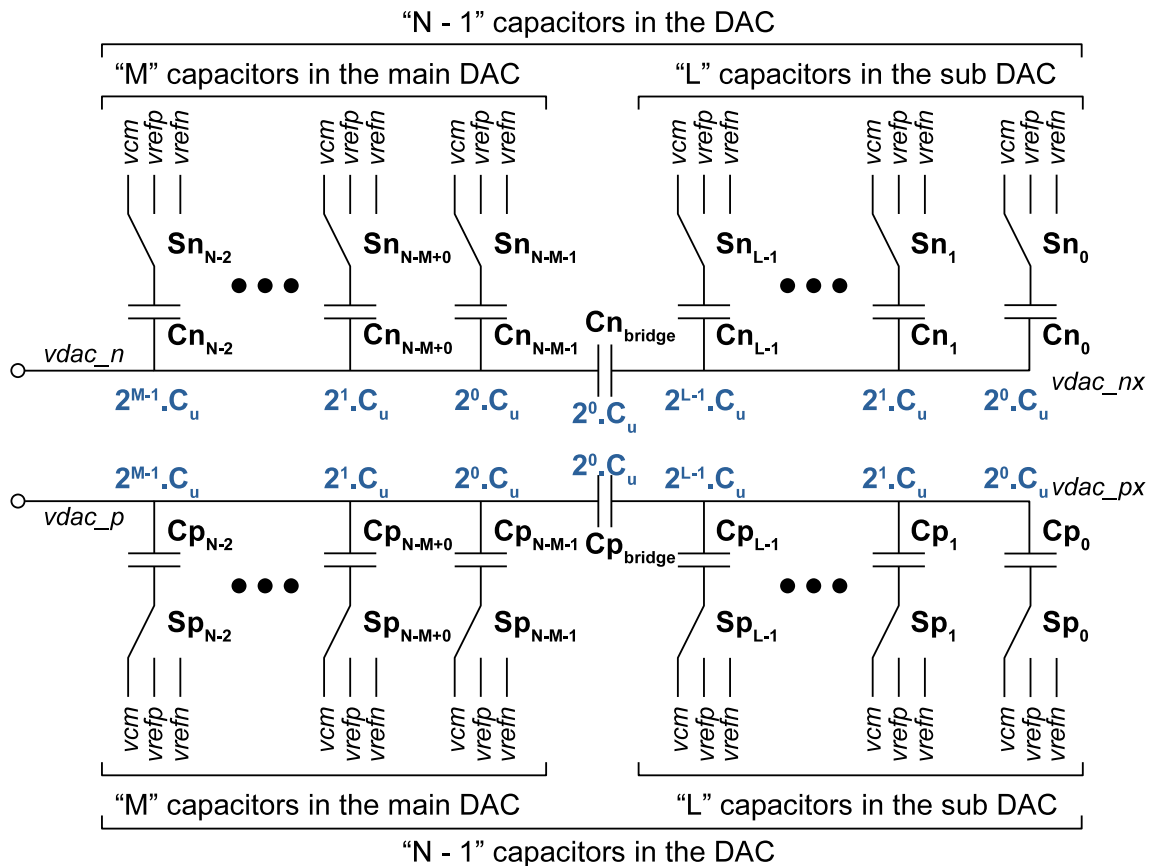


Fig. 4 The capacitive DAC array

To reduce the power consumption, the merged capacitor switching scheme (MCS) was adopted for the search process [12]. It provides good switching efficiency and a low digital circuitry complexity. It presents three-level capacitor array voltage switches (to V_{REFP} , V_{REFN} , and common-mode $V_{CM} = (V_{REFP} + V_{REFN})/2$ voltage levels) in contrast with the conventional two-level capacitor array voltage switch (to V_{REFP} and V_{REFN}).

The switching scheme works as follows: at the sampling phase of the ADC, the bottom plates of all capacitors in the main and the sub DACs are shorted to the common-mode voltage V_{CM} and the top plate of the main DAC capacitors are connected to the differential input signal. During the conversion phase, the DAC is decoupled from the input signal and N iterations are performed. The sequence of steps in the conversion phase is as follow: in the first iteration, $vdac_p$ and $vdac_n$ are compared and the result, pointing out if $vdac_p$ is higher or lower than $vdac_n$, is stored as “0” or “1” in the most significant bit (MSB) of the output register. In the second iteration, if it was found that $vdac_p$ was higher than $vdac_n$ in the previous iteration, Cp_{N-2} and Cn_{N-2} are connected to V_{REFN} and V_{REFP} , respectively, or, if $vdac_p$ was lower than $vdac_n$, to V_{REFP} and V_{REFN} . A new comparison between $vdac_p$ and $vdac_n$

is performed, and the result is stored in second most significant bit of the output register. In the next iterations, the remaining capacitors are successively connected to either V_{REFP} or V_{REFN} according to the comparison result of their previous steps, $vdac_p$ and $vdac_n$ are again compared, and the result is stored. From the first step to the last one, ten comparisons and nine charge redistributions are performed to obtain the ten bits. After the last iteration, $vdac_p$ and $vdac_n$ will be close to V_{CM} .

M and L , the number of switches in the main and in the sub DAC, were set to 5 and 4, respectively, because this choice leads to the minimal number of unitary capacitors needed to implement the arrays, improving the matching and connection routing between these devices.

In typical implementations of the split capacitive array structure, there is an additional unitary capacitor C_f in parallel with the capacitors of the sub DAC. This capacitor C_f has one of its plates permanently connected to V_{CM} , and it is necessary to provide correct binary weighted steps in the switching. In this case, the bridge capacitor (C_{bridge}) should ideally present a capacitance of $(16/15) \cdot C_u$, [11] when $L = 4$. Nonetheless, it is a common practice to use $C_{bridge} = C_u$ for a better layout and matching, and, as a

result, the ADC transfer curve will present several output codes with twice the expected length.

In the implementation of Fig. 4, the capacitor C_f is not present. In this case, the bridge capacitor should present a value close to $(1.0669) \cdot C_u$. When the bridge capacitor is implemented as a unitary capacitor, a common practice as mentioned, a -1.0 LSB (Least Significant Bit) offset and a tolerably small gain error are introduced in the DAC transfer curve [13].

In addition to the errors caused by the bridge capacitor value, parasitic capacitances between nodes $vdac_n$, $vdac_p$, $vdac_{nx}$, and $vdac_{px}$ and V_{DD} or ground will introduce an additional offset and gain errors. If the parasitic capacitances in the nodes $vdac_n/vdac_p$ are C_p and in the nodes $vdac_{nx}/vdac_{px}$ are C_{px} , the offset error is around $(16 \cdot C_p + C_{px})/C_u$ LSB. Note that errors caused by the parasitic in the nodes $vdac_n/vdac_p$ are by far the most important.

Since the offset errors due to the parasitic capacitors are probably higher than 1.0 LSB and the DAC implementation without C_f and with $C_{bridge} = C_u$ causes only offset and small gain errors, but not alteration in the code length of the transfer curve, such implementation was chosen for application in the ADC.

Although the split array structure reduces the number of unitary capacitors, as compared to a conventional binary-weighted capacitive DAC, the minimum value for C_u to meet the mismatch requirements is higher. For a differential array to provide 3-sigma yield, the minimum value for C_u is given by [13]

$$C_u \geq 9(2^M - 1)2^{2(N-M)}K_\sigma^2K_C \tag{1}$$

where K_C is the capacitor density parameter ($C = K_C \cdot Area$) and K_σ is the capacitor matching coefficient ($\sigma(\Delta C/C) = K_\sigma/Area^{1/2}$).

Using Metal–Insulator–Metal (MIM) capacitors for better matching coefficient, Eq. (1) resulted in a minimum C_u of 42 fF, with dimension of $4.4 \mu\text{m} \times 4.4 \mu\text{m}$. This value also meets with the requirement that the thermal noise introduced by the switches must be smaller than the quantization noise of the ideal 10-bit ADC [2]. Figure 5 presents the Differential Nonlinearity (DNL) errors caused only by the DAC capacitor mismatches. The DNL errors mean and standard deviation are zero and 0.098 LSB, respectively. The capacitor mismatches also influence the effective number of bits, ENOB, which will have mean of 9.94 and standard deviation of 0.047. These results show that the performance degradation caused by the chosen C_u value is small.

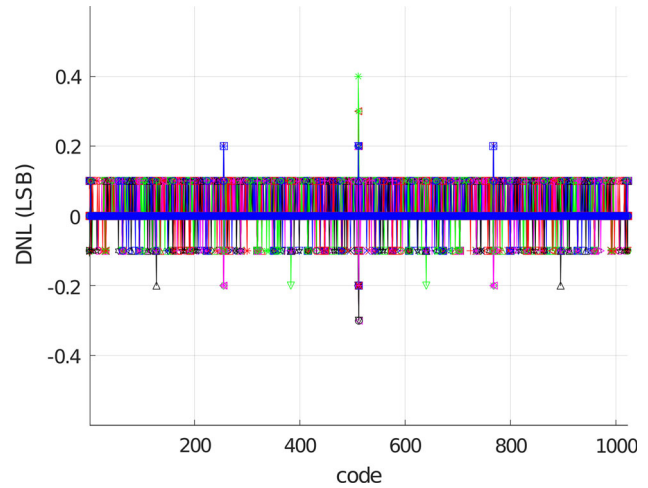


Fig. 5 DNL error caused by DAC capacitors mismatch, obtained through Monte Carlo simulations (DNL precision of 0.1 LSB)

2.2 The bootstrapped switch

A basic sample and hold circuit is composed by a hold capacitor and a switch. In our ADC, the hold capacitor is the capacitor array of the DAC, described and sized in Sect. 2.1, whereas the switch is depicted in this section.

To provide a low distortion differential sampling, bootstrapped switches [9] were considered in the design. These switches keeps the gate to source voltage of an effective switch transistor nearly constant. The schematic of the employed circuit is shown in Fig. 6.

In this circuit, transistors M_1 and M_2 , capacitors C_1 and C_2 and the inverter Inv_1 constitute a voltage doubler necessary to the operations of transistor M_3 , transistors M_3 and M_4 are used in the charge of the capacitor C_3 , transistors M_5 , M_6 , and M_8 and the inverter Inv_2 are responsible for applying a voltage to the gate of transistor M_{11} , and transistor M_{11} is the effective switch transistor. The bootstrapped switch works as follows: when $sample_clk$ is set to high logic level, va is clamped to approximately $2V_{DD}$ and both transistors M_3 and M_4 are turned on, charging the capacitor C_3 to V_{DD} . At the same time, node vg_switch is connected to V_{SS} through transistor M_8 , switching off the effective switch transistor M_{11} (switch off). When $sample_clk$ is set to low logic level, va is clamped to approximately V_{DD} and both M_3 and M_4 are turned off. Now, node vg_switch is connected to the top plate of C_3 through transistor M_5 , node vin is connected to the bottom plate of C_3 through transistor M_6 , and M_{11} is turned on (switch on) with a gate to source voltage of V_{DD} . In this circuit, transistors M_9 and M_{10} are responsible for turning on/off the transistors M_6 and M_5 , respectively, according to the above-mentioned phases. Transistor M_7 is added to alleviate the drain to source voltage experienced by M_8 .

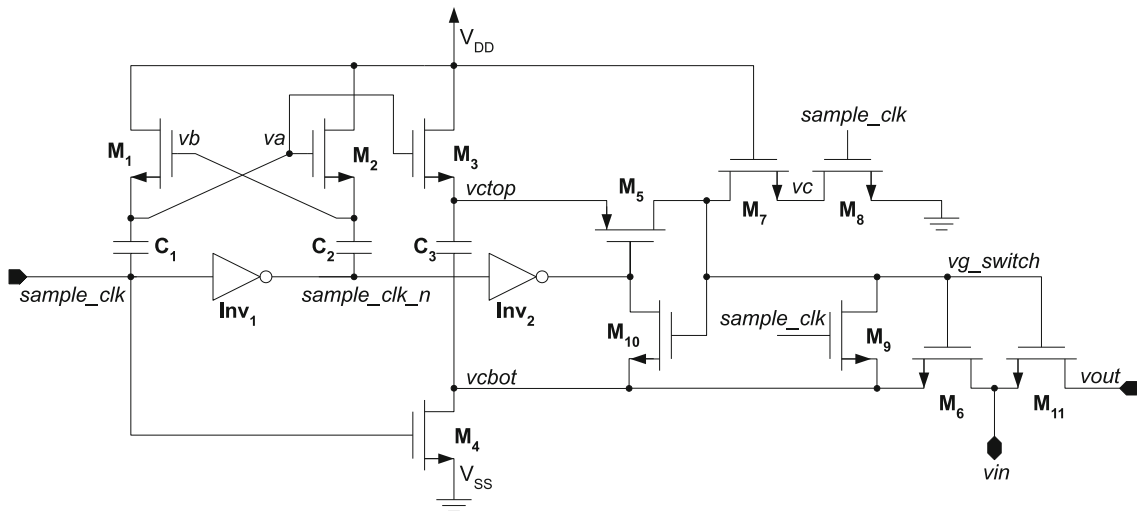


Fig. 6 The bootstrapped switch schematic

Considering transistor M_{11} is implemented with the lowest possible length, the width of M_{11} , W_{11} , must be carefully determined because the charge injection limits its maximum value, and the bandwidth, on the other hand, limits its minimum value.

For a NMOS switch, the charge injection voltage error can be approximated to [14]

$$\Delta V_e = \frac{-kW_N L_N C_{ox}(V_G - V_{TH} - vin)}{C_H} \tag{2}$$

where k is the fraction of the channel charge injected into the capacitor array, C_H is the capacitance value of the array, V_G is the gate voltage at sampling time, and vin is the input voltage at the end of the sampling time.

In the bootstrapped circuit, $(V_G - vin) = V_{DD}$ and, at first analysis, the charge injection would affect $vdac_p$ and $vdac_n$ evenly. In this case, the ADC evaluation would not be affected by the charge injection. Unfortunately, V_{TH} depends on vin , which will result in different charges redistributed to each side of the differential input. The errors due to charge injection should not be greater than $V_{LSB} = V_{FS}/2^N$, and the maximum allowed W_{11} is constrained by

$$|\Delta V_{e1} - \Delta V_{e2}|_{max} = \frac{kW_{11}L_{11}C_{ox}(V_{TH}(V_{DD}) - V_{TH}(0))}{C_H} \leq \frac{V_{FS}}{2^N} \tag{3}$$

where ΔV_{e1} and ΔV_{e2} are the voltage errors of the two switches, and $V_{TH}(V_{DD})$ and $V_{TH}(0)$ are the threshold voltage of transistor M_{11} when $vin = V_{DD}$ and $vin = 0$ V, respectively.

The impact of the sizing of W_{11} in the track bandwidth becomes clear when one considers that the on-resistance of M_{11} and the hold capacitor (DAC) form a low pass RC filter. Therefore, the maximum allowed switch resistance

for charging the DAC capacitors within half the sampling period with a maximum error of V_{LSB} , as analyzed in [13], is constrained by

$$\frac{1}{2^{N+1}} \leq e^{\frac{-0.5T_S}{R_{ON}C_H}} \tag{4}$$

where T_S is the sampling period and R_{ON} is the on-resistance of the switch.

Transistors M_1 - M_4 and both inverter logic gates of the bootstrapped switch were sized after the choosing of C_1 , C_2 and C_3 , because they must deal with the charging/discharging of the capacitors within half T_S . To minimize errors, the capacitors must be relatively larger than the parasitic capacitances added by transistors connected to their terminals. The remaining transistors were sized according to the required strength to drive the gate of other small size transistors within a short time interval.

2.3 The dynamic comparator

The comparator circuit design plays an important role in the system performance. For typical N -bit synchronous SAR ADCs, the N iterations are controlled by the SAR iteration clock, which presents its period N times lower than the sampling clock period. The time budget for the comparator to present a valid response after the start of a comparison, the regeneration time, is usually limited to half period of the SAR iteration clock. The other half period of the iteration clock is applied to reset the comparator and to settle the DAC voltage nodes during the charge redistribution.

An asynchronous converter does not present a SAR iteration clock and the sampling period is usually used half to do the input sampling and half to do the conversion itself. During the conversion, the comparator should

perform N decisions, and the available time is allocated to each comparison by the circuitry according to the greater or lesser difficulty in carrying it out. In consequence, more time can be employed in the harder comparisons. As shown in [10], this feature reduces the data Code Error Rate of the converter, CER, due to the exponential reduction, when compared with its synchronous counterpart of same resolution, in the probability of a metastability event occurring in the conversion of a sample, P_{meta} . For the asynchronous SAR ADC, we have

$$P_{meta} = 2^{N+1} e^{-(T_S - t_{track} - T_{FIX,TOT} - T_{easy})/\tau} \quad (5)$$

where T_S is the sampling clock period, t_{track} is the sampling phase, $T_{FIX,TOT}$ is the sum of all fix delays for DAC settling and comparator reset, T_{easy} is the sum of all regeneration times, excluding the hardest one ($t_{reg,hard}$), and τ is the regeneration time constant of the dynamic comparator.

Note that T_{easy} also depends on the regeneration time constant and its value is approximately

$$T_{easy} \approx \tau \sum_{i \in \{N-1 \text{ softest comparisons}\}} \ln \left(\frac{V_{DD}}{2|\Delta V_i|} \right) \quad (6)$$

where $\Delta V_i = (vin_p - vin_n)$ is the input voltage of the comparator in the i -th iteration.

Once the value of T_S was chosen, the best way to keep P_{meta} and CER low is through the reduction of τ . The dynamic comparator topology of [15] was considered in this work since it presents a low regeneration time constant and, as an additional advantage, a reduced kickback noise. The comparator schematic is shown in Fig. 7. In this circuit the comparator itself is composed by transistors M_1 up to M_{14} . The logic gates at the output stage of the comparator are responsible for delivering the comparison result ($comp_out_n$) and the ready indication flag ($comp_ready_n$) to other circuits.

The comparator works as follows: when $clkc$ node is set to high logic level, the circuit is at reset phase, which turns on the transistors M_{11} and M_{12} and turns off transistors M_7 and M_8 , setting both output voltages, $voutp$ and $voutn$, to V_{DD} . After these nodes reaching V_{DD} , the $ready_n$ signal is set to high, signaling the end of the reset, and is fed back to switches M_3 and M_4 , keeping them on. The $comp_ready_n$ is a copy of $ready_n$, with exception that it is forced to “0” by eoc_n , the inverted version of eoc , when $ready_n$ is locked at “1” due to a metastability event. This action is necessary for a proper resetting of the asynchronous logic, which depends on $comp_ready_n$, before the next conversion. Transistors M_{13} and M_{14} were added to discharge the parasitic capacitors of nodes $ap2$ and $an2$, ensuring they will present the same voltage level before the next comparison.

When $clkc$ node is set to low logic level, the regeneration phase is triggered, meaning that transistors M_{11} , M_{12} , M_{13} and M_{14} are turned off, transistors M_7 and M_8 are turned on, and the output voltages will fall from V_{DD} according to the current drained by the input differential pair M_1 and M_2 , which depends on $(vinp - vinn)$. The cross-coupled transistors M_5/M_6 and M_9/M_{10} further amplify the differential input, increasing the difference among $voutp$ and $voutn$. As soon the differential output voltage presents enough magnitude to trigger the output logic circuits, $ready_n$ and $comp_ready_n$ nodes are set to low, signaling the end of the comparison, and the switches M_3 and M_4 are open, disconnecting M_1 and M_2 differential pair from the rest of the comparator circuit. Once the drain terminals of the differential pair will not sense the voltage swing driven by the cross-coupled pairs, this topology will reduce the M_1 and M_2 gate-drain voltage swing, therefore, reducing noise coupling between $ap2/an2$ and $vinp/vinn$ through the gate-drain capacitances C_{GD} of M_1 and M_2 (kickback noise). Note that M_3 and M_4 are open during the final part of the regeneration phase and most of the reset phase.

The dimensions of the transistors were chosen considering the regeneration time constant and mismatches. At first analysis, the mismatches, and the offset generated by them, is not a critical concern. In fact, the latch offset, when the common-mode voltage is kept constant, is not affected by the input values and, in consequence, is almost time invariant and slightly influence the ADC linearity [16]. Still, an exaggerated offset could decrease the signal-to-noise ratio (SNR) by reducing the input voltage swing [13]. Therefore, the differential pair transistors were enlarged to reduce the mismatch, being their size limited by the kickback noise problem. The remaining transistors, on the other hand, were made as small as possible to reduce their parasitic capacitances, fulfilling the time constraints of the system. The reduction of the NMOS transistors were limited, for this design, by the minimal enclosure space required for the drain and source regions to hold at least 2 diffusion contacts, whereas the width of the PMOS transistors were limited to 4 diffusion contacts, as a compensation for the reduced mobility of their majority carriers. This care was taken to increase the yield. Finally, buffers in the output stage were added to mitigate the coupling from $comp_out_n$ node into $voutp$ and $voutn$ nodes during the regeneration phase. The buffers were provided by the standard cells library.

2.4 The asynchronous logic

The SAR logic circuit is responsible for providing the switching sequence for the DAC circuit. In this work, a custom combinational asynchronous SAR logic, based on

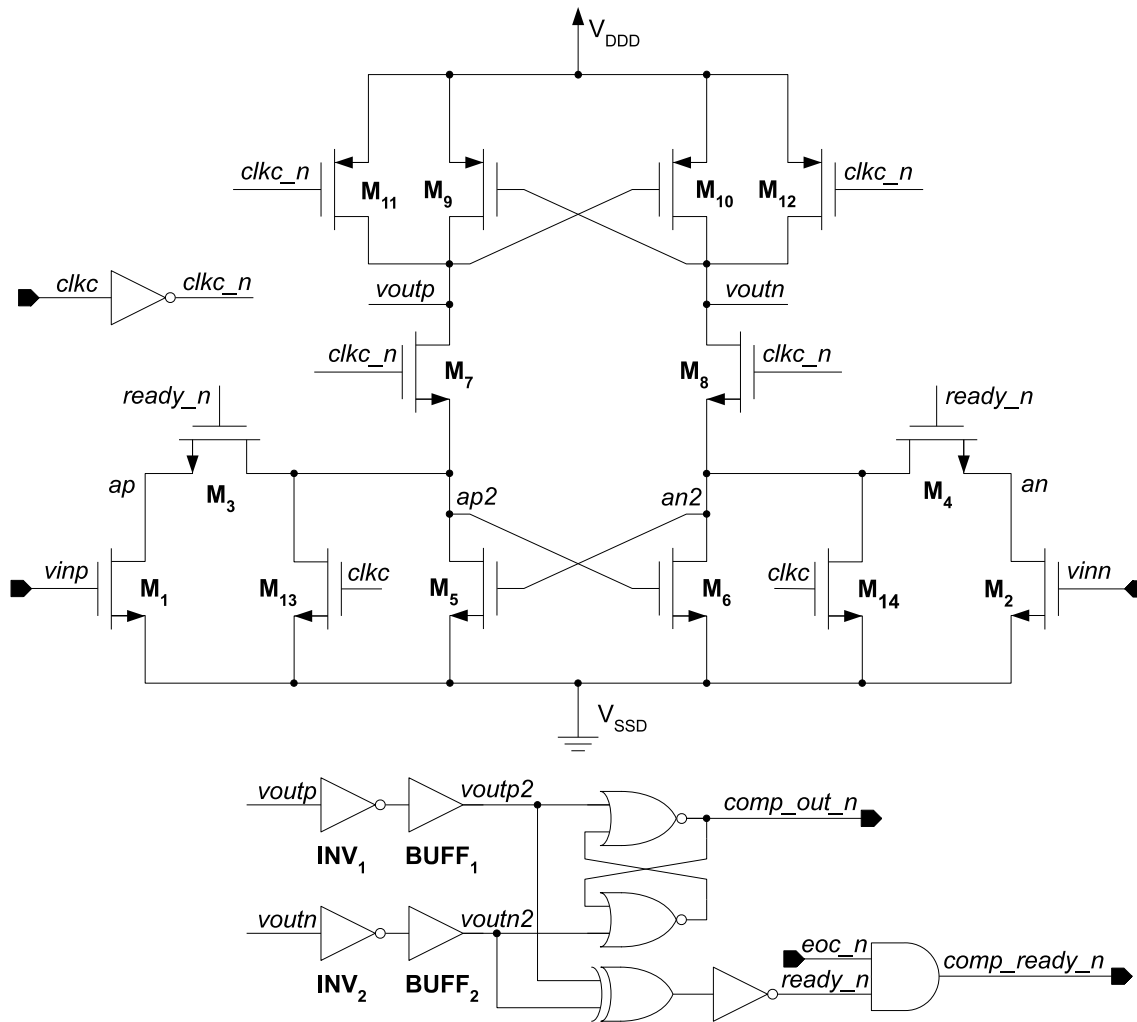


Fig. 7 The comparator schematic

the circuit described in [8], with modifications to support the merged capacitor switching scheme was employed. This asynchronous logic allows a “manual” device placement, presents reduced power consumption and makes use of only one clock source.

Figure 8 presents the SAR logic circuit block diagram, and Figs. 9, 10, and 11 present, respectively, the implementation of the Main Control, the DAC Control and the Comparator Control circuits.

The Main Control circuit has four input signals, coming from the preceding Main Control circuit, from the Comparator, from the DAC Switch, and from the General Control, and two output signals, going to the next Main Control circuit, to the DAC Control, to the next DAC Control, to the DAC Switch, and to the Comparator. At the beginning of the comparison phase, the node states of the Main Control circuit are: $eoc_n = “1”$, $bit_set = “0”$, $comp_ready_n = “1”$, $bit_ready = “0”$, $compare_n = “1”$, and $next_bit_set = “0”$. The Main Control

k is ready for operation when its bit_set is set to high. After that, the bit_ready is also set to high by the DAC Switch k , signaling that the previous DAC charge redistribution was concluded. The Main Control k will then drive the node $compare_n$ to low, and that will start, through the Comparator Control, a new comparison. When the comparison is ready, the $comp_ready_n$ is set to low, causing the change in the value of $next_bit_set$. Now, the $next_bit_set$ has a high level, and it will reset the comparator, through the Comparator Control, will release the DAC Control k circuit to store the comparator result, and will initiate a new DAC charge redistribution and the operation of the Main Control ($k - 1$), through the DAC Switch ($k - 1$).

The DAC Control circuit has six input signals and one output signal. At the beginning of the comparison phase, the node states of this circuit are: $eoc_n = “1”$, $bit_set = “0”$, $comp_ready_n = “1”$, $compare_n = “1”$, $next_bit_set = “0”$, and $bit_n = “1”$. The DAC Control k operation also starts with $bit_set = “1”$, discharging the node

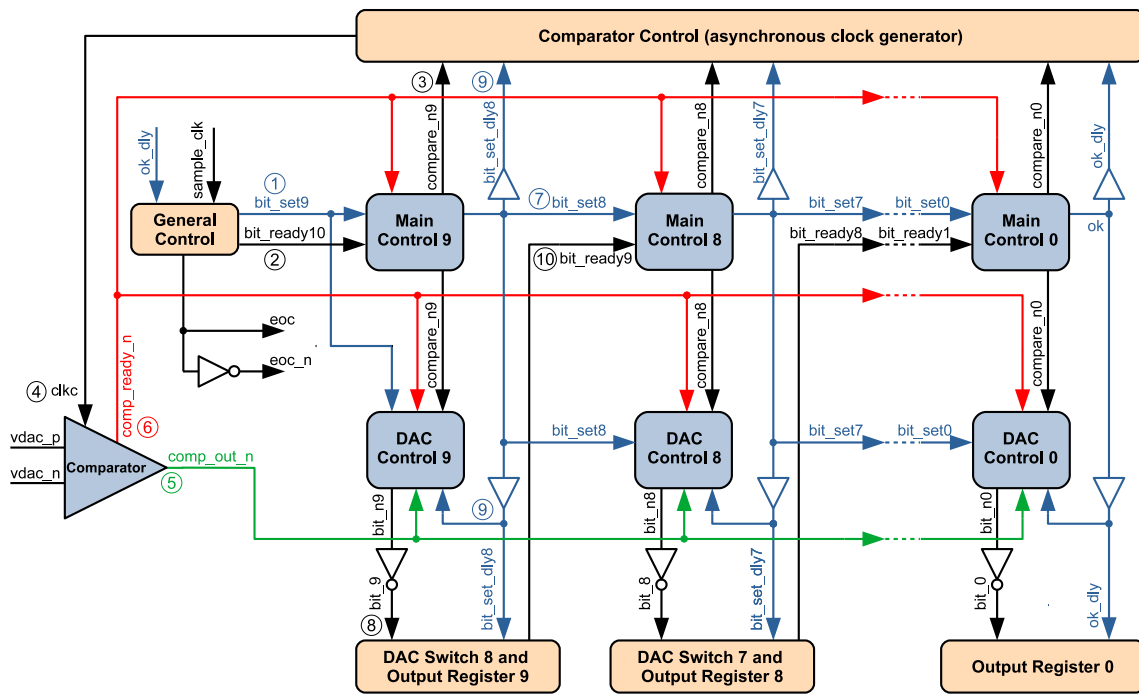


Fig. 8 The SAR logic block diagram (some signals are omitted for simplicity)

Fig. 9 The main control circuit

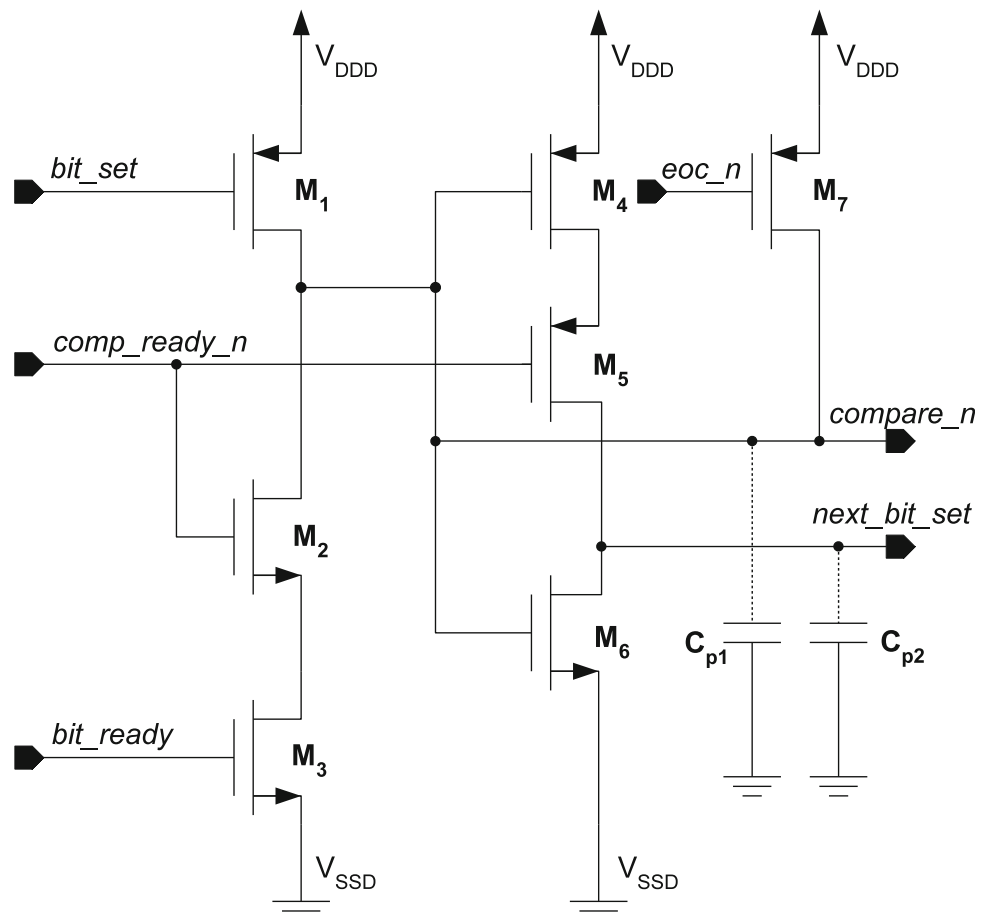


Fig. 10 The DAC control circuit

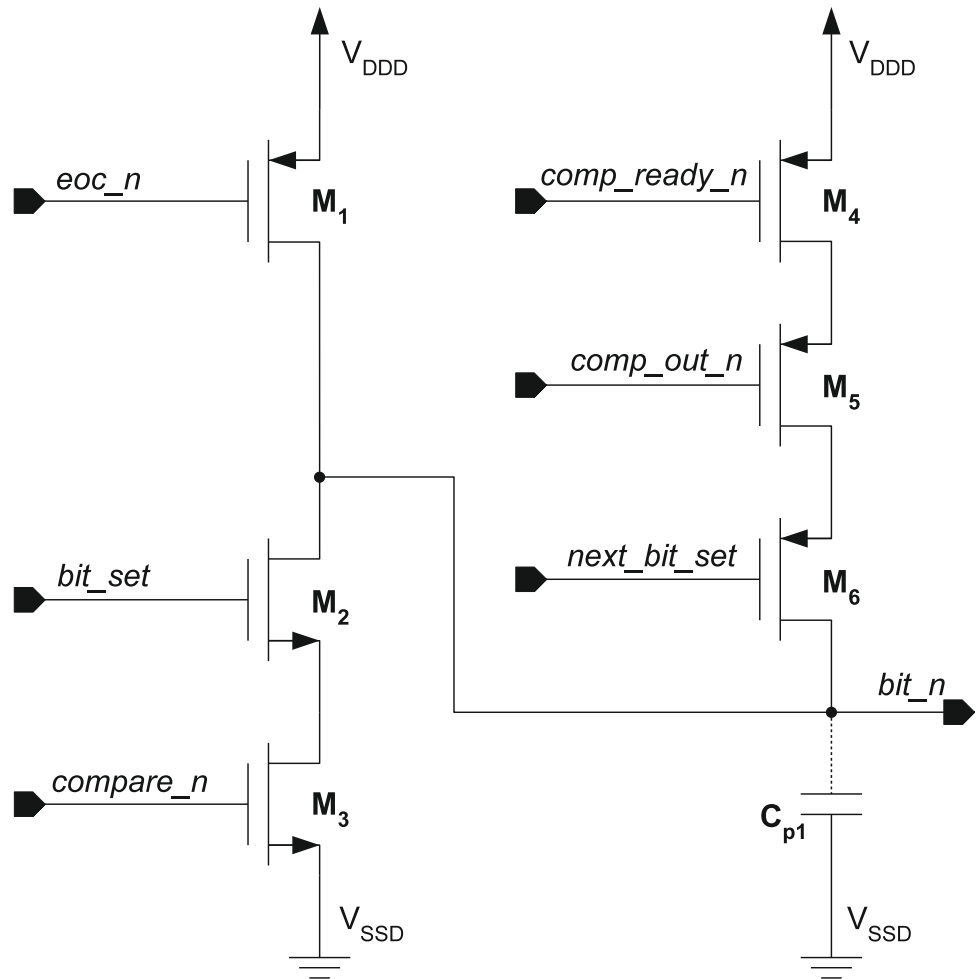
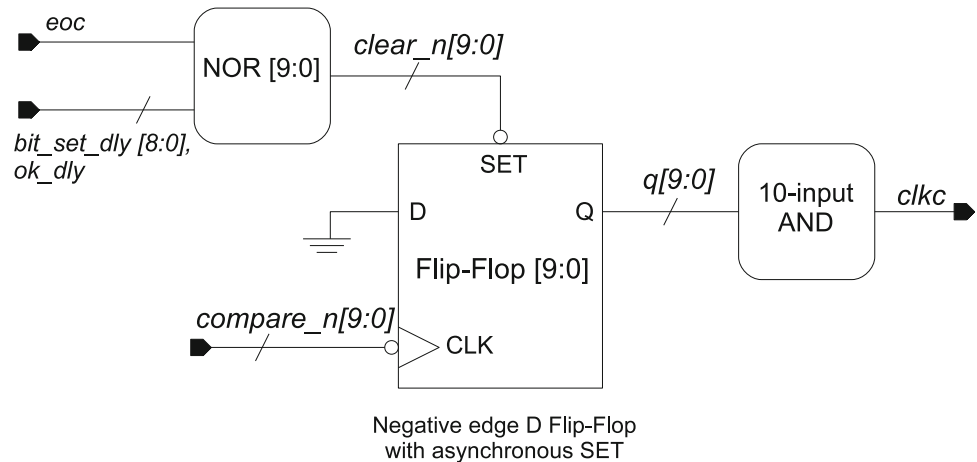


Fig. 11 The comparator control circuit



bit_n . When the $comp_ready_n$ is set to low after the end of a comparison, and while the signal $next_bit_set$ is kept low, the DAC Control will dynamically register the current comparator result in bit_n . This signal is sent to the DAC Switch ($k - 1$) to be used in the switches' selection.

To drive the bottom plate of the capacitors in the DAC array to either V_{REFP} or V_{REFN} , inverters as switches were

applied in the proposal of [8]. In this work, the adoption of the MCS required the use of three-level voltage switches for each bit in the DAC. Therefore, the DAC Switch ($k - 1$) must initially short the bottom plates of the capacitors to V_{CM} and then, according to each comparison result, switch $C_{p_{k-1}}$ and $C_{n_{k-1}}$, respectively, to either V_{REFN} and V_{REFP} or V_{REFP} and V_{REFN} . In Fig. 12, it is illustrated

the implementation of the DAC Switch for each single bit. The DAC Switch has three input signals, *bit*, *bit_set_dly*, and *eoc_n*, and one output signal, *bit_ready*, which is responsible for signaling the asynchronous circuit that the DAC has settled. The DAC switch also generates six internal signals, *s0*, *s0_n*, *s1*, *s1_n*, *s2*, *s2_n*, which control the capacitive array switches. The *bit* input signal of the DAC Switch ($k - 1$) is provided by inverting the *bit_n* output of the DAC Control k circuit. This was accomplished by inverter logic gates, which also provide buffering and protection to the high impedance *bit_n* nodes from the noise coupled in the long interconnections going from the DAC Control to the DAC Switches and Output Registers. At the beginning of the comparison phase, the *bit_set_dly* state is “0” and only the switches connecting to V_{CM} are closed. When the comparison is ready, the Main Control k set the *bit_set_dly* of the DAC switch ($k - 1$) to high, which will open the V_{CM} switches. Now the two NAND gates will prepare the signals controlling the other switches, according to the value of the node *bit*, which came from the DAC Control k . The utilization of the delayed version of *next_bit_set*, *bit_set_dly*, will provide a longer time for the preparation of the node *bit* and ensure that this signal is stable when *s0_n* is set to high. This will avoid glitches in the NAND gates. The signal *bit_ready*, sent to the Main Control ($k - 1$), is set to high after the charge redistribution is completed.

Note that, due to the careful design of the DAC Switch Control logic, the nodes *s0*, *s1*, and *s2* are never set to high

at the same time, avoiding temporary short circuits between V_{CM} and V_{REFN} or V_{REFP} power sources.

The complete SAR logic block works as follow: during the sampling phase of the ADC, the *sample_clk* signal has low logic level and no activity is observed in the circuit. When the *sample_clk* signal has high logic level, the asynchronous circuit is triggered and, from now on, N iterations will take place. In the first iteration, the General Control presets the Main Control 9 (1), *bit_set9* = “1”, and waits for the input signals of the comparator to settle, after the opening of the bootstrapped switches. Once the signals are settled (2), *bit_ready10* = “1”, the Main Control 9 requests a comparison (3) to the Comparator Control, *compare_n9* = “0”, which, in turn, sets the dynamic latch comparator to the regeneration phase (4), *clk* = “0”. When the result is available in the output of the comparator (5), the Main Control 9 and DAC Control 9 blocks are signaled (6) with *comp_ready_n* = “0”. After the comparison, *bit_set8* rises (7) to preset the Main Control 8 and DAC Control 8. Also a delayed and buffered version of *bit_set8*, *bit_set_dly8* (9), is used to lock the DAC Control 9 (*next_bit_set*) after the settling of *bit9*, to reset the Comparator Control and to trigger the DAC Switch 8 and Output Register 9. Now, *bit9* (8) holds the actual 10th bit of the converted signal, which will be used by the Output Register 9 and DAC Switch 8 circuits. This circuit will determine, according to the value of *bit9*, to which reference voltage the bottom plate of the MSB capacitors of the capacitive array should be switched. Finally, after a fixed delay, the *bit_ready9* is set to high (10), and the Main

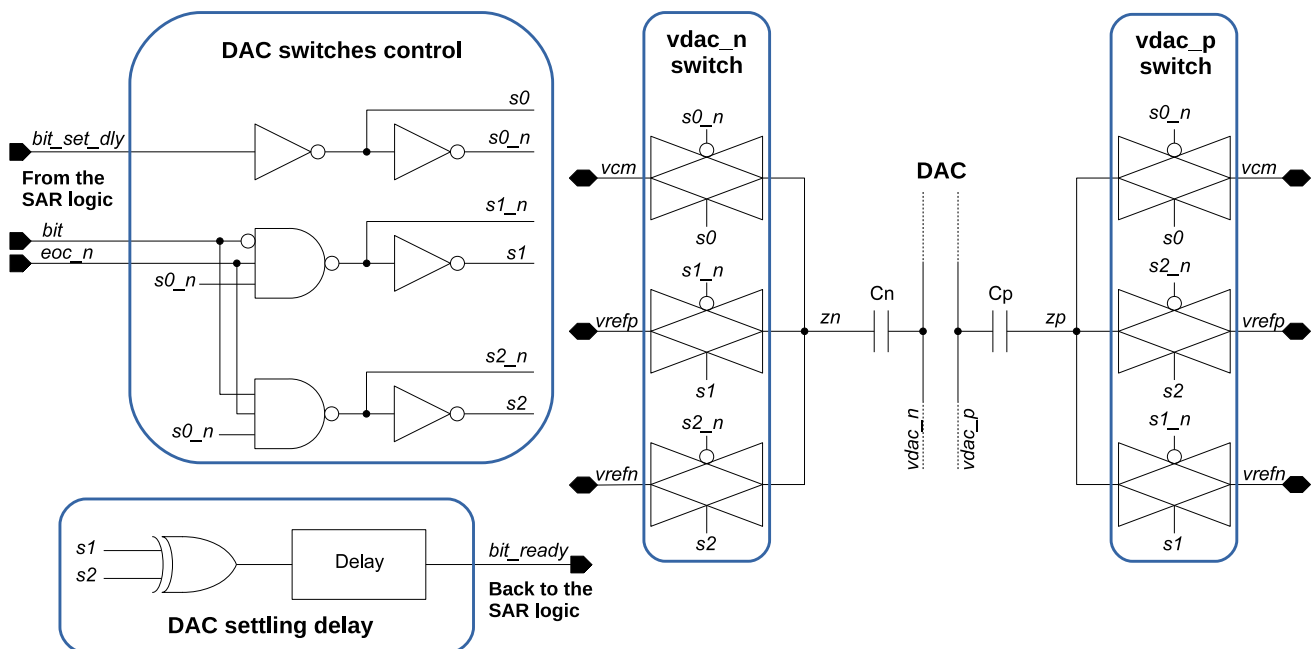


Fig. 12 The DAC switch circuit

Control 8 will initialize the next iteration. The Main Control 8 and the DAC Control 8 will repeat the operations done by the DAC Control 9 and the Main Control 9 and will obtain the 9th bit. The sequence of iterations will continue until all bits are obtained. Once the conversion is completed, the *ok_dly* signal is fed back to the General Control, the *eoc* flag will rise and all the circuits of the SAR logic Block will be reset. It should be mentioned that the *bit_n0* holds the first bit of the converted signal and does not trigger any switching in the DAC.

3 Layout considerations

The layout of mixed-signal integrated circuits usually has its analog circuitry placed as far as possible from its digital circuitry and presents dedicated supply voltages for each domain, to reduce the noise coupled into sensitive areas. The ADC was laid out in a 65-nm CMOS technology following these guidelines and is shown in Fig. 13.

In the layout, the bootstrapped switches and the comparator were placed at the leftmost side of the chip to reduce the routing length of the sensitive wires *vinp*, *vinn*, *vdac_p* and *vdac_n*. The wires *vinp* and *vinn* had their widths increased to provide a low resistance path, reducing

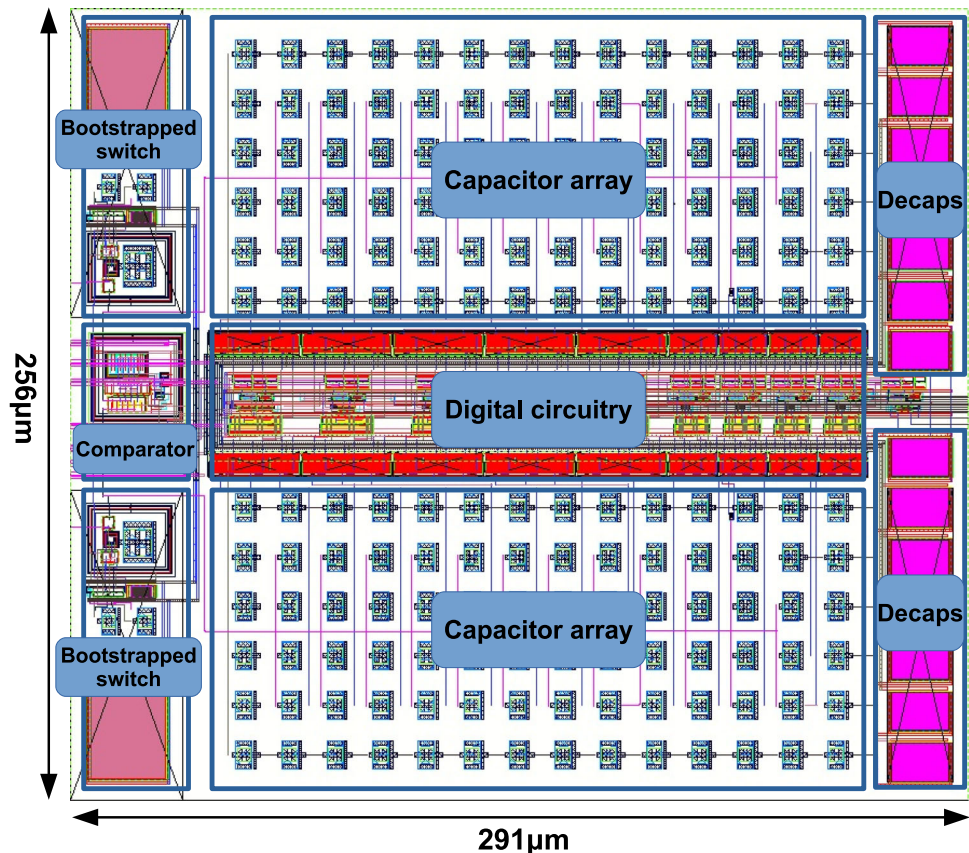
the amount of charge injected into the hold capacitor when the bootstrapped switches are opened. In addition, *vdac_p* and *vdac_n* connections were carefully analyzed and placed to reduce their parasitic capacitances that are the main cause of offset errors. In order to keep the power supply and reference nodes as steady as possible, decoupling capacitors (Decaps) were added to these nodes, at the rightmost side of the chip.

The symmetry in the layout of a differential ADC can affect the system linearity. So, all circuits that appear in pairs, like the bootstrapped switches, capacitive arrays, DAC switches and Decaps, were symmetrically placed along the horizontal axis. Although the comparator presents itself as a single circuit, any asymmetry in its implementation directly affects its offset voltage. So, a meticulous layout drawing of this circuit was performed.

To greatly reduce the congestion due to digital signals routing, the digital circuitry was placed along the horizontal axis in sequential bit order. Following this alignment, a row of DAC switches was placed near each capacitor array, permitting the creation of a pair of reference voltage buses from the Decaps throughout the DAC switches.

Additionally, for each bit, some delay cells were applied to ensure proper delay is placed to the charge

Fig. 13 Layout of the ADC



redistributions of the DAC. For the least significant bits, however, delay cells were not necessary because the delay of the logic circuits is enough to ensure the small amount of charge is properly redistributed before the next comparison.

Finally, to further isolate sensitive circuitries, some transistors were implemented within a *Deep N-Well* guard ring. This careful procedure is applied to the transistors of the bootstrapped switch, except for the transistors related to the voltage doubler circuits, and the transistors of the comparator circuit.

4 Simulation results

The performance of the ADC was verified by running post-layout simulations with Cadence Spectre simulator. To estimate static parameters, such as Differential Nonlinearity and Integral Nonlinearity (INL), the code density analysis is applied [2]. In this work, it was performed by running a transient simulation where the ADC converted 10,240 samples of a differential ramp input signal (v_{inp} increases from zero up to the full-scale voltage, V_{DD} , and v_{inn} decreases from the full-scale voltage down to zero). The resulted code density was analyzed to extract the DNL and INL, which are shown in Fig. 14. For typical corner model and $V_{DD} = 1.2$ V, the worst DNL and INL errors were found to be, respectively, 0.52 LSB and 0.53 LSB. The results of this transient simulation were also used to plot the actual transfer curve of the ADC, in which it was possible to obtain parameters like gain and offset errors. The calculated gain error is 18.1 LSB (less than 1.8% of the full-scale range) whereas the calculated offset error is -11.1 LSB (less than 1.1% of the full-scale range).

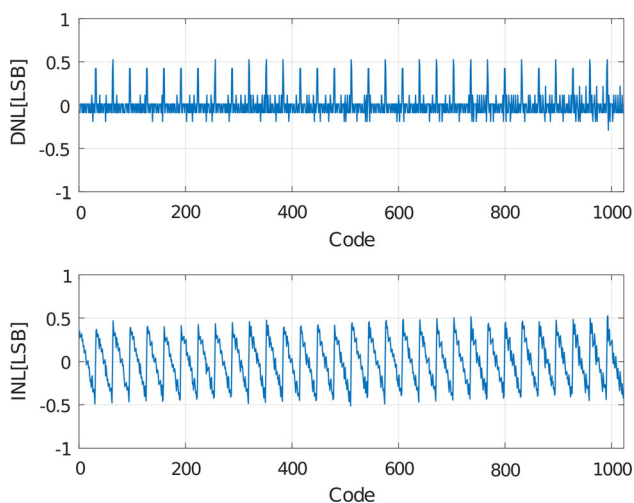


Fig. 14 DNL/INL vs. output code

Parameters like ENOB and power consumption were extracted by running transient simulations, where 1024 samples of a differential sinusoidal input signal are converted and analyzed. For each simulation, the differential input signal frequency is adjusted to be slightly lower than half the sampling frequency (Nyquist criteria), the peak-to-peak voltage to be 90% of input range (to avoid saturation), and the common-mode voltage to be 0.6 V (V_{CM}). The frequency spectrum analysis of the converted codes reveals parameters like signal-to-noise and distortion ratio (SNDR), required for the ENOB calculation [2]. Although the amplitude reduction of the input signal decreases the SNDR, and consequently the ENOB, this effect is compensated by applying a correction factor [17] in the ENOB to properly estimate its value. By using the abovementioned setup, a set of simulations with different sampling frequencies was run to observe the range in which the system keeps a satisfactory performance. For each simulation, a precise frequency for the input signal was calculated for coherent sampling. For typical corner model and $V_{DD} = 1.2$ V, the obtained results are shown in Table 1. The table shows that the ADC can operate with sampling rate ranging from 10 kS/s up to 12 MS/s with practically constant ENOB and reduced power consumption, confirming that the ADC is suitable for a wide spectrum of low power applications.

As expected, the simulated power consumption of the circuit presented an almost linear dependency of the sampling frequency. By drawing the Fig. 15, the coefficient “Power/Sampling frequency” is observed to be roughly constant for sampling rates ranging from 0.1 up to 12.0 MS/s.

Figure 16 shows the current consumption from the several power sources applied in the ADC. The power sources are: the digital power supply (v_{ddd}), the analog power supply (v_{dda}), the positive reference power supply (v_{refp}), the common-mode power supply (v_{cm}) and the input power sources (v_{inp} and v_{inn}). The biggest contributions to the power consumption are given by the digital circuitry (current sinking from v_{ddd}) and by the capacitive DAC (current sinking from v_{refp}). Some of the digital circuitry was implemented with cells from the foundry standard digital library, which means that better power consumption could be achieved if only custom cells were employed. Additionally, the applied merged capacitor switching scheme [12] reduced the current sink from v_{refp} and kept low the power consumption wasted with the DAC charge distribution.

The method used for estimation of the P_{meta} and the CER due to the metastability was based on [18]. By running a set of transient simulations of the comparator, each with different constant input voltages $\Delta V_{i,k} = v_{inp_k} - v_{inn_k}$, the τ parameter can be extracted by looking at the different

Table 1 Performance of the SAR ADC for different sampling frequencies

Sampling frequency [MS/s]	Input frequency	ENOB [bit]	SNDR [dB]	Power [μ W]	FoM ₁ * [fJ/Conv. step]
0.01	4.970 kHz	9.63	59.7	0.26	32.8
0.02	9.941 kHz	9.63	59.7	0.38	24.4
0.1	49.707 kHz	9.62	59.6	1.39	17.8
0.4	198.828 kHz	9.65	59.8	5.17	16.2
2	994.140 kHz	9.65	59.8	25.3	15.9
2.4	1.192 MHz	9.59	59.5	30.4	16.5
4	1.988 MHz	9.63	59.7	50.5	16.0
6.0	2.982 MHz	9.61	59.5	75.7	16.3
10.0	4.970 MHz	9.61	59.6	126.1	16.2
12.0	5.964 MHz	9.65	59.8	151.4	15.8

*FoM₁ = Power/(f_{sample}·2^{ENOB})

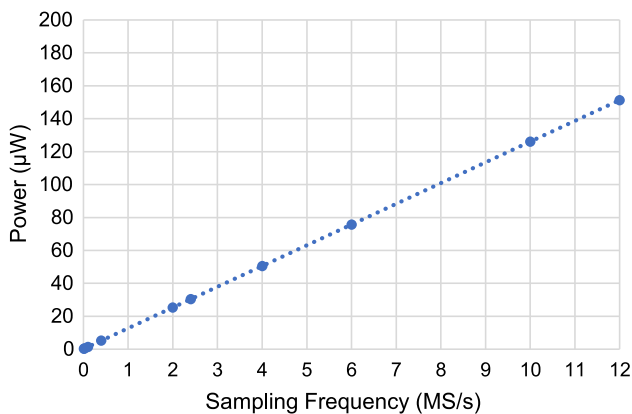


Fig. 15 Simulated average power consumption vs. sampling frequency

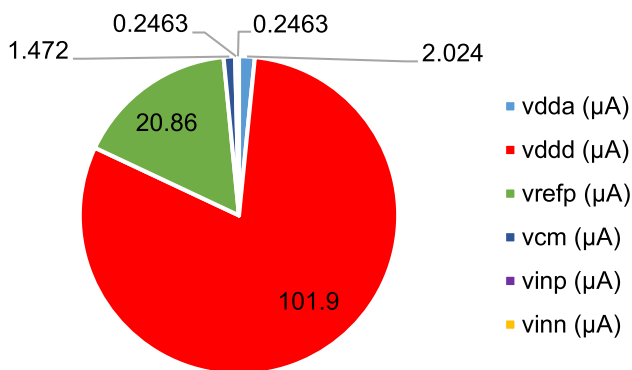


Fig. 16 ADC average current consumption @12MS/s

regeneration times of the comparator for each case. If the set of input voltages are arranged in a geometric progression with a common ratio of 1/10, we have $\Delta V_{i,k} = \Delta V_{i,k-1}/10$ and Eq. (6) can be used to calculate

$$\tau \approx \frac{t_{p,k} - t_{p,k-1}}{\ln 10} \tag{7}$$

where $t_{p,k}$ and $t_{p,k-1}$ are the regeneration time for the input $\Delta V_{i,k}$ e $\Delta V_{i,k-1}$, respectively.

For typical corner model and $V_{DD} = 1.2$ V, post-layout simulations of the comparator show that $\tau = 29$ ps and the simulations of the ADC at 12.0 MS/s show that $t_{margin} = (T_S - t_{track} - T_{FIX,TOT} - T_{easy})$ are close to 17.4 ns. With these parameters, we find that P_{meta} has an extremely small value, on the order of 10^{-258} error/sample, leading to an irrelevant CER.

The simulations for extraction of DNL/INL, ENOB and CER were repeated considering process (Typical, Fast-Fast and Slow-Slow), supply voltage (1.08 V, 1.2 V, and 1.32 V), and temperature (0 °C, 27 °C, and 85 °C) variations (PVT) to evaluate the behavior of the circuit under these different circumstances. In the worst cases of PVT variations, at 12.0 MS/s, the circuit presented a 9.44 ENOB (@FF, 1.32 V, 0 °C), a power consumption of 228 μ W (@FF, 1.32 V, 85 °C) and a CER of $4.95 \cdot 10^{-9}$ (@SS, 1.08 V, 85 °C).

The CER presented itself as the most sensitive parameter because the exponent of Eq. (5), $-t_{margin}/\tau$, varies significantly for different PVT conditions. In Table 2 it is shown the typical and the slow-slow, (SS), 85 °C results for different supply voltage conditions. Notice that the exponent can change from -601 , in the typical case, to -26.7 , the highest valor obtained among all tested conditions. This wide variation in the exponent will cause, in turn, a huge variation in the CER value, which goes from 10^{-258} to 10^{-9} . Even so, the obtained CERs are compatible with the necessary Bit Error Rate (BER) reported in the literature for low power Zigbee and BLE frontends [19, 20], ranging from 10^{-6} up to 10^{-3} . For more strict applications, the CER of the ADC can be greatly reduced by limiting the supply voltage to $V_{DD} \pm 5\%$. In such circumstance, the worst PVT condition is (@SS, 1.14 V, 85 °C) with a CER as low as $1.92 \cdot 10^{-59}$.

Table 2 CER of the ADC for different supply voltages, at typical and worst corners

Corner	Power supply [V]	t_{margin} [ns]	τ_L [ps]	$-t_{margin}/\tau_L$	CER [error/sample]
(TT, 27 °C)	1.20	17.4	29.0	– 601	$< 10^{-258}$
	1.14	14.7	33.5	– 438	$< 10^{-186}$
	1.08	11.4	39.8	– 287	$< 10^{-121}$
(SS, 85 °C)	1.20	9.9	37.6	– 264	$1.96 \cdot 10^{-112}$
	1.14	6.4	44.8	– 142	$1.92 \cdot 10^{-59}$
	1.08	1.4	52.3	– 26.7	$4.95 \cdot 10^{-9}$

Table 3 Performance comparison of similar SAR ADCs

Specifications	[21] ^a	[22] ^a	[23] ^a	[24] ^a	[25] ^a	[26] ^a	This work*
Technology [nm]	65	65	65	180	65	65	65
Resolution [bit]	10	10	10	10	12	10	10
Supply Voltage [V]	1	0.8	1	1	0.6	1.3	1.2
Samp. Freq.[MS/s]	50	50	1	10	10	8	12
Input Freq.[MHz]	25	6.25	0.5	1	5	4	5.96
SNDR [dB]	56.6	58	54.4	60.97	64.3	57.7	59.8
ENOB [bit]	9.1	9.35	8.74	9.83	10.4	9.07	9.65
Power [μ W]	820	120.7	1.9	98	83	12.8	151.4
FoM ₁ [fJ/Conv. step]	29.7	14.8	4.4	11	6.2	2.5	15.8
FoM ₂ [dB] [@]	161.4	165.1	168.8	167.4	172.1	172.6	165.8
Core Area [mm ²]	0.039	0.012	0.027	0.086	0.1	0.04	0.074

^aMeasurement typical results, *Post-layout simulation results, @FoM₂ = SNDR + 10log($f_{sample}/(2 \cdot Power)$)

A summary of the simulation results of this design is shown in Table 3, alongside other published work measurement results for similar topology, resolution and fabrication process.

5 Conclusions

A low power, differential, asynchronous 10-bit SAR ADC was successfully designed, drawn to layout and simulated. In the topology, it is employed split binary-weighted capacitive arrays, to reduce the circuit area, and the merged capacitor switching scheme, to reduce the power consumption. Improved switches were designed for the sample-and-hold circuit to warrant the linearity of the ADC. Finally, a reduced kickback noise comparator was applied, which presented low power consumption, although additional transistors were required to discharge internal nodes. All the modifications resulted in an ADC with a performance comparable with the best circuits of the literature. In post-layout simulations, at maximum sampling rate of 12.0 MS/s, the circuit achieved an ENOB of 9.65 and a power consumption of 151.4 μ W, leading to a Figure of Merit of 15.8 fJ/Conversion-step; at 10.0 kS/s sampling rate, the ENOB is almost the same, 9.63, but the power

consumption is cut to only 0.26 μ W. These results show that the implemented ADC can be employed in a wide range of low power, moderate resolution systems as expected.

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Compliance with ethical standards

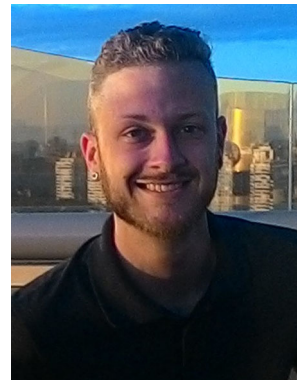
Conflict of interest The authors declare that they have no conflict of interest.

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