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Automated top-down pruning optimization approach in RF power amplifier designs

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Abstract

This study presents an automated high-accuracy optimization approach for designing high-performance radio frequency high power amplifiers (HPAs). The amplifier is designed by applying a *top-down pruning optimization* approach that automatically converts the given HPA with lumped elements (LEs) to the HPA with distributed elements (DEs). Firstly, the lumped element HPA is designed based on a *bottom-up optimization* presented in Kouhalvandi et al. (2019 11th international conference on electrical and electronics engineering (ELECO), pp 510–513, 2019, 10.23919/ELECO47770.2019.8990407), then the LE amplifier is decomposed into basic unit cells that consist of one capacitor (C) and one inductor (L). For each LC unit, a suitable transmission line cell network is selected from predefined models by considering the maximum a posterior (MAP) metric. The component values of the resulting HPA design with DEs are optimized using *Bayesian Optimization* to achieve the desired design specifications. The overall proposed automated optimization accelerates the design process and outperforms the amplifier's specifications that is constructed with DEs, automatically. The optimization starts with LE amplifier designs for keeping high linear gain performance and is converted to the HPA with transmission lines for having ready to fabricate circuit design. The proposed approach is validated by designing three HPAs with GaN HEMT from 1.8 to 2.2 GHz operational band frequency with drain efficiency more than 50% and with minimum linear power gain of 14.5 dB in all band frequency.

Keywords Automated · Bayesian optimization · Bottom-up optimization · Distributed element (DE) · Lumped element (LE) · Matching network (MN) · High power amplifier (HPA) · Top-down pruning optimization · GaN HEMT

1 Introduction

Advanced wireless communication systems demand wide bandwidth, high efficiency, and reliable operation of high power amplifiers (HPAs). The complexity of the HPA circuits are increased dramatically to meet the new requirements [2] due to the nonlinear behavior of the high power radio frequency (RF) transistors, wideband responses of the passive components, coupling effects of the transmission lines, and so on [3]. Therefore, various design methods have been studied to improve the performances of HPA designs. The traditional HPA design methodologies such as Class-F/F^{-1}, Class-J, and Class-E are evaluated deeply with several kinds of modified configurations and different devices such as Gallium Nitride (GaN), Gallium Arsenide (GaAs), and Laterally-Diffused Metal-Oxide Semiconductor (LDMOS) [4].

Over the past decades, optimization techniques for RF and microwave designs are receiving more attention [5] as

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described in the following. The real frequency technique (RFT) [6] and simplified real frequency technique (SRFT) [7] are two effective methods for designing broadband matching networks (MNs) that are applied in several studies of HPA designs [8, 9]. These techniques are mainly used to specify both the initial structure and the initial component values to be applied to the computer-aided optimization algorithms. In [10], a systematic method based on source-pull/load-pull simulations is used for designing a highly efficient power amplifier that the source impedances are optimized in the way that: they match to 50-Ω in large frequency bandwidth. Highly efficient broadband power amplifier is designed by using a slightly modified SRFT which provides harmonically optimized matching networks [11]. In another approach presented in [12], a method defining the optimal impedance regions is applied. Theses regions are obtained by using stochastic reduced-order models and Voronoi partition [13], and this method results in a high power added efficiency (PAE). Artificial neural networks [14], shape-preserving response prediction [15], and space mapping technique [16] are some of the widely accepted intelligent optimization algorithms. These methods mostly focus on optimizing one of the key parameters in designing HPAs, such as efficiency or gain and have successful performances when the data dimension of the parameter space is not huge.

In this study, to overcome the mentioned design optimization difficulties, we propose a novel optimization-oriented method with a combination of presented *bottom-up optimization* method in [1]. The proposed *top-down pruning optimization* method [17], converts the designed HPA with LEs to the HPA that is consisting of DEs. This conversion is performed for inheriting the high gain performance of the HPA design with LEs [2], and for making the design ready to be realized and fabricated. The proposed method is performed in an automated environment that is based on a top-down pruning approach [5] and implements Bayesian optimization (BO) [18, 19] for sizing design parameters. In our proposed method firstly, the lumped-element HPA is designed by applying the presented bottom-up optimization method in [1]. Then, input and output MNs are divided into unit cells consisting of one capacitor (C) and one inductor (L). For each inductor-capacitor network, different DE candidate networks chosen from [10, 20–22] are substituted for each unit block. For each LC network, the best fitted DE network is determined by selecting maximum a posteriori (MAP) metric [23] based on the BO method [18] to maximize the fitness of S-parameters of LE and DE unit blocks. For input and output MNs, these partitions and optimization process are performed and finally, a high-performance HPA design with DEs is created.

The general form of this study is as follows: In Sect. 2, the theory of high efficiency and high gain HPA design is reviewed. Section 3 explains the design procedure and the proposed optimization method. Section 4 verifies the proposed optimization technique by designing three GaN high-electron mobility transistor (HEMT) HPAs in operation band frequency from 1.8 GHz to 2.2 GHz. Finally, Sect. 5 discusses the conclusion.

2 High-efficiency and high-gain HPA theory

To achieve high efficiency in HPA designs, overlaps between the voltage and current waveforms must be reduced at the internal current source plain of the transistor drain to minimize the dissipated power (P_{diss}) on the transistor. Figure 1 depicts an ideal HPA structure.

The drain efficiency is defined by (1) as follows:

$$\eta_D = \frac{(\mathrm{v_m i_m}).0.5\mathrm{V_{DS}I_{DS}} = \frac{\mathrm{P_{L,1f}}}{\mathrm{P_{DC}}}}{} \tag{1}$$

where

$$P_{DC} = P_{diss} + P_{L,1f} + \sum_{n=2}^{\infty} P_{L,nf} \tag{2}$$

$P_{L,1f}$ is the output power (power on the load) at the fundamental frequency, and $P_{L,nf}$ denotes output power at different harmonics. Detailed generation of other parameters in (1) and (2) are defined in (3)–(6), as below:

$$P_{diss} = \frac{1}{\mathrm{T}} \int_0^T v_{ds}(t).i_{ds}(t)dt \tag{3}$$

$$\begin{aligned} i_{ds}(t) =& I_0 + I_{1f}.cos(\omega_0 t) + I_{2f}.sin(2\omega_0 t) + \ldots \\ &+ I_{2n,f}.sin((2n)\omega_0 t) \end{aligned} \tag{4}$$

$$\begin{aligned} v_{ds}(t) =& V_0 + V_{1f}.cos(\omega_0 t) + V_{3f}.cos(3\omega_0 t) + \ldots \\ &+ V_{(2n+1)f}.cos((2n+1)\omega_0 t) \end{aligned} \tag{5}$$

$$\sum_{n=2}^{\infty} P_{L,nf} = \frac{1}{2} \sum_{n=2}^{\infty} V_n.I_n.cos(\theta_n) \tag{6}$$

In (6), V_n and I_n are voltage and current at the n^{th} harmonic with conduction angle θ_n. Therefore, the proper termination of the harmonics has a significant effect on HPA's performance.

The power gain (G_P) is defined as the ratio of power delivered to a load (P_L) to the available power (P_{in}) of the generator. Hence, the power gain is expressed as (7), and it demonstrates that for achieving the desired power gain in HPA designs, two parameters as P_L and P_{in} must be arranged considerably.

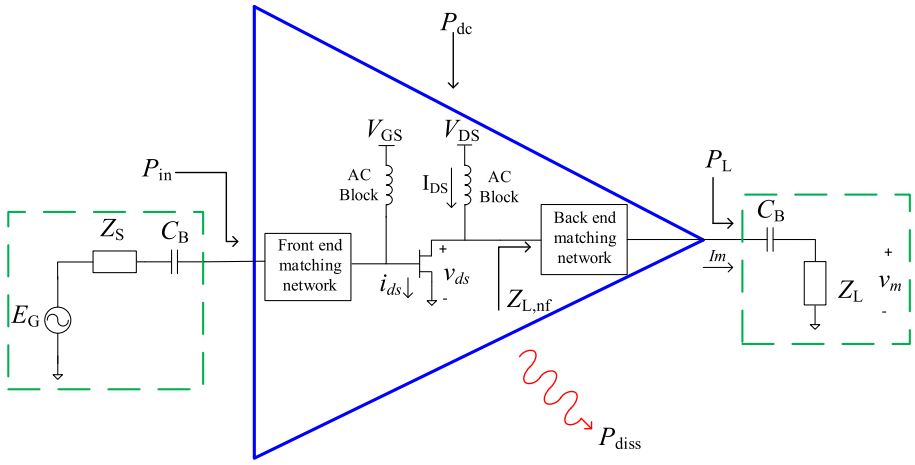


Fig. 1 High power RF amplifier architecture

$$G_P = \frac{\mathrm{P_L}}{\mathrm{P_{in}}} \tag{7}$$

3 Proposed optimization-oriented strategy

This section first reviews the presented bottom-up optimization approach in [1] results in designing LE power amplifiers. Then, the proposed top-down pruning optimization method for converting the given lumped element power amplifier to distributed element power amplifiers is described briefly. The proposed optimization method combines the main advantages of the lumped element design and distributed element design, as offering higher and flatter gain performance and manufacturing readiness, respectively [2]. The proposed optimization is applied in an environment constructed with a commercial electronic design automation (EDA) tool and a programming environment (i.e., numerical analyzer) [24], leads to an automated environment.

3.1 Designing a lumped element HPA with the bottom-up optimization method

This section reviews the brief description of the presented method in [1] for designing lumped element power amplifiers.

Figure 2 shows a general HPA design structure consisting of LC type lumped element matching networks. As it is clear, each front end and back end MNs consists of k and m LC type unit blocks, respectively. The presented bottom-up optimization method starts with one LC unit block in the input and output MNs. Then, the number of LC units are increasing automatically in both MN sides up to achieving the desired design specifications.

3.2 Proposed top-down pruning optimization method for designing a distributed element HPA

Power amplifiers are nonlinear systems where design specifications as power gain, efficiency, and output power are nonlinear functions. As it is evident, any HPA design consists of MNs that designing these networks are not straightforward, and large-signal operation is required for enhancing HPA's output specifications. In order to reduce design time, we propose using a top-down pruning optimization that seeks optimal topology and optimal component values by partitioning the general topology into smaller basic cells. At each step, only the parameters of the considered unit cell are optimized; hence the optimization approach is computationally effective.

The generation of *scattering parameter (S-parameter)* for the front end MN presented in Fig. 2, is expanded in Fig. 3 where for each LC unit block, the transfer scattering matrix (TSM) [7] is specified. The descriptions in the

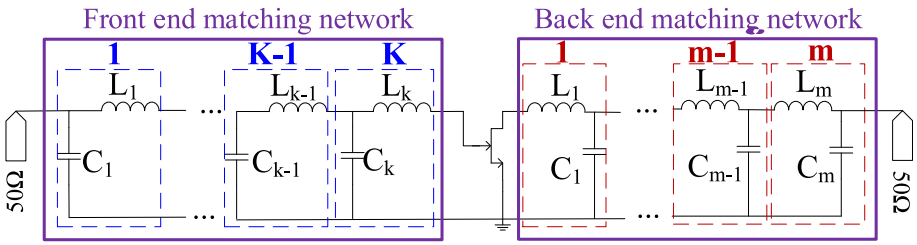


Fig. 2 HPA design topology with bottom-up optimization method presented in [1]

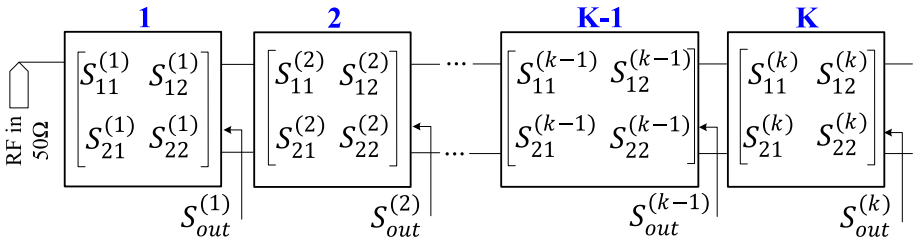


Fig. 3 Generation of scattering parameters for the front end matching network of Fig. 2

sequel given for the front-end MN, are also valid for the back-end MN. As Fig. 3 shows, the S-parameter of k^{th} block depends on the S-parameter of the $(k-1)^{\text{th}}$ block. Thus, scattering parameters of the k cascade blocks are explained as (8)-(10):

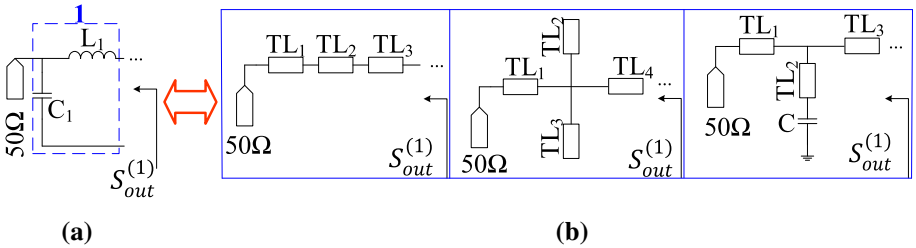
$$S_{out}^{(1)} = S_{22}^{(1)} \tag{8}$$

$$S_{out}^{(2)} = S_{out}^{(1)} + \frac{S_{12}^{(2)} S_{21}^{(2)}}{1 - S_{out}^{(1)} S_{11}^{(2)}} S_{11}^{(2)} \quad \ldots \tag{9}$$

$$S_{out}^{(k)} = S_{out}^{(k-1)} + \frac{S_{12}^{(k)} S_{21}^{(k)}}{1 - S_{out}^{(k-1)} S_{11}^{(k)}} S_{11}^{(k)} \tag{10}$$

Each LC unit block is substituted with one of the candidate topologies studied in [10, 20–22], where Fig. 4 shows these equivalent topologies for the case of the front end matching network. For the sake of simplicity, these candidate circuits are given for the first cell where the input port impedance is 50 Ω. The other cells' candidate circuits are obtained considering the respective port impedances of the neighboring stages and are designed using the equation presented in (10).

The detailed step descriptions of the proposed methodology are given in Algorithm 1. Firstly, a lumped element HPA is designed and optimized using the bottom-up optimization method presented in [1] (Step-1). Then, the whole HPA design is decomposed to LC unit cells as Fig. 2 shows (Step-2). The lumped element unit cells in the HPA topology of Fig. 2 are sequentially replaced by one of the distributed unit cells of Fig. 4.b starting from RF-in 50 Ω to RF-out 50 Ω (Step-3). For each considered unit cell, the best distributed unit cell and component values are evaluated based on the BO method [18], where the objective functions are defined in terms of S-parameters. BO is a supervised learning algorithm that is based on Gaussian Processes (GP) as surrogate models [25, 26] (Step-4). The distributed unit cell with optimum MAP is selected as the best-fitting model for each unit cell (Step-5). Once the considered lumped element unit cell is replaced with the optimum DE cell topology, the circuit parameters are optimized using the method presented in [27]. In this step, the following design parameters as: output power P_{out}, G_P, and PAE of the whole HPA are used to construct objective functions. It should be noted that we optimize only the parameters of the replaced distributed unit cell while the parameters of the other cells are kept constant. Therefore, the optimization cost at this stage is substantially reduced as the parameter space is minimized (Step-6). In the case of not obtaining desired design goals, additional transmission lines are added to the MNs, and the design parameters are optimized using *random iteration optimization* (increasement/decrement) presented in [24] (Step-7).



(a) **(b)**

Fig. 4 **a** First unit LC block of Fig. 2; **b** Equivalent DE design models for unit block of part a

Algorithm 1 Automated HPA design with DEs through top-down pruning optimization method

1: Design lumped element HPA circuit with the automated bottom-up optimization method [1].
2: Decompose input & output matching networks to basic units consisting of LC cells.
3: Start from the input port to the output port, replace each unit cell with the candidate distributed cells that are presented in Fig.4.
4: Evaluate the performance of each DE candidate cell using the BO method.
5: Select the distributed element unit cell topology which has an optimum MAP for each LC unit.
6: Optimize element values of the selected distributed element topology using the method described in [27], while the element values of the remained cells are kept constant.
7: If the desirable HPA design goals are not achieved yet, add additional transmission lines to MNs and obtain design parameters by random iteration optimization [24].

4 Practical HPA designs using top-down pruning optimization method

For validating the proposed optimization method, three HPAs are designed and optimized. For these designs, Ampleon CLF1G0060-10 GaN high-electron mobility transistor (HEMT) that is biased with 50 (V) and 40 (mA) is used. A wideband and nonlinear model of the transistor is provided by the Ampleon company for nonlinear analysis. The designs are implemented on Rogers RO4350B substrate with ε_r=3.66, and a thickness of 0.508 mm.

Lumped element HPA design The lumped element HPA, consists of passive components (i.e., inductor and capacitor), is designed by implementing the optimization algorithm presented in [1]. Figure 5 shows the designed HPA with lumped elements in [1] with an output power of around 40 dBm. The S-parameter simulation results with power gain and power added efficiency specifications are summarized in Fig. 6 for the optimized HPA of Fig. 5. The optimized HPA has linear power gain larger than 17 dB, and PAE specification is between 47–77.4% for the operation band frequency of 1.8–2.2 GHz.

Distributed element HPA design The proposed top-down pruning optimization method, described in Algorithm 1, is applied to the optimized HPA with lumped elements (i.e., Fig. 5). For this type of design, the initial drain biasing line is formed with a quarter wavelength transmission line with a capacitor bank including pF, nF, and uF value capacitors. The gate biasing network includes a quarter wavelength transmission line with a serial resistor to improve the stability at lower frequency bands [28]. Furthermore, a

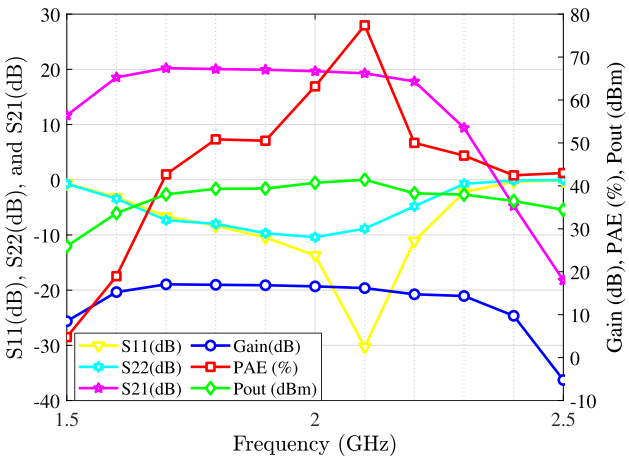


Fig. 6 Simulation results of the optimized HPA in [1]

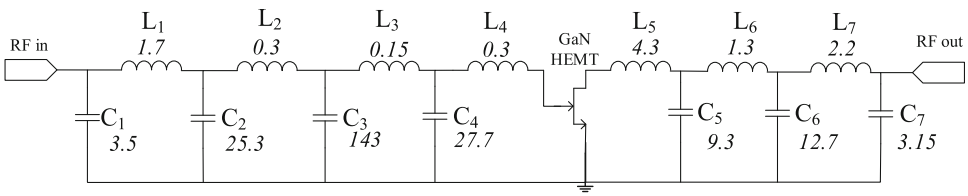
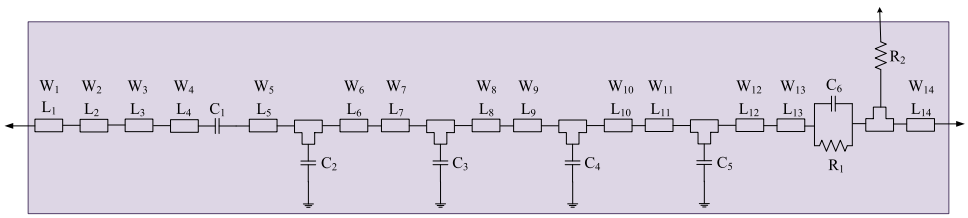


Fig. 5 Lumped element HPA optimized in [1]; Units for capacitors and inductors are pF and nH, respectively



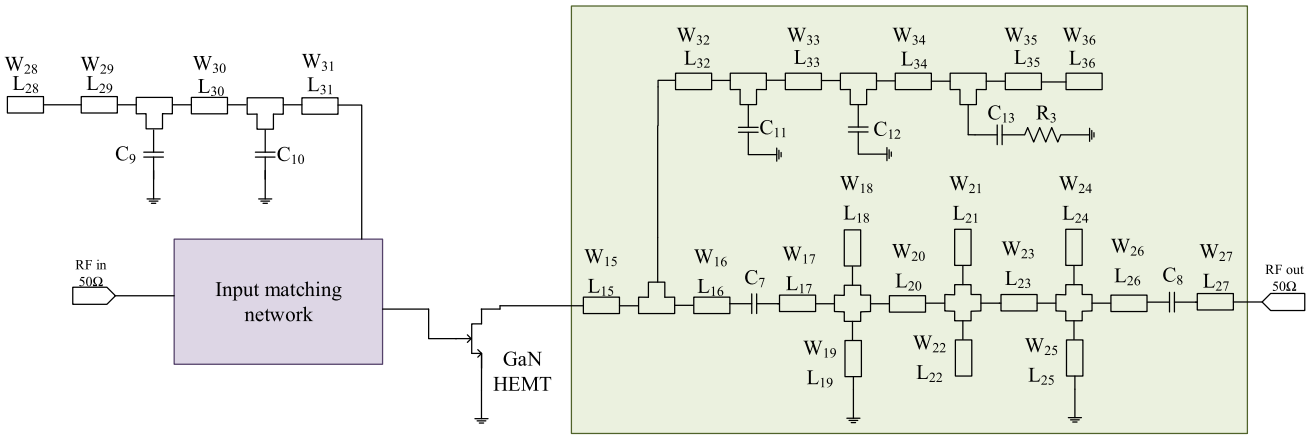


Fig. 8 First optimized HPA

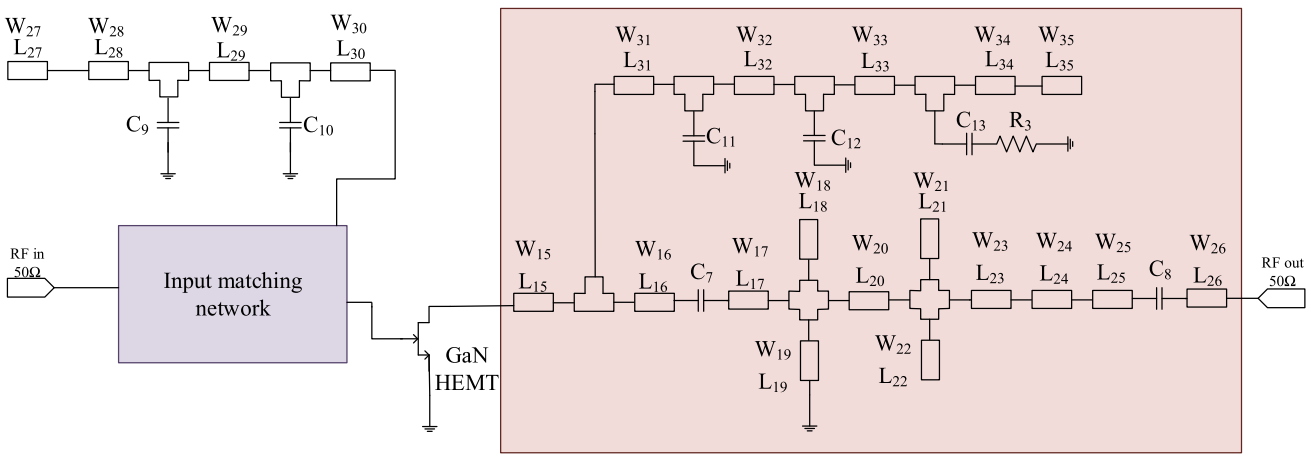


Fig. 9 Second optimized HPA

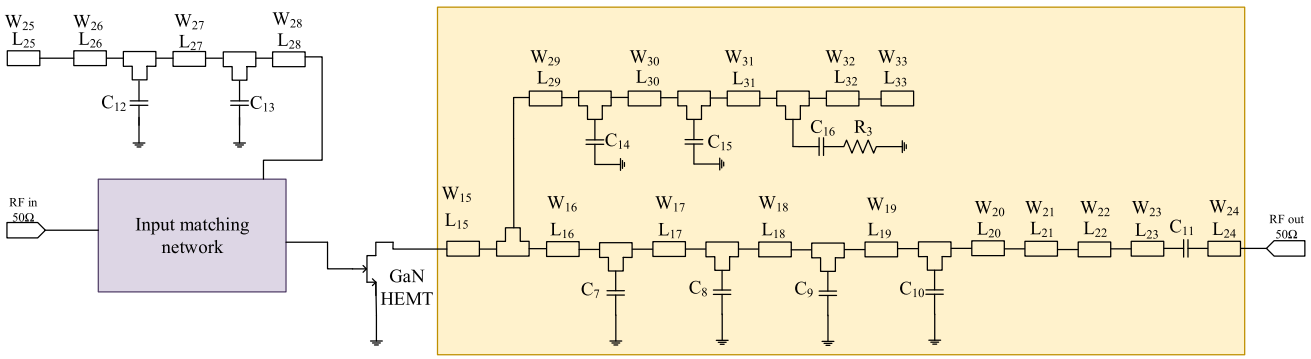


Fig. 10 Third optimized HPA

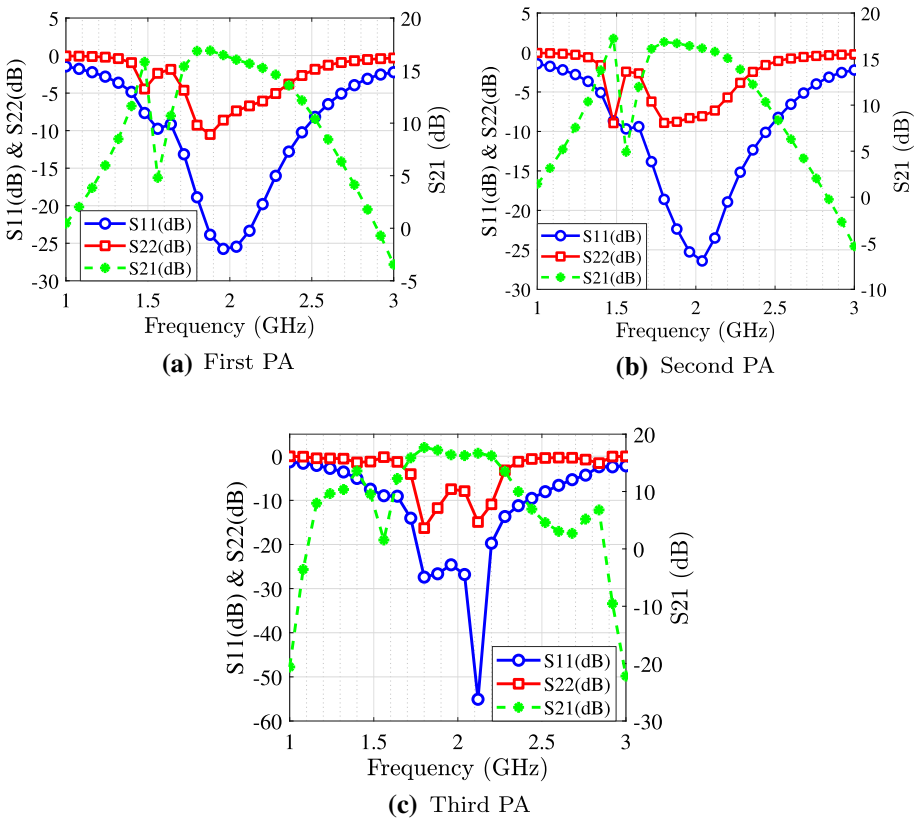


Fig. 11 S-parameters versus frequency for optimized DE power amplifiers

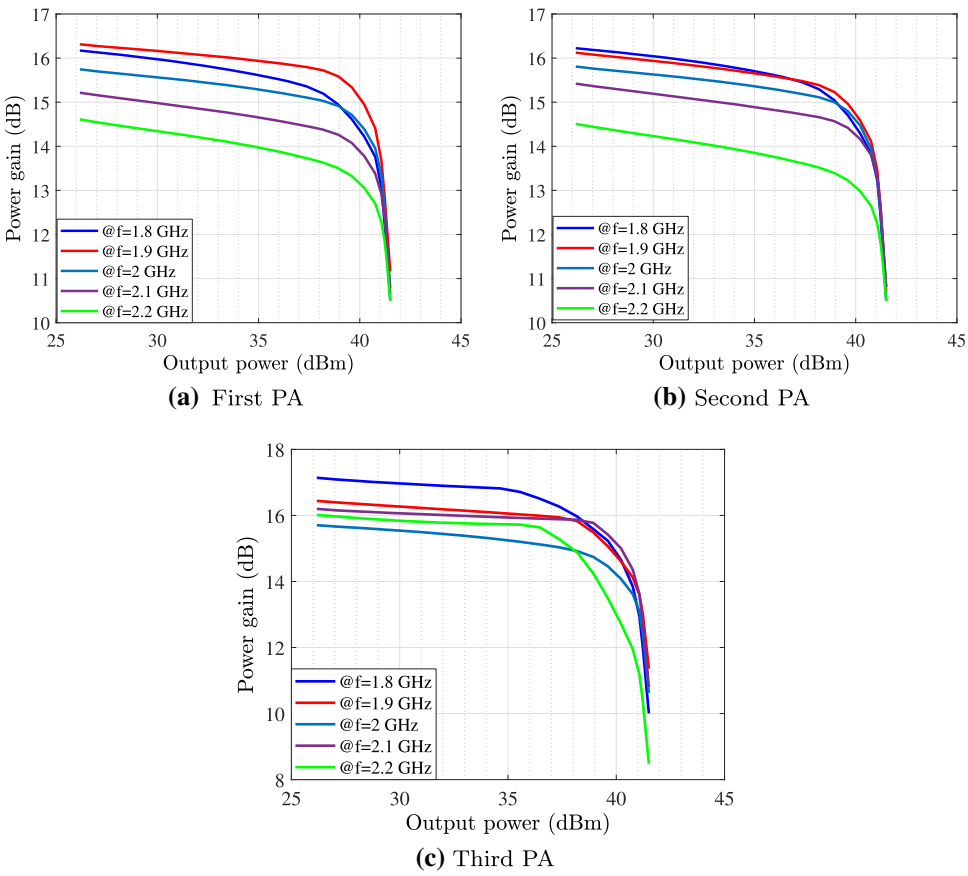


Fig. 12 Power gain versus output power at different frequencies for optimized DE power amplifiers

parallel capacitor and resistor network also attached to the RF signal line to prevent even mode oscillations. Basic design circuit rules, presented in [3], are also applied to achieve a realizable circuit layout such as implementations of T sections for the component connections, minimum and maximum width for the microstrip lines, and suitable capacitor and resistor values. Figure 7 shows the common input matching network for the three designed HPAs, as shown in Figs. 8, 9, and 10.

Optimized design variables for Fig. 8 are as following: W_{1-36} = [4.8, 4.0, 3.0, 1.07, 1.5, 1.5, 1.5, 1.5, 1.5, 1.5, 1.5, 1.5, 3, 1, 4, 3.7, 3.7, 4.1, 4.1, 3.7, 5.3, 5.3, 3.7, 5.3, 5.3, 3.7, 3.7, 8, 1, 1, 1, 1, 1, 1, 1, 8] mm, L_{1-36} = [1.6, 1.7, 1.8, 3, 1, 1, 1, 1, 1, 1, 1, 1, 2, 0.2, 0.2, 8.16, 1.6, 5.4, 3.6, 1.6, 5.5, 6.8, 1.6, 3.4, 1.7, 1.6, 1.6, 8, 1, 1, 26.4, 26.4, 1, 1, 1, 8] mm, C_{1-13} = [40.9, 0.28, 0.04, 1.08, 3.6, 1.6,27.50, 24.5, 10e3, 2.2, 2.2, 10e3, 10e6] pF, R_{1-3} = [10, 10, 10] Ω.

Optimized design variables for Fig. 9 are as following: W_{1-35} = [4.8, 4.0, 3.0, 1.07, 1.5, 1.5, 1.5, 1.5, 1.5, 1.5, 1.5, 1.5, 3, 1, 4, 3.8, 3.8, 3.5, 3.5, 3.8, 5.7, 5.7, 3.8, 3.8, 3.8, 3.8, 8, 1, 1, 1, 1, 1, 1, 1, 8] mm, L_{1-35} = [1.6, 1.7, 1.8, 3, 1, 1, 1, 1, 1, 1, 1, 1, 2, 0.2, 0.2, 9.56, 1.6, 4.5, 3.4, 1.6, 5.8, 6.9, 1.6, 1.6, 1.6, 1.6, 8, 1, 1, 26.4, 26.4, 1, 1, 1, 8] mm, C_{1-13} = [40.9, 0.28, 0.04, 1.08, 3.6, 1.6, 27.50, 32.50, 10e3, 2.2, 2.2, 10e3, 10e6] pF, R_{1-3} = [10, 10, 10] Ω.

Optimized design variables for Fig. 10 are as following: W_{1-33} = [4.8, 4.0, 3.0, 1.07, 1.5, 1.5, 1.5, 1.5, 1.5, 1.5, 1.5, 1.5, 3, 1, 4, 0.55, 2.48, 9.7, 9.7, 9.7, 9.35, 6.16, 7.04, 7.04, 8, 1, 1, 1, 1, 1, 1, 1, 8] mm , L_{1-33} = [1.6, 1.7, 1.8, 3, 1, 1, 1, 1, 1, 1, 1, 1, 2, 0.2, 0.2, 4.7, 0.7, 0.216, 1.12, 9.5, 0.5, 9.3, 3.1, 3.1, 8, 1, 1, 26.4, 26.4, 1, 1, 1, 8] mm, C_{1-16} = [40.9, 0.28, 0.04, 1.08, 3.6, 1.6, 6.5, 32.2, 3.0, 7, 22, 10e3, 2.2, 2.2, 10e3, 10e6] pF, R_{1-3} = [10, 10, 10] Ω.

Figure 11 shows the S-parameter responses of the optimized final HPAs. The simulation results for S_{11} show lower than −13 dB with S_{21} higher than 15 dB in the operation band frequency. The simulated results of power gain over output power are shown in Fig. 12 from 1.8 to 2.2 GHz band frequency. Figure 13 depicts the output power, gain, and drain efficiency in the operation band at p3dB with average output power around 40 dBm. For all designed HPAs, the linear power gain is between 14.5 dB and 17 dB with drain efficiency more than 50% at *p3dB*.

On the other hand, it is of vital importance to ensure the stability of the designed amplifier overall frequency band of interest. Rollett's stability factor is an important and

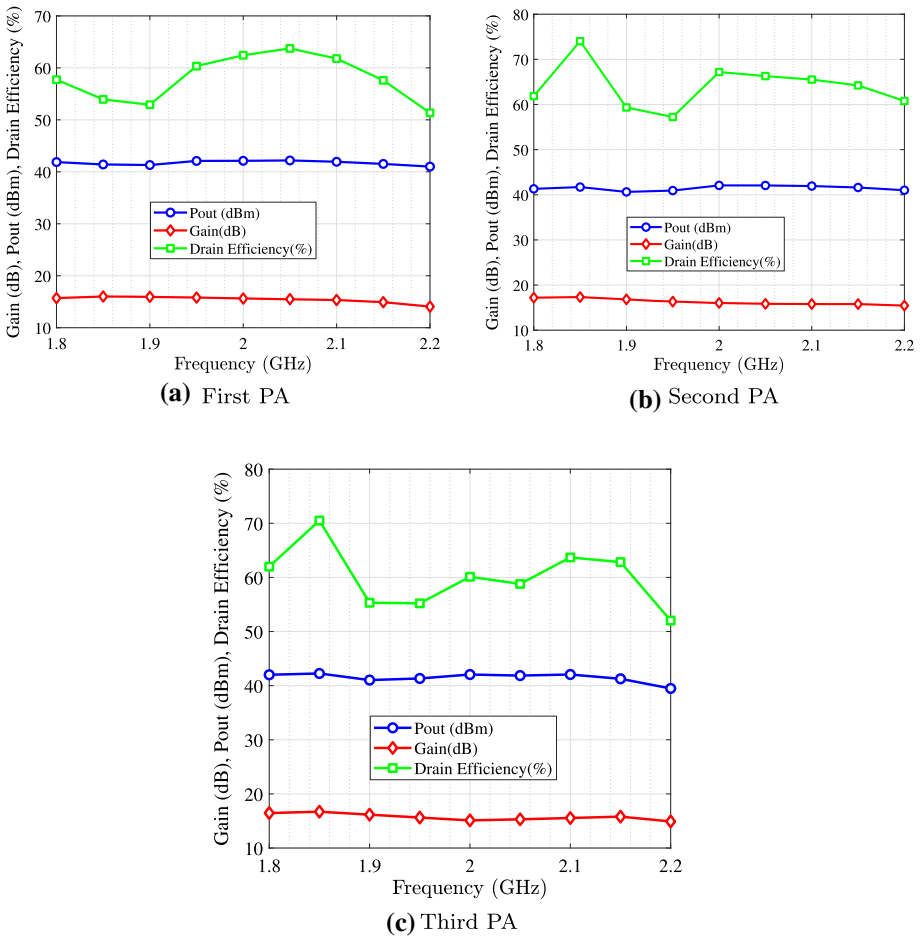


Fig. 13 Output power, gain, and drain efficiency results at 3 dB gain compression for optimized DE power amplifiers

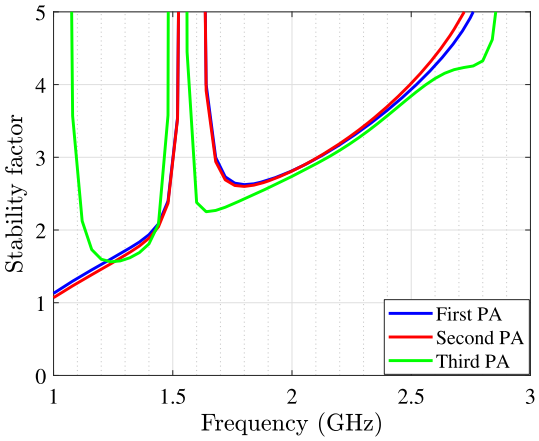


Fig. 14 Stability factor of optimized DE power amplifiers

useful figure conventionally in HPA designs. We have derived Rollett's stability factor *(K)*, of the designed HPAs for inside and outside of the operation band, and the results are presented in Fig. 14.

5 Conclusion

An automatically innovative approach for converting lumped element power amplifier to the RF HPA design with distributed elements is proposed in this paper. The automated optimization method is based on the top-down pruning optimization approach. The novelty of this work is based on getting the benefit of high gain performance in a lumped element design and preparing the HPA for fabrication in distributed elements with high-efficiency and high-gain performance. To improve first-pass design success, design rules and manufacturing requirements of the layout are implemented into the optimization algorithm due to its flexible structure. In order to demonstrate the validity of this design approach, a high linear performance HPA with lumped element is designed by using the bottom-up optimization method. Then the proposed method is applied for designing and optimizing three HPAs with transmission lines result in high-performance designs. The simulation results of designed HPAs with transmission lines show good agreement with the results of designed HPA with lumped elements in [1].

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Compliance with ethical standards

Conflict of interest One of the authors (O. Ceylan) has taken up a position at Maury Microwave CA/USA during the elaboration of this work, having no conflict of interest to declare. The other authors have declared no conflict on interest.

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