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A Schmitt-trigger based low read power 12T SRAM cell

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Abstract

In this article, a Schmitt trigger based 12-Transistors(ST12T) static random-access memory (SRAM) bit-cell has been proposed. The Read Power of proposed cell is reduced by 29.17%/ 24.14% /7.66% /5.87% /7.67% /16.62% when compared to 6T/ 7T/ TA8T/ 9T/ PPN10T/ D2p11T SRAM cells. Proposed ST12T cell also shows 1.52× and 1.86× lesser variability in read current and read power respectively as compared to conventional 6T SRAM cell. Further, the write access time/read access time of the proposed topology are improved by 1.71 × /1.82× as compared to 6T SRAM cell. The read power delay product of proposed ST12T cell is minimum with variation in supply voltage from 0.5 to 1 V when compared with all considered SRAM cells. ST12T SRAM cell also exhibits 26.82% and 8.87% higher read static noise margin and write static noise margin respectively as compared to conventional 6T SRAM cell. This may be attributed to Schmitt trigger design of inverters in core latch of proposed SRAM cell. The proposed bit-cell is free from half select issue and supports bit interleaving format. Authors have used cadence virtuoso tool with Generic Process Design Kit 45 nm technology file to carry out simulation.

Keywords Read stability · Low power · Process variation · Static random-access memory (SRAM) · Write ability · Half select

1 Introduction

Improvement in integration density and device performance are logical outcomes of aggressive transistor scaling with each technology generation. The standby power reduction is crucial in battery operated devices such as portable medical equipment, IoT devices, cell phones etc. The effective solutions to control enhanced leakage power is reduction in supply voltage or improvement in circuit level techniques. Minimizing supply voltage is a tested and effective measure as it declines dynamic power in quadratic manner [1]. Therefore, supply voltage scaling becomes a major focus in low power design. However, with the reduction in supply voltage, the increase in sensitivity of various parameters of circuit to process variations is also observed [2]. The circuit operation is also limited by process variations, specifically in memory topologies, where many similar circuits are interconnected to execute required operation [3]. In a system-on-chip (SOC) device, embedded memories are expected to occupy 80–85% of total die area [4]. Intra-die variations in nano-scaled SRAM bit-cells include line edge roughness (LER), random dopant fluctuations (RDF) etc. These variations may result in threshold voltage mismatch between end- to-end placed transistors in embedded memory [5].Furthermore, many techniques such as dynamic V_{dd}, source biasing [6] etc. have been adopted in order to minimize process variation impact. At higher voltage levels, the aspect ratio enhancement is most popular way to improve read and write stability of memory circuits. However, increase in transistor dimensions may also lead to further enhancement of leakage current. In deep sub-micrometer technology lowering of supply voltage becomes challenging due to reduced static noise margins specifically during read operation [7]. This degradation in SRAM parameters may get influenced further with variation in operating conditions such as temperature. It may also lead to flipping of data during standby mode of device. As an Illustration,

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substantial variation in data retention voltage (DRV) can be observed with variation in temperature at different process corners [8]. DRV is the minimum supply voltage in SRAM cell for which data can be stored reliably. Many factors such as threshold voltage, sizing constraints etc. are responsible to impact DRV [9]. Moreover, rise in threshold voltage can be observed with increase in transistor width as depicted in Fig. 1(a). The 8–10% variation of threshold voltage is noticed as the NMOS transistor width is increased from 120 to 450 nm. Subsequently, fixing the topology with minimal variation in width to length ratio of transistors is another major design aspect. The conventional six transistors static random-access memory (referred to as conv. 6T SRAM hereafter) cell, shown in Fig. 1(b), suffers from static noise margin reduction with supply voltage scaling. In order to execute non- destructive, read and write operations cell ratio, CR (pull down transistor width to access transistor width ratio) and pull-up ratio, PR (pull-up transistor width to access transistor width ratio) should be kept greater than one and less than or equal to one respectively. This condition is widely understood as access transistor sizing (ATS). At higher supply voltages, transistor sizing is sufficient to ensure correct functioning of conv. 6T static memory circuit. The increased local and global process variations at low voltage levels reduce the read and write margins of conv. 6T SRAM cell to undesirable levels. Apart from these challenges half select disturbance issue is also required to be resolved in order to support complex array mechanisms such as bit interleaving format.

2 Related works

In order to address aforementioned static memory design issues, several configurations of static random access memory bit-cells have been reported. Farkhani et al. [10] presented a modified version of 6T SRAM cell for low voltage operation. This topology followed the single end read operation and required write assist circuit. Another attempt to reduce read and write power was made by Chang et al. [11]. Author proposed a differential read/write 8T circuit that was driven by its bit-line pair. However, the proposed topology was not tested to process variations. Single ended feedback controlled 8T SRAM cell topology was presented [12] to attain low leakage power. Further, 12T SRAM topologies [13, 14] were projected for low power applications. However, impact of variability of read current and read power during process variations were not taken in to consideration. Furthermore, few topologies [15, 16] attempted to enhance stability parameters along with reduced stand-by power. liu et al. [16] projected 9T SRAM cell topology in order to enhance read SNM of bit-cell with decline in leakage power. The sleep transistor logic was utilized in cell for controlling leakage current. A 7T SRAM cell was proposed by Ansari et. al [17] for enhancement of RSNM of the topology. The effect of process variations on performance of cell is also presented. Though the topology dissipates high read power. Different techniques such as WRE8T [18], read decoupled [19], common word line with tunable access [20] etc. were investigated for simultaneous enhancement of read stability and write ability without any assisting circuitry.

Many topologies based on differential write and read operation have been also investigated. This include topologies with sleep NMOS [13, 18], read buffers [21–23], and swing voltage control [24, 25] to reduce power while maintaining stability. P-P-N based 10T SRAM cell [26, 27] exhibited tolerance to process variations. Half-select issue of these cells were eliminated in order to achieve bit interleaving capability. Though, these topologies had higher access time during read and write operations. Furthermore, Sharma et al. [28] proposed a data dependent power supplied SRAM cell for expanded write/read noise margin and low leakage operation. The read stability and write ability issues were addressed simultaneously in [28] by employing read decoupled technique. Also, the circuit in this topology takes liberty to substantially reduce hold power due to data aware power supplied technique. This also make circuit capable for addressing IoT applications. Half select issue was also addressed in this cell. 7T SRAM topology [29] displayed improvement in various performance matrices viz. read current, read power etc., as compared to that of standard 6T SRAM cell. However, this topology makes use of read assist circuitry and necessitates silicon area, which is a substantial trade-off as seen in current demand for higher memories and reduced device sizes. Ahmed et al. [30] proposed another robust 11T SRAM cell which replaced conventional inverter in core latch with Schmitt trigger inverter for

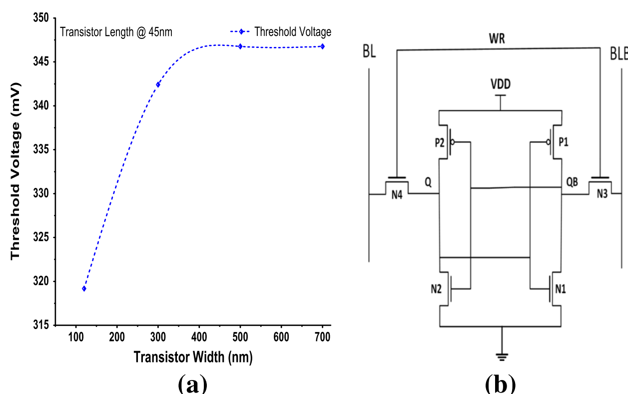


Fig. 1 **a** Threshold voltage versus transistor width. **b** Conventional 6T SRAM Cell

enhancement in several performance matrices of SRAM cell. A hybrid circuit is proposed which utilized both schmitt trigger as well as conventional inverter in its core latch [31].

Yamaoka et al. [32] predicted that the minimum voltage on which a circuit can perform correct read and write operation is limited by process variations. Therefore, in order to accommodate the above discussed vital challenges, a single ended read and differential write Schmitt trigger-based 12-T (ST12T) SRAM cell is proposed with following features:

(i) The read power dissipation is observed as minimum when compared with all considered cells.
(ii) In proposed ST12T SRAM cell, write access time is minimum of all considered cells which signify a reasonable improvement in write performance.
(iii) The read static noise margin and write static noise margin are improved by 26.82% and 8.93% respectively, when compared with conv. 6T SRAM cell. Also, the proposed cells works at minimum data retention voltage when compared with all considered cells
(iv) The read power delay product is minimum among all considered SRAM cells.

The proposed circuit, single ended read and differential write Schmitt trigger-based 12-T SRAM cell hereafter will be referred to as, ST12T. As mentioned in Table 1, the proposed ST12T cell is compared with conv. 6T, 7T [17], 8T [20], 9T [16], 10T [26] and D2p11T [28] SRAM cells.

Presented article is organized in following way. Section 3 details about the circuit description along with half select issues. The observations and analysis of proposed ST12T SRAM cell parameters along with the comparison with conv. 6T, 7T [17], 8T [20], 9T [16], 10T [26] and D2p11T [28] SRAM cells are discussed in Sect. 4. Finally, concluding remarks are given in Sect. 5.

3 Proposed ST12T SRAM cell design

3.1 Inverter based on Schmitt trigger design

A number of researchers have reported about the conventional cross coupled inverter latch parameters such as stability, access time, I_{on}/I_{off} ratio etc. These parameters doesn't behave promising with scaling of supply voltage. Said parameters may be improved at lower supply voltage with modification in core latch inverter structure. Kulkarni et al. [33] utilized a Schmitt- trigger inverter to achieve improved inverter characteristic. Schmitt- trigger (ST) behaves like a comparator that incorporates positive feedback. The basic ST inverter utilized for design is shown in Fig. 2(a). The difference in DC characteristics of ST inverter and conventional inverter for low to high transition of input data at 1V supply voltage is depicted in Fig. 2(b). Let us consider the input transition from 0 to 1. For conventional inverter, the transition in output starts from 1 to 0 as soon as the voltage at input approaches to threshold voltage V_{th} of pull-down transistor. However, for ST-inverter when output voltage is high the feedback NMOS transistor(NF) is switched on and this ensures the voltage at node X at V_{dd}. In addition to this transistor N2 also add-up certain resistance in ground path. Therefore, the minimum voltage required to switch the output from high to low, known as switching threshold, will be higher and switching time gets reduced.

The capacitance C_{gd} of transistor N1 in ST-inverter connects input to output. If in case, input is changed instantaneously from 0 to V_{DD}, the voltage over C_{gd} will also instantaneously change from V_{DD} to -V_{DD}. However, this can only happen in case infinite current flows through C_{gd}. When input of an ST-inverter suddenly rises from 0 to V_{DD}, this will turn on transistors N1 and N2 and switches off transistor P1. Transistor N1 in ST-inverter can-not sink constant current unless it crosses V_x (voltage at node X). Also, even in that case current will be far from infinite value. Therefore, C_{gd} can only decrease its value slowly. At the precise instance where the input switches, the output will have to follow same amount of voltage. Therefore, C_{gd}

Table 1 Different bit-cell topologies considered for comparison

Cell Feature	Conv. 6T	7T [17]	8T [20]	9T [16]	10T [26]	D2p11T [28]	Proposed 12T cell
Read/Write	Diff./Diff.	Diff./Diff.	Diff./Diff.	Diff./Diff.	Diff./Diff.	SE/Diff.	SE/Diff.
Bit-lines	2-BL/BLB	2-BL/BLB	2-BL/BLB	2-BL/BLB	2-BL/BLB	3-BL/BLB/ RBL	2-BL/BLB
Control Signals	1-WL	2-WL/RWL	2-WL/CWL	2-WR/RD	2-WL/VGND	4-WL/RWL /ZWL/RGND	3- WL/WLB/RWL
Area	1	1.41	1.44	2.13	2.57	2.44	2.96

SE:Single ended, WL:Word Line, RD:read, VGND:Virtual Ground, RWL:Read word line, Diff.:Differential, RBL:Read bit-line, CWL:control word line, RGND:Read path ground, WLB:Inverted Word-line signal

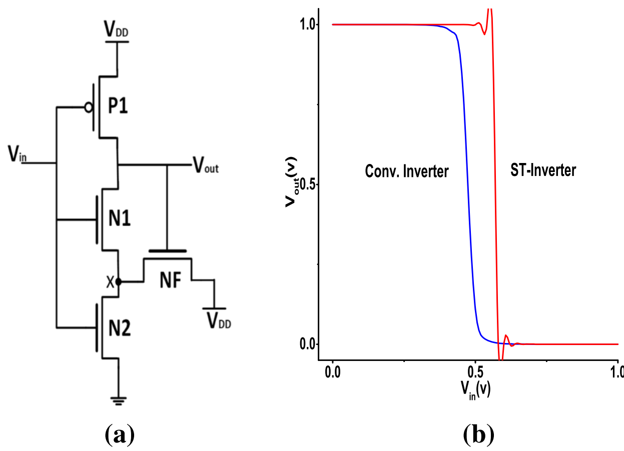


Fig. 2 **a** Schmitt trigger (ST) based inverter design [33]. **b** DC Characteristics of conventional inverter versus ST inverter for 0 → 1 transition

(of N1) fight over the output voltage with other capacitance present at the output. The output voltage will also depend on those output capacitance. In the end, this causes the output to jump over some smaller voltage which appears in the form of spike [34]. In case we attach the capacitance at the output, the peak of spike will get smaller. However, the slew rate at the output will also get smaller.

Another added advantage of ST based SRAM is higher static noise margin due to improved inverter characteristic. Though, the ATS conflict of read stability and write ability still pertains in [33] (see Fig. 3(a)). Hence, a modified version of [33] was proposed in [35] (see Fig. 3(b)) which utilized separate signals to control NF transistor in core latch. In [33] gate node of NFL and NFR transistors are controlled by Q and QB node respectively whereas in [35] separate WL signal is provided for controlling gate node of these transistors. Since, with active NF transistor it is difficult to execute write operation due to voltage

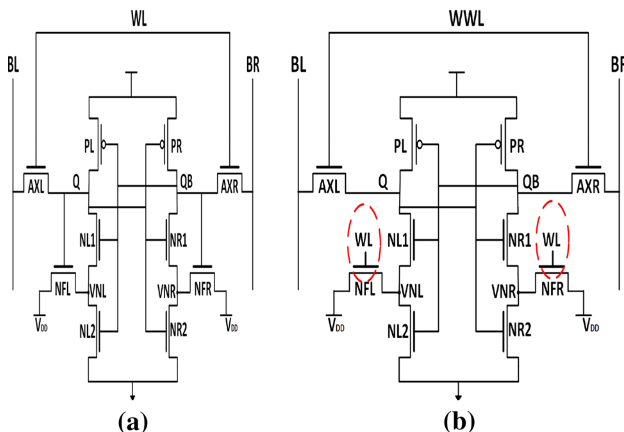


Fig. 3 **a** ST-based SRAM design [reported in [33]]. **b** Improved version of ST- based SRAM circuit [reported in [35]]

development at V_X node. The situation becomes severe in case of process variations because a weak '0' will also add some voltage to V_X node and this may result in write failure. Therefore, [35] improved the feedback mechanism and further resolved destructive read issue to certain level. Another effort to resolve this challenge has been made in presented article.

3.2 Detailed ST12T cell architecture

Figure 4(a) shows the schematic design of projected ST12T SRAM topology. The read '1' operation of proposed circuit is depicted in Fig. 4(b). Table 2 summarizes the status of control signals for different operations i.e. hold state, write and read operations. The projected topology operates in single ended mode during read operation and in differential mode for write operation. Proposed topology is asymmetrical and carries twelve transistors(12T). Transistors N1, N2, N3 and P2 form the right-hand side ST inverter of core latch. Whereas, transistors P3, N5, N6 and N7 forms the left-hand side ST inverter. In the presented work, we have employed N4 and N8 as separate access transistors for write and read operations and their gate controlled by RWL and WL signals respectively. Hence, it is possible to adjust the size of transistors of both inverters to improve write ability and read stability simultaneously. In order to address ATS issue, the read operation is kept single sided and write process is operated in differential mode. Low voltage at WL signal during read operation keeps left inverter silent. Therefore, the W/L ratio of right-hand side inverter is maintained for maximizing the read static noise margin. During write operation, transistor P1 and transistor N9 are turned off to make left-hand side inverter weaker than its complement [18]. In order to evaluate the switching threshold voltage V_{sth} (at node QB) during low to high transition, first we need to calculate voltage at node X i.e. V_X. The drain current can be written as,

$$I_D = A.exp\left(\frac{V_{GS} + \eta V_{DS}}{\frac{mkT}{q}}\right).\left(1 - e^{\frac{-V_{DS}}{\frac{kT}{q}}}\right) \quad (1)$$

where T is temperature, m is body effect coefficient, η is drain induced barrier lowering coefficient and A is directly proportional to W/L ratio of transistor. Since, the V_{DS} for the present case is above 150mV, therefore, the term $\left(1 - e^{\frac{-V_{DS}}{\frac{kT}{q}}}\right)$ can be ignored. The simplified equation turns out to be,

$$I_D = A.exp\left(\frac{V_{GS} + \eta V_{DS}}{\frac{mkT}{q}}\right) \quad (2)$$

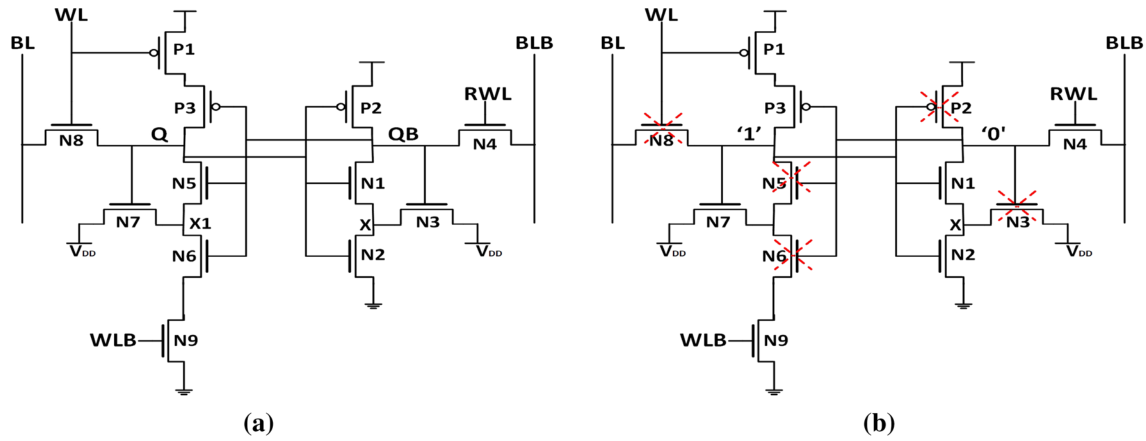


Fig. 4 **a** Proposed ST12T SRAM cell schematic. **b** Read '1' operation

Table 2 Operation table of Proposed ST12T SRAM cell

Signals	Read operation	Write operation	Hold state
RWL	V_{dd}	V_{dd}	GND
WL	GND	V_{dd}	GND
WLB	V_{dd}	GND	V_{dd}

Since both sides of the proposed circuit are not symmetrical. Let us first take the case of right-hand side of proposed topology represented in Fig. 4(a) which is being used for read operation. At node $Q_B = V_{out}$,

$$I_{P2} = I_{N1} \tag{3}$$

From Eqs. 2 and 3

$$A_{P2}.exp\left(\frac{(V_{dd} - V_{in}) + \eta_{P2}(V_{dd} - V_{out})}{\frac{m_{P2}kT}{q}}\right) = A_{N1}.exp\left(\frac{(V_{dd} - V_{in}) + \eta_{N1}(V_{dd} - V_{out})}{\frac{m_{N1}kT}{q}}\right) \tag{4}$$

Hence,

$$\frac{A_{P2}}{A_{N1}} = \frac{exp\left(\frac{(V_{dd}-V_{in})+\eta_{P2}(V_{dd}-V_{out})}{\frac{m_{P2}kT}{q}}\right)}{exp\left(\frac{(V_{dd}-V_{in})+\eta_{N1}(V_{dd}-V_{out})}{\frac{m_{N1}kT}{q}}\right)} \tag{5}$$

Taking log on both sides

$$\ln\frac{A_{P2}}{A_{N1}} = \left(\frac{(V_{dd} - V_{in}) + \eta_{P2}(V_{dd} - V_{out})}{\frac{m_{P2}kT}{q}}\right) - \left(\frac{(V_{dd} - V_{in}) + \eta_{N1}(V_{dd} - V_{out})}{\frac{m_{N1}kT}{q}}\right) \tag{6}$$

$$\frac{kT}{q}\ln\frac{A_{P2}}{A_{N1}} = \left(\frac{(V_{dd} - V_{in}) + \eta_{P2}(V_{dd} - V_{out})}{m_{P2}}\right) - \left(\frac{(V_{dd} - V_{in}) + \eta_{N1}(V_{dd} - V_{out})}{m_{N1}}\right) \tag{7}$$

Also, we have assumed that the switching threshold of transistors at input and output of left inverter is V_{Sthl}. Now it can be rewritten as,

$$V_X = \left(1 + \frac{m_{N1}(1+\eta_{P2})}{m_{P2}(1+\eta_{N1})}\right)V_{Sthl} - \left(\frac{m_{N1}(1+\eta_{P2})}{m_{P2}(1+\eta_{N1})}\right) V_{dd} - \left(\frac{kT}{q}\right)\left(\ln\frac{A_{P2}}{A_{N1}}\right)\left(\frac{m_{N1}}{(1+\eta_{N1})}\right) \tag{8}$$

Assuming that,

$$\left(\frac{kT}{q}\right)\left(\ln\frac{A_{P2}}{A_{N1}}\right)\left(\frac{m_{N1}}{(1+\eta_{N1})}\right) = \delta \tag{9}$$

From Eqs. 8 and 9,

$$V_X = \left(1 + \frac{m_{N1}(1+\eta_{P2})}{m_{P2}(1+\eta_{N1})}\right)V_{Sthl} - \left(\frac{m_{N1}(1+\eta_{P2})}{m_{P2}(1+\eta_{N1})}\right)V_{dd} - \delta \tag{10}$$

For the case, $m_{N1} = m_{P2}$ and $\eta_{P2} = \eta_{N1}$, then V_X can be rewritten as,

$$V_X = 2V_{Sthl} - V_{DD} - \delta \tag{11}$$

Further, node X, $I_{N1} + I_{N3} = I_{N2}$

$$A_{N1}.exp\left(\frac{(V_{in}-V_X)+\eta_{N1}(V_{out}-V_X)}{\frac{m_{N1}kT}{q}}\right) + A_{N3}.exp\left(\frac{(V_{out}-V_X)+\eta_{N3}(V_{dd}-V_X)}{\frac{m_{N3}kT}{q}}\right) = A_{N2}.exp\left(\frac{(V_{in})+\eta_{N2}(V_X)}{\frac{m_{N2}kT}{q}}\right) \quad (12)$$

For the case, $m_{N1}=m_{N2}=m_{N3}=m_N$ and $\eta_{N1}=\eta_{N2}=\eta_{N3}=\eta_N$, Eq. 12 becomes,

$$A_{N1}.exp\left(\frac{(V_{in}-V_X)+\eta_{N}(V_{out}-V_X)}{\frac{m_{N}kT}{q}}\right) + A_{N3}.exp\left(\frac{(V_{out}-V_X)+\eta_{N}(V_{dd}-V_X)}{\frac{m_{N}kT}{q}}\right) = A_{N2}.exp\left(\frac{(V_{in})+\eta_{N}(V_X)}{\frac{m_{N}kT}{q}}\right) \quad (13)$$

Since we have assumed that the switching threshold of transistors at input and output is V_{Sthr}, Eq. (13) becomes,

$$A_{N1}.exp\left(\frac{-V_{Sthr}+V_{dd}+\delta+\eta_N(-V_{Sthr}+V_{dd}+\delta)}{\frac{m_{N}kT}{q}}\right) + A_{N3}.exp\left(\frac{-V_{Sthr}+V_{dd}+\delta+\eta_N(-2V_{Sthr}+2V_{dd}+\delta)}{\frac{m_{N}kT}{q}}\right) = A_{N2}.exp\left(\frac{V_{Sthr}+\eta_N(2V_{Sthr}-V_{dd}-\delta)}{\frac{m_{N}kT}{q}}\right) \quad (14)$$

Numerical solution of Eq.14 can be obtained to find switching threshold voltage V_{Sthr}. Value of A_N for various transistors be contingent upon process conditions. During read operation, signal WL is kept on logic low and signals RWL and WLB are maintained at logic high as shown in Table 2. Subsequently, transistors P2, N3, N5, N6 and N8 remain switched off in case we assume bit ‘1’ and bit ‘0’ at node Q and node QB respectively as represented in Fig. 4(b). The complement bit ‘0’ is shown on right hand side inverter.

The read waveform and bit-lines status during read operation is represented in Fig. 5(a). The write operation in projected circuit is differential and no assist circuitry for write operation is required. Signal WL and RWL are kept at logic ‘high’ whereas WLB signal is kept logic ‘low’ during write operation. The major requirements for correct write operation are strong write access transistor and incapacitated feedback loop. WLB signal is kept low and at the same time gate voltage of P1 transistor is kept at logic high for weakening of feedback loop. Figure 5(b) presents

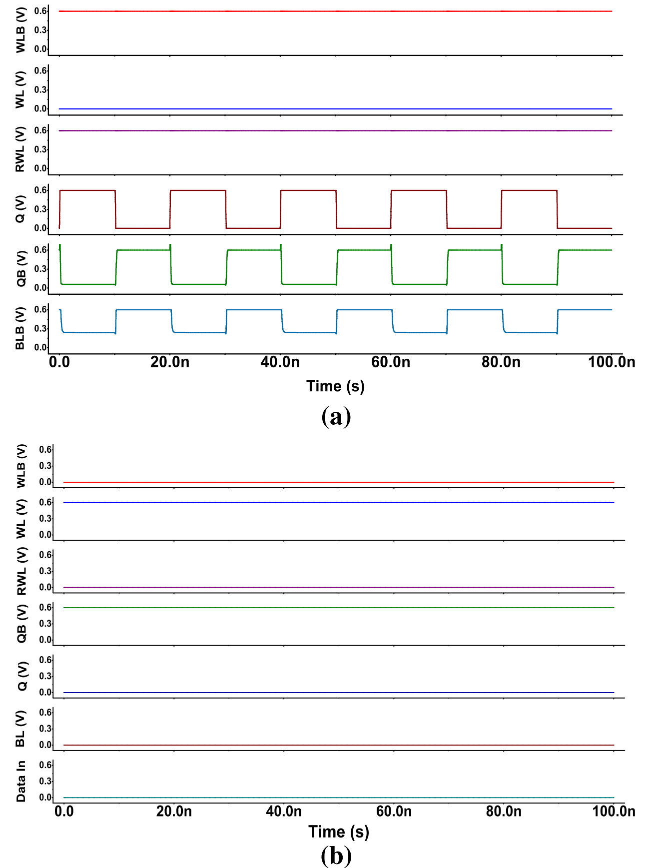


Fig. 5 **a** Read waveform. **b** Write waveform of Proposed ST12T SRAM cell

the cell signaling scheme to portray status of used signals during write operation. The feedback by strong inverter on right side of latch confirms generation of complement signal at QB node. This is can be noticed from Fig. 5(b) that as soon as WLB is activated, the weak one at node Q becomes strong one because at the same moment, supply voltage from P1 transistor is also activated. This also reduces write power during write operation.

Following transistor sizing strategies are considered for proposed ST12T SRAM cell topology.

(i) Similar to conv. 6T SRAM cell design, for lowering the pull-up ratiotransistors P1, P2 and P3 are maintained at minimal width
(ii) Transistors N2 and N9 are kept strongest as these are responsible for discharge of present voltage to ensure logic ‘low’ on observed node
(iii) Since NMOS is good pass of ‘0’, therefore, feedback transistors N3 and N7 are kept at lower width
(iv) Access transistors N4 and N8 are crucial to maintain conduction path between bit-lines and

accessed cell during write and read operations and thus, must be kept a little wider.

(v) Pull-down transistors N1, N5 and N6 are moderately strengthened as they are vital to retain effective resistance during standby mode.

3.3 Half select issue

SRAM bit cell suffers from soft error issue (sometimes referred to as single event upset problem) during its array implementation. Incorrect stored datum is the common interpretation of soft error issue. This may be due to cosmic rays or radiation of alpha particles from packaging materials. Subsequently, these alpha particle radiation leads to impact ionization of electrons at effected nodes. Furthermore, the scaling of transistors to nano-meter regime along with reduction in supply voltage make SRAM more susceptible to single event upset issue. Temperature and process variations may also enhance the vulnerability of static memory bit-cells to soft error issue [36]. Three possible case of occurrence of single event upset are shown in Fig. 6(a). In first case, single bit is affected by a particle strike. Though, hamming error correcting codes are enough to resolve this issue [37, 38]. But in second case, the particle hit effects more than one bit of the word. This event can-not be corrected easily by error correcting codes. To resolve this problem, adjacent bits of a word are not kept side by side. This scheme is called bit interleaving arrangement as shown in third case of Fig. 6(a). Solution of half select issue is crucial as it is a prerequisite for implementation of bit-interleaving scheme. This further allows pitch matching of layout between peripheral and proposed cell array. Generally, the major challenge while implementing static random-access memory circuits with single end read or single end write operation is ascribed to half select issue [39]. In this case, variation (low/high) of a particular signal for enable/disable of row/column to execute either read or write operation while implementing an array is required to be performed with utmost precision. This means that other bit-cells which are not intended to be selected should not be affected by variation of that signal. This challenge is widely understood as half-select issue. In present case, whenever a write or read operation is performed for a bit-cell in array, other bit-cells in those

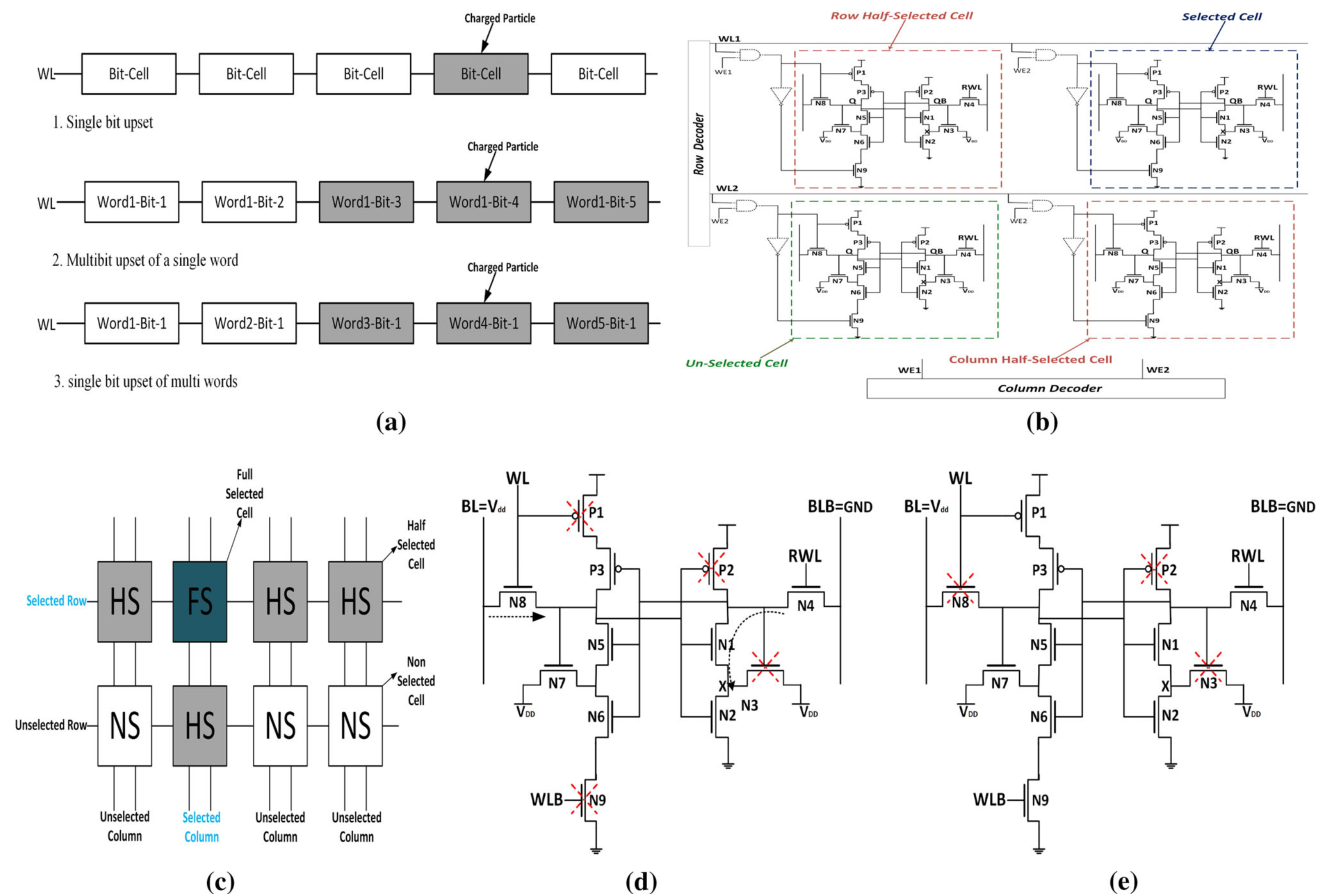


Fig. 6 **a** Different cases of soft errors. **b** Selected, Un-selected and Half-selected bit cells in 2×2 array. **c** Half-selected row and column representation in array. **d** Write '1' Operation in selected cell. **e** Write '1' Operation in Column Half-Selected cell

row/columns are required to remain in hold state for that duration.

The 2 × 2 array of proposed ST12T cell is depicted in Fig. 6(b). This array is sufficient to understand the presence of selected, row-half selected and column half selected cells. However, it is inevitable to mention here that, all the cells in selected cell's row and column will remain in half-select mode. This can be seen from Fig. 6(c). Therefore, the parameters of all row half-selected and Column half-selected SRAM cells will be adjusted in accordance with description given in this section. Generation of WL and RD signal is critical to eradicate row half-select issue during write and read operation. The signals must be generated in such a way that half selected and un-selected bit-cells should maintain standby state. Table 2 suggests that while executing read operation RWL and WLB signals must maintain logic '1' whereas WL should remain on logic '0'. Rest of the cells are required to have WLB at logic '1' and rest signals at logic '0' to attain standby mode. Similar pattern is required to be followed during write operation. The RWL and WL signals are required to be kept at logic '1' for successful differential write operation in the proposed cell. Also, for weak left inverter operation, the WLB is required to maintained at logic low as shown in Fig. 6(d). However, during column half selected write operation, WL signal gets switched off. consequently, P1 transistor also starts conducting. In addition to this, WLB signal gets logic high and changed status of these signals make SRAM cell unable to write the data present over bit line as shown in Fig. 6(e). Most of the cells which are considered for comparison excluding PPN10T [26] are susceptible to half select issue. However, it can be observed from Fig.6(b) that un-selected and half-selected cells in investigated 2×2 array of proposed ST12T cell remain in stand-by mode during read and write operation of selected cell.

4 Simulation results and discussion

4.1 Simulation set-up

To simulate proposed ST12T SRAM cell and various cells considered for comparison, cadence virtuoso tool and Generic Process Design Kit (GPDK) 45-nm process technology file is used. Monte-Carlo (MC) simulation with minimum 2000 samples have been carried out for analyzing the effect of process variations [29, 30, 40] on various simulated results of proposed topology. The cell is also analyzed for variation in temperature and on different process corners. For investigation of global and local parametric variability impact, variation in channel doping concentration, channel width (W),channel length (L),and oxide thickness (t_{ox}) [40] have been assumed. These parameters are presumed to have a normal Gaussian distribution with 3σ variations of 10%.In the following subsections, critical performance parameters of proposed ST12T SRAM cell have been compared with that of considered existing cells.

4.2 Stability

In this article, stability of SRAM cell has been investigated in terms of Static Noise Margin (SNM). Minimum DC noise that is sufficient to modify the present stored bit of SRAM cell is understood as static noise margin. This means that for achieving robustness, the SRAM topology must have higher SNM values for read, write and standby mode. The feedback and biasing effects are also examined while analyzing SNM of considered bit-cells. The SNM can be evaluated by observing the length of maximum possible square in any of lobes of symmetric butterfly curve. Though, in case of asymmetric butterfly curve the SNM is assessed by length of maximum possible square in smaller lobe [41].

4.2.1 Stand-by static noise margin

Dense SRAM is vital for realization high performance system-on-chip design with low power. SRAM is used in standby mode for preservation of data. Thus it is of utmost importance to have reliable data retention in hold state. Hold static noise margin (referred to as HSNM, hereafter), signify the maximum amount of DC noise voltage that a SRAM cell can tolerate without affecting the stored data during standby mode. Graphical butterfly VTC curve method [42] is applied to measure HSNM of considered SRAM cells. Figure 7(a) represents VTC butterfly curve plots of proposed ST12T SRAM cell and conv. 6T SRAM cell. Also, comparison of SNM during hold state of conv. 6T SRAM cell and proposed cell at diverse supply voltages is investigated in Fig. 7(b). This can be observed from Fig. 7(b) that there is narrow gap between HSNM of conv. 6T SRAM cell and projected ST12T SRAM cell. This may be due to similar cross coupled inverter structure of both SRAM cells. Though, the HSNM of proposed ST12T SRAM cell is better even at low voltages because of use of Schmitt trigger inverter structure that has better VTC characteristics. The asymmetric VTC curve is attributed to single end read structure. Also, the variation in temperature has small effect on hold SNM of a bit cell [15]. The aspect ratio of transistors in core latch needs to be carefully maintained for maximum resistance towards data flipping. Also, the stack transistor N9 in left inverter also adds up to data hold stability during stand-by mode. The MC simulation of HSNM for proposed ST12T cell and its comparison with conv. 6T SRAM cell and D2P11T cell is

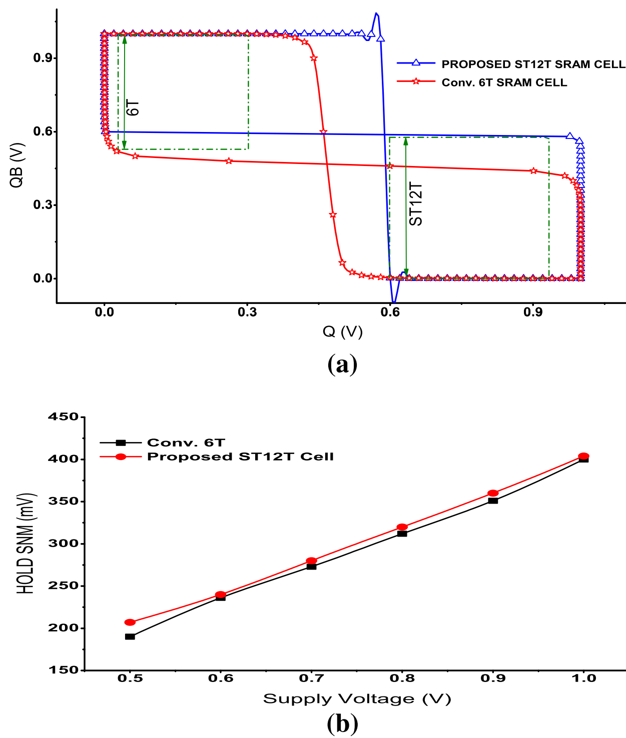


Fig. 7 **a** VTC of Proposed ST12T cell during standby Mode. **b** HSNM versus Supply Voltage

represented in Fig. 8. The mean value to Hold SNM for proposed topology is 1.69× better than that of D2ps11T cell. The mean hold margin of proposed topology is pretty close to conv. 6T SRAM cell even with stacked devices. Optimally sized core latch transistors may be attributed for this improvement.

4.2.2 Data retention voltage

One of the simplest methods for ultra-low power design is scaling of supply voltage. A few methodologies e.g. sleep transistor [25], stack transistor [28], buffers method [43] etc. are also utilized by researchers for reduction of leakage current during standby mode. Though the data retention voltage (DRV) may become the limiting parameter in implementing these strategies. The supply voltage must be above DRV for avoiding hold failures during data retention mode [9]. The butterfly curve method is used to observe DRV of proposed SRAM cell and attained results are compared with that of various considered cells. The HSNM curve is drawn to investigate DRV with minimum voltage for which area within curve declines to approximately 'zero' value [44] as shown in Fig. 9. Further, to investigate sensitivity of proposed cell towards DRV temperature is varied from − 20 to 100 °C. DRV of proposed ST12T cell is compared with that of considered cells with aforesaid temperature variation in Fig. 10(a). It can be observed from Fig. 10(a) that the DRV of the memory bit cell increases with decline in temperature below 27 °C. Though, similar shift of DRV is observable for all considered SRAM bit cells as shown in Fig. 10(a). This may be attributed to increase mobility of electrons with rise in temperature. Consequently, transistor become active early and may get incapacitated to remain stuck with present data. It can be observed that ST12T structure seems to lose its advantage in terms of DRV compared with other structures at 100-degree temperature. DRV is investigated in hold state in which core latch is involved. It can be noticed that during hold state in 6T SRAM cell core latch, 1-PMOS and 1-NMOS device remain active. However, in proposed cell core latch, 4-NMOS and 2-PMOS devices remain active during hold state. Electron mobility is approximately three times higher than that of hole mobility which helps core latch of proposed cell to hold the data during standby mode at lower voltage. The mobility of charge carriers in transistors decreases with rise in temperature. Due to this transistor become unable to hold the data for longer period of time [44]. This is the key reason of rise in DRV. However, with increase in temperature, electron mobility reduces more than that of hole mobility [45]. Since there are greater number of active NMOS transistors in proposed design during hold state whose mobility is degraded with rise in temperature, therefore, it lose the advantage of lower DRV at 100-degree temperature. This is worth noticing that DRV of proposed ST12T SRAM cell is minimum among

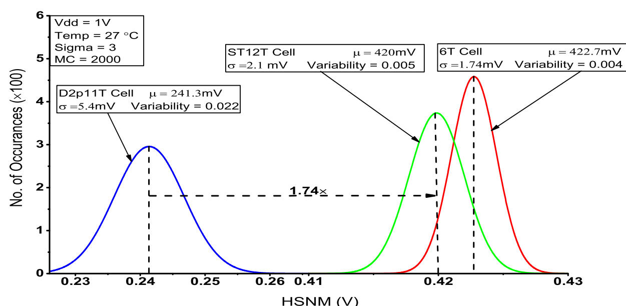


Fig. 8 Variability analysis for HSNM comparisons for Conv. 6T cell, D2p11T cell, and Proposed ST12T cell

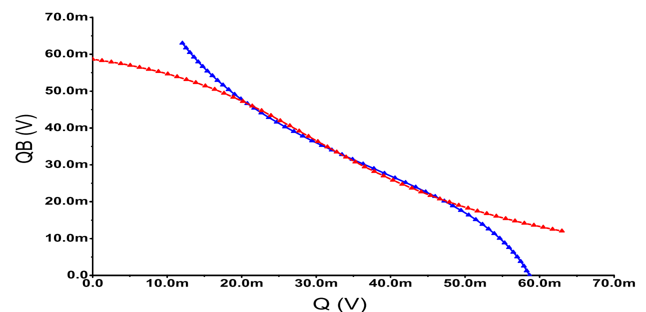


Fig. 9 VTC of Proposed ST12T cell for observing DRV [44]

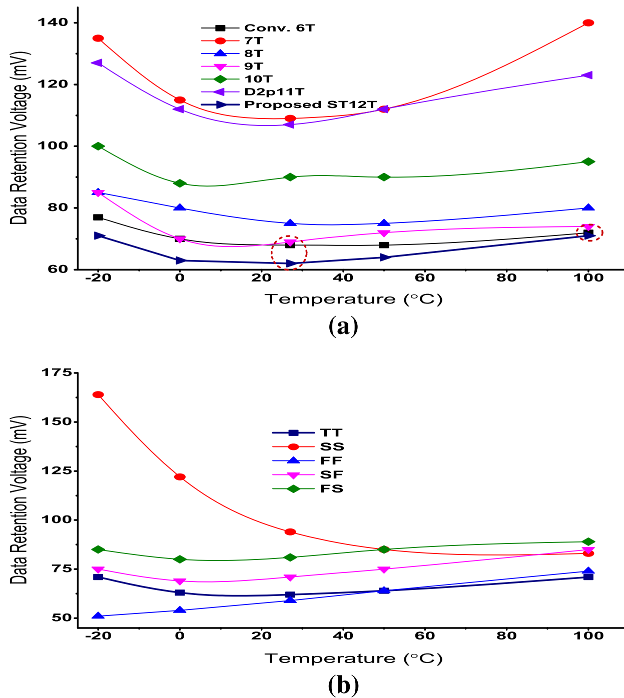


Fig. 10 DRV versus Temperature **a** For considered cells (**b**) at different process corner for Proposed ST12T cell

all considered cells. This may be owed to voltage developed at by feedback transistors in Schmitt trigger inverter design. Furthermore, the 7T SRAM cell shows the worst DRV i.e. nearly 1.76× more than proposed ST12T cell at all temperature values. Also, Process variation become dominant with scaling of supply voltage which impact SRAM cell reliability. Therefore, for reliable storage of data, it is very much necessary to analyze data retention voltage of SRAM cell in presence of process variations. Sensitivity and reliability of circuit under process corner variations [8] with variation in temperature has also been investigated. The DRV variation for proposed topology at each process corner with temperature ranging from − 20 to 100 °C is shown in Fig. 10(b). The maximum DRV at lower temperature is noticed in SNSP (slow NMOS, slow PMOS) process corner at − 20 to 100 °C.

4.2.3 Read stability

The voltage scaling intensifies the issue of read stability due to voltage dividing effect in conv. 6T cell. The read stability of SRAM cell is often dictated in terms of read static noise margin (RSNM). During execution of read operation SRAM cell is most prone to noise. Consequently, the voltage at node storing '0' slightly enhances and vice versa. The possible solution to expand the read margin includes read decoupled structure [19], read assist circuit [29] etc. Though, in proposed ST12T cell, Schmitt trigger inverter is utilized to improve read stability.Also, strengthening of driver transistor improves cell ratio. However, it is further affected by strength of read access transistor. Therefore, RSNM is more crucial than HSNM [46]. Figure 11(a) shows that butterfly curve used to determine RSNM. Length of maximum possible square in smaller lobe of butterfly curve gives estimate of read margin. In proposed circuit, single end read arrangement is used to evade ATS conflict. Though no 'read upset' issue is observed during bit-cell design. Figure 11(b) shows the comparison between read stability of the SRAM cells at each voltage at 27 °C.

NMOS transistor performance is also impacted by inverse narrow width effect (INWE). Driver transistors in left inverter are stacked in proposed topology which makes it slightly weaker than right side inverter. Subsequently, stronger pull-down transistor in right side inverter of proposed cell have higher threshold voltage (V_{th}) in comparison with that of Conv. 6T SRAM cell. The transistors with higher value of V_{th} are more rigid to change the state i.e. from 'on state' to 'off state' and vice versa. Due to usage of Schmitt trigger inverter improvement in read margin of proposed cell is attained as compared to conv. 6T SRAM cell. Also, the potential division at QB node gets enhanced with increase in supply voltage. This is owed to lower resistance offered by pull-down transistor. Hence, the proposed cell achieves 1.25× higher read margin than that of conv. 6T SRAM cell. Width of N1 transistor is the

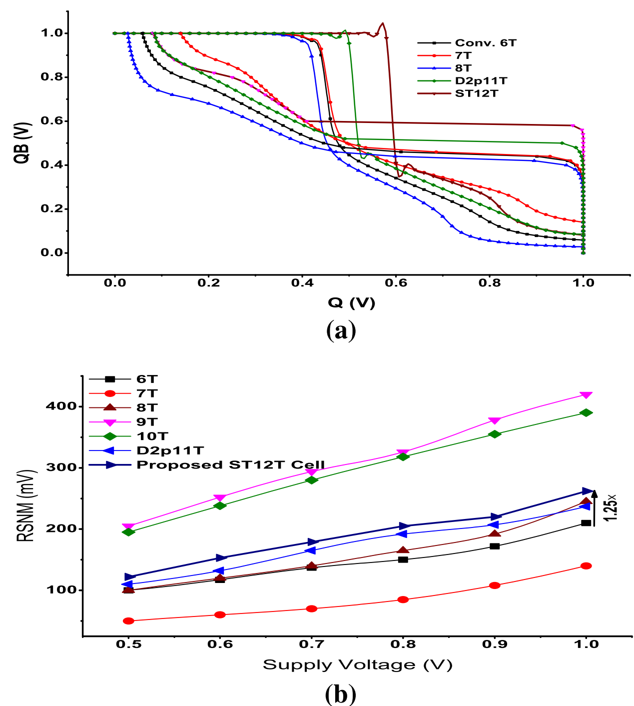


Fig. 11 **a** VTC of Conv. 6T, 7T, 8T, D2p11T and Proposed ST12T Cell. **b** RSNM versus Supply Voltage

limiting parameter for read margin in proposed topology. The RSNM of 9T SRAM cell is almost equivalent to its HSNM. This may be attributed to decoupled access transistor structure for read operation. However, trade-off for this improvement in topology is enhancement in power dissipation during read operation.

4.2.4 Write ability

The ability of SRAM topology to flip the stored value during write operation is often determined by write static noise margin (WSNM). The various methods to find WSNM include Bit-line voltage sweep [47, 48], word line sweep [49, 50], and analytical method [51]. For investigating WSNM in this work butterfly curve method [52]is used. In this method, storage node Q is swept from 0 to V_{dd} and the voltage at the storage node QB is monitored to attain read voltage transfer characteristic (RVTC) curve.

As the differential write method is used in this work, hence, Bit-lines are pre-charged to V_{dd} while keeping RD on logic '1' during RVTC plotting. For plotting WVTC, voltage is observed at storage node Q while sweeping QB from 0 to V_{dd}. The side length of the smallest square, that can be fitted between RVTC and WVTC curves is quantified as WSNM. For effective and successful write operation in proposed circuit storage node Q is required to be pulled below trip point of right-hand side inverter. Proposed cell must overcome sink current through stacked pull-down transistor N6 and transistor N9 and also flip the other inverter as well for attaining successful write operation.

Also, the write signal is deteriorated by potential division effect between pull down transistors and access transistors of left inverter. However, to eradicate this problem stack transistor N9 is switched off to weaken the driver transistor of left inverter. Once the left side inverter changes its state, the feedback will support other inverter to change the storage data. We have already calculated the switching voltage of right-hand side inverter by Eq. 14. The switching threshold of left inverter,V_{Sthl} can be calculated as given below, considering $V_{SN6} = V_{DN9} = V_y$, and also at node X1, $I_{N5} + I_{N7} = I_{N6} + I_{N9}$,

$$\begin{aligned} &A_{N5}.exp\left(\frac{(V_{in} - V_{X1}) + \eta_{N5}(V_{out} - V_{X1})}{\frac{m_{N5}kT}{q}}\right) \\ &\quad + A_{N7}.exp\left(\frac{(V_{out} - V_{X1}) + \eta_{N7}(V_{dd} - V_{X1})}{\frac{m_{N7}kT}{q}}\right) \\ &= A_{N6}.exp\left(\frac{(V_{in} - V_y) + \eta_{N6}(V_{X1} - V_y)}{\frac{m_{N6}kT}{q}}\right) \\ &\quad + A_{N9}.exp\left(\frac{(V_{dd}) + \eta_{N9}(V_y)}{\frac{m_{N9}kT}{q}}\right) \end{aligned} \tag{15}$$

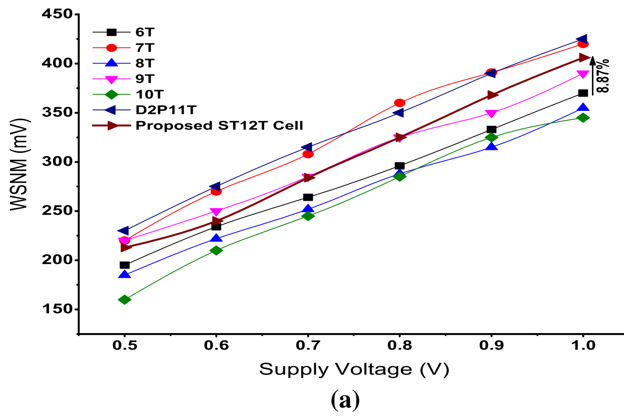
when WLB= V_{dd}, considering $V_X = V_{X1} = 2V_{Sthl} - V_{dd} - \delta$, and For the case, $m_{N5} = m_{N6} = m_{N7} = m_{N9} = m_N$ and $\eta_{N5} = \eta_{N6} = \eta_{N7} = \eta_{N9} = \eta_{N9}$, Eq. 15 simplifies to,

$$\begin{aligned} &A_{N5}.exp\left(\frac{-V_{Sthl} + V_{dd} + \delta + \eta_N(-V_{Sthl} + V_{dd} + \delta)}{\frac{m_N kT}{q}}\right) \\ &\quad + A_{N7}.exp\left(\frac{-V_{Sthl} + V_{dd} + \delta + \eta_N(-2V_{Sthl} + 2V_{dd} + \delta)}{\frac{m_N kT}{q}}\right) \\ &= A_{N6}.exp\left(\frac{-V_{Sthl} - V_y + \eta_N(2V_{Sthl} - V_{dd} - \delta - V_y)}{\frac{m_N kT}{q}}\right) \\ &\quad + A_{N9}.exp\left(\frac{V_{dd} + \eta_N(V_y)}{\frac{m_N kT}{q}}\right) \end{aligned} \tag{16}$$

where

$$V_y = \frac{2}{3}\left(\frac{kT}{q}\right)\left(\ln\frac{A_{N6}}{A_{N9}}\right)\left(\frac{m_N}{(2\eta_N)}\right) - \frac{2}{3}\left(\frac{V_{Sthl} + V_{dd}}{(2\eta_N)}\right) \tag{17}$$

Numerical solution of Eq. 16 can be obtained to find V_{Sthl}. Value of A_N for various transistors be dependent upon process conditions. Write static noise margin is measured at 406 mV for 1 V supply voltage for proposed ST12T cell that is 8.87% higher than that of conv. 6T SRAM cell. Figure 12(a) shows the comparison of WSNM of proposed ST12T cell with reported work at different supply voltages. Furthermore, write margin of proposed topology is observed as better than 6T, 8T,9T and 10T SRAM cells as portrayed in Fig. 12(a). Figure 12(b) shows MC transient response for 2000 samples run at 0.7 V supply voltage and 27 °C temperature for proposed ST12T SRAM circuitry. This is worth noticeable that out of 2000 samples, no write case has gone unsuccessful. The Q and QB node change their state as soon as WL signal gets high. The write margin of proposed cell can be further expanded by



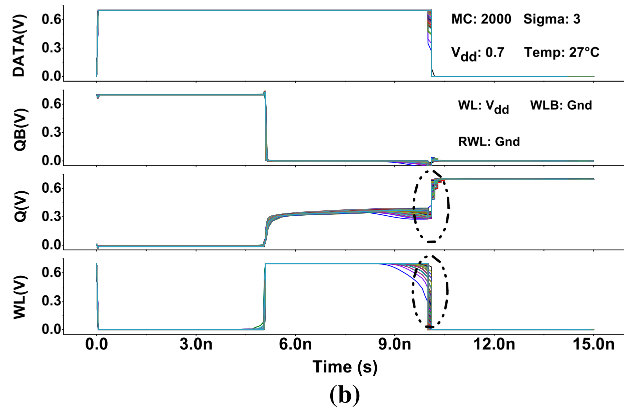
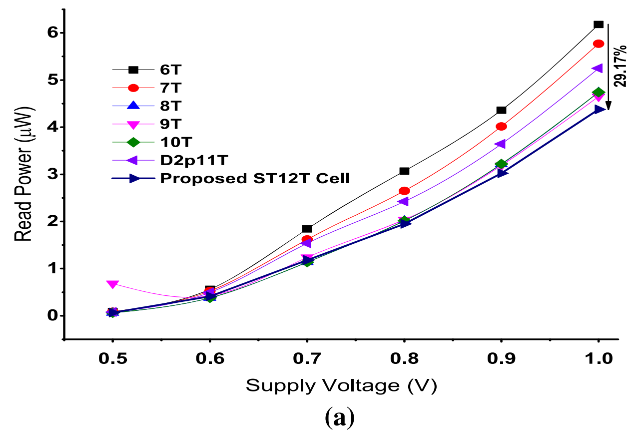


Fig. 12 **a** WSNM versus Supply Voltage. **b** MC simulation plot for Proposed ST12T cell for write operation



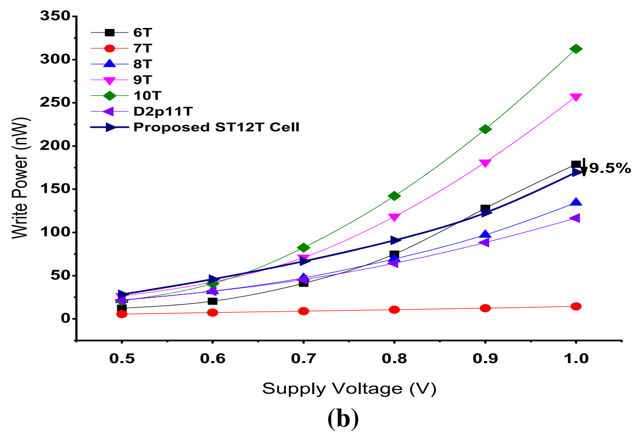


Fig. 13 **a** Read Power versus Supply Voltage. **b** Write Power versus Supply Voltage

enhancing width of N8 transistor. However, in such a case leakage power gets enhanced further and I_{on}/I_{off} ratio is declined as trade off.

4.3 Dynamic power dissipation

The key parameter in SRAM topology design is Power dissipation. Curtailing switching and swing voltage is critical for reduction in power dissipation [53]. The read power dissipation plot with variation is supply voltage for proposed ST12T SRAM cell and various considered cells for comparison is shown in Fig. 13(a). At 1V supply voltage the read power of proposed cell is significantly reduced by 29.17% when compared with that of conv. 6T SRAM cell. Single bit line read operation in proposed ST12T cell leads to reduction in power dissipation. It may be due to smaller power consumption for bit-line pre-charging before read operation. Also, maximum power at internal read node rises to V_{dd} only half of the time. Hence, reduction in swing voltage is observed. These factors lead to least power consumption of proposed ST12T SRAM cell among the all considered cells with variation in supply voltage from 0.5V to 1V. The maximum read power consumed by conv. 6T and 7T SRAM cells. This may be due to greater swing voltage at access transistor nodes. Figure 13(b) shows write power dissipation plot of different SRAM cells at variable supply voltages. It can be observed that increase in write power dissipation of proposed topology is less sharp than other considered cells with variation in supply voltage. At 1 V supply voltage the write power dissipation of proposed topology is 9.5% lesser than that of conv. 6T cell. It can be observed from Fig. 13(b) that, 7T SRAM cell consumes minimum write power. It is attributed to asymmetrical core latch and usage of dual NMOS transistors in place of access transistor in its topology. The single end write technique employed in this cell uses only one PMOS transistor in right hand side of core latch. This technique reduces the voltage swing at one node of SRAM cell significantly and therefore results in reduction of power dissipation during write operation. Further, the trade-off between write and read power dissipation can effortlessly be inferred from Fig. 13(a, b).

4.3.1 Process variation analysis for read power

The Monte-Carlo (MC) simulation of read power dissipation with 4000 samples at 3σ process variations is investigated to analyze impact of process variations. This variation is also contrasted with that of conv. 6T SRAM cell, 10T cell, and D2P11T cellat 0.8V supply voltage. The major observations of comparison are plotted in Fig. 14(a). This can be inferred from Fig. 14(a) that proposed ST12T cell dissipates 2.066μW mean read power which is 43.49%, 21.74% and 20.84% less than that of conventional 6T cell, 10T cell and D2P11T cell respectively. Variability analysis is comprehensive assessment of behavior of pattern and degree of disparity for a given quantity with respect to variation in given parameter. Fig. 14(a) shows variability (σ/μ) comparison of conv. 6T, 10T, D2p11T, and proposed ST12T cell at 0.8 V supply voltage. Further, variability for read power of proposed ST12T cell is observed with variation in supply voltage i.e. at 0.5 V, 0.8 V and 1 V as depicted in Fig. 14(b). This can be concluded from Fig. 14(b) that, the variability of proposed ST12T SRAM cell shrinks with upsurge in supply voltage. Also, we have extended variation analysis to process corners. MC simulation is performed for 4000 samples at 1V supply voltage at various process corners. Figure 15(a, b) depict MC simulation results of process corner variation for read power dissipation of proposed ST12T cell. The maximum read power dissipation was noticed for FNFP (Fast NMOS, Fast PMOS) process corner i.e. 6.93 µW which is followed by SNFP process corner (slow NMOS, Fast PMOS) at 6.77 µW. The expected gap between mean read power values at extreme process corners (FNFP, SNSP & FNSP, SNFP) can be observed from Fig. 15(a). This has been reported in literature [29] that at SNFP process corner NMOS transistor behaves weaker than PMOS transistor assuming the equivalent size of both transistors. This may be owed to superior current drive capability of PMOS transistor at lower threshold voltage. This reason can further be attributed for higher mean read power consumption observed at FNFP (fast NMOS, fast PMOS) corner i.e. 6.93µW. The least mean power dissipation is noted at SNSP (slow NMOS, slow PMOS) corner i.e. 2.56µW as represented in Fig. 15(b).

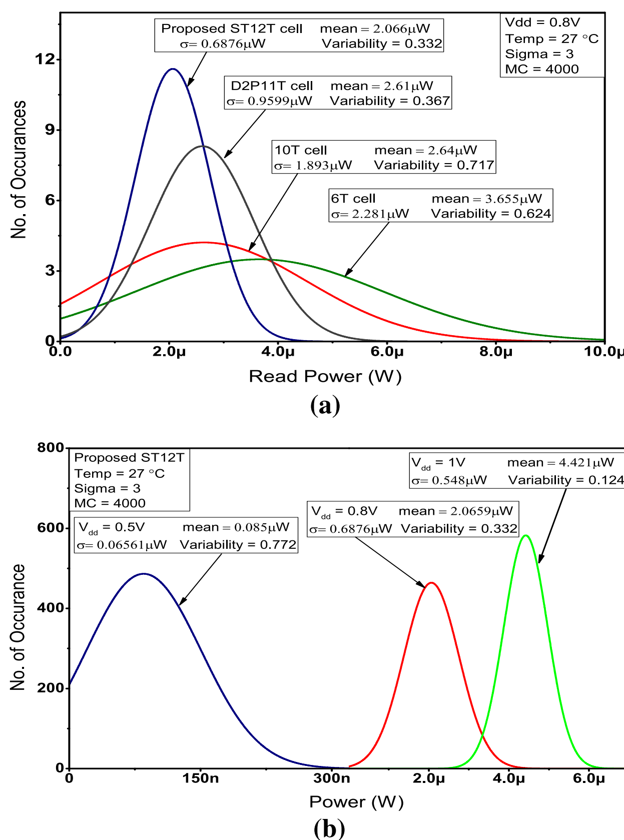


Fig. 14 **a** Variability investigation of mean read power for considered SRAM cells. **b** Mean read power analysis for Proposed ST12T cell at different supply Voltage (4000 samples)

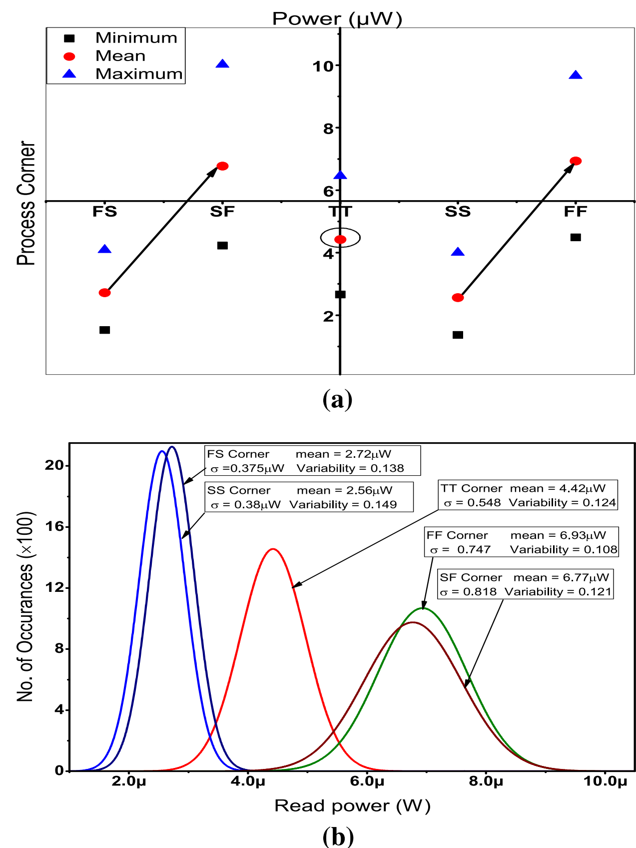


Fig. 15 **a** Min,Max and Mean Read Power dissipation and **b** Variability investigation of process corners for proposed ST12T circuit at 1 V supply voltage (4000 samples)

4.4 Leakage power

The power dissipation from the SRAM cell during idle condition is understood as leakage power. Current leaking transistors of proposed ST12T cell during stand-by mode are shown in Fig. 16(a). Transistors with crossed sign in Fig. 16(a) signify to be in 'off' state. These transistors contribute significantly to the leakage power of proposed topology. In addition to core latch of proposed cell transistors N3 and N7 are also powered by supply voltage. This further contributes to leakage power during idle mode. Also, combined effect of large width of access transistors and highly resistive pull-down path of left inverter contributes to significant enhancement of leakage power. A. Islam et al. [42] have revealed that the minimization of gate leakage is important to suppress the leakage power as portrayed in Fig.16(b). Though, in proposed cell, the minimization of static power is not that effective. This may be owed to domination of subthreshold leakage current (I_{sub}). In proposed topology, stacking effect in left inverter further hinders the suppression of leakage power. Besides, the large width of access transistor on right side leads to quadratic rise in leakage power (R $\times$ $I^2_{leakage}$) . The comparative plots for hold '0' and hold '1' power vs supply voltage is shown in Fig.17(a, b) respectively. The proposed ST12T cell dissipates smaller leakage power in contrast with considered 10T SRAM cell. Though, careful investigation of plots shows that hold '0' power of proposed cell upsurges sharply with increment in supply voltage when compared with that of hold '1' power. At 1V supply voltage, proposed ST12T topology dissipates 1.55× and 1.38× higher hold '0' and hold 1' leakage power respectively as compared to that of conv. 6T SRAM cell. Table 3 shows details of comparison of proposed ST12T cell with

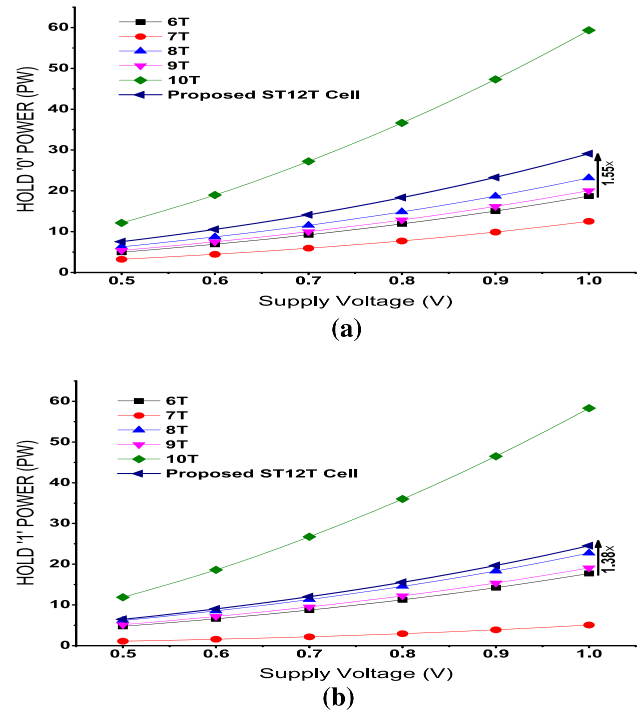
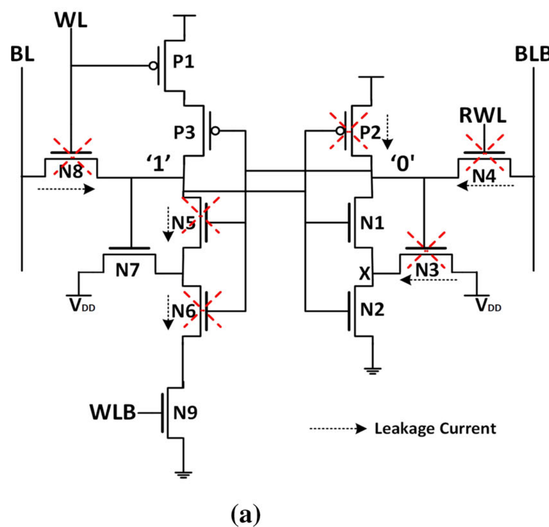


Fig. 17 **a** Hold '0' power of considered cells versus Supply Voltage. **b** Hold '1' power of considered cells Vs. Supply Voltage

conv. 6T SRAM cell for leakage power. The off-state transistors and transistors in core latch contribute significantly to the leakage power of proposed topology. In addition to core latch of proposed cell transistors N3 and N7 are also powered by voltage source equivalent to supply voltage. This further contributes to leakage power during idle mode. Also, combined effect of large width of access transistors and highly resistive pull-down path of left inverter contributes to significant enhancement of leakage



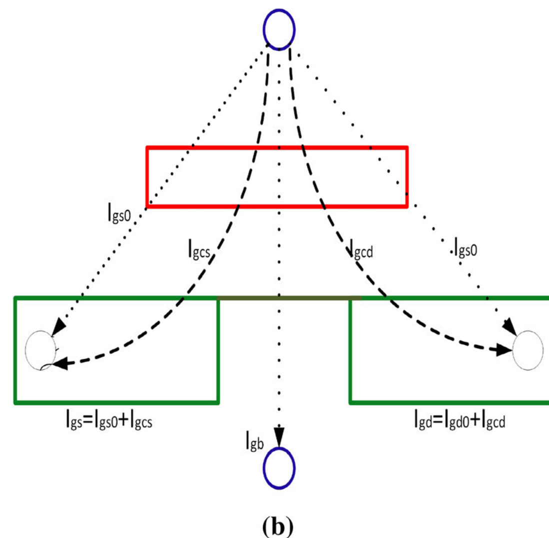


Fig. 16 **a** Proposed ST12T circuit during hold '1' mode. **b** Gate leakage current components in a short-channel device (Adopted from [42])

Table 3 leakage power comparison of proposed ST12T cell and Conv. 6T SRAM

Parameter	Conv. 6T SRAM cell	Proposed ST12T cell	Change
Total Number of transistors in the cell	6	12	2×
Total Number of transistors in core latch	4	10	2.5×
Total Number of transistors active during hold state	2	6	3×
Supply voltage(V)	**Leakage power (PW)**	**Leakage power (PW)**	
0.5	4.984	7.528	1.5×
0.6	6.932	10.5469	1.5×
0.7	9.227	14.13	1.5×
0.8	11.912	18.3506	1.5×
0.9	15.0505	23.2752	1.5×
1	18.735	29.1	1.5×

power. In proposed cell, the minimization of static power is not that effective. This may be owed to domination of sub-threshold leakage current, I_{sub}. In proposed topology, stacking effect in left inverter further hinders the suppression of leakage power. It can be noticed from Table 3 that, although there are 3× more transistors are there in core latch which are active during hold state, yet the power dissipation rises to 1.5× only. This may be attributed to adjustment of aspect ratios to minimize the leakage to best possible level and getting maximum possible improvements. In comparison to conv. 6T SRAM cell, proposed ST12T cell improves in terms of read power (1.57×), read current (1.04×), RSNM (1.37×), WSNM(1.10×), DRV(1.11×), Read access time (1.46×), write access time(2.15×) and power delay product of read(3.19×) and write (1.78×). However, it trades off in terms of leakage power (1.5×).

4.5 Cell current

Cell current (hereafter referred to as I_{on}) is another key parameter of static random-access memory cell design.In proposed ST12T topology cell current is observed during read operation as numeric addition of drain current of N4 transistor (I_{DN4}) and source current of N1 transistor (I_{SN1}). I_{on}, also known as read current, is significantly affected by sizing constraints of transistors. For reliable and faster read operation, large cell current is important. The cell current strength of considered SRAM cells during read operation is compared in Fig. 18(a). Read current of projected ST12T topology is improved by 1.44% when compared with that of conv. 6T SRAM cell. Although read current in proposed cell is improved by 1.44%, yet, this improvement is less than expected due to following reasons. Two transistors are connected in series in ST-structure, which increases the effective pull-down width of transistor that should improve

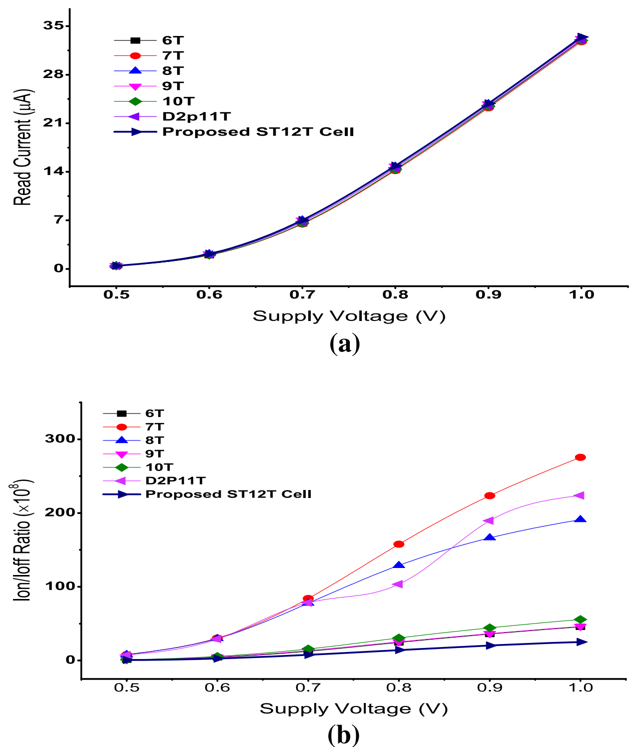


Fig. 18 **a** Read current versus Supply voltage. **b** I_{on}/I_{off} ratio versus Supply Voltage

the read current. However, this also increases the resistance due to stacking of two transistors (resistance in series). In case, the width of transistors is further increased, to further improve the read current, this also increases the leakage current, which is highly undesirable. Additionally, this can be noted that with scaling of supply voltage, read current for all considered cells declines in approximately linear fashion. During the execution of read operation of a particular cell other cells in that row/column of array are required to remain in idle mode. Though the bit-line

leakage current (hereafter referred to as I_{off}) incessantly flows through the idle transistors during that period. The contributing devices for leakage current are shown in Fig.16(a). Combined leakage from all the cells in same column may lead to false read [43]. To investigate I_{off}, voltage levels of RD and WR are lowered to logic '0'. I_{on}/I_{off} ratio dictates the number of SRAM bit-cells that can be connected with a bit-line [54]. The variation of I_{on}/I_{off} ratio with supply voltage is plotted on logarithmic scale in Fig. 18(b). Since read current enhances with increase in supply voltage, therefore, I_{on}/I_{off} ratio also follows the same pattern. Less I_{on}/I_{off} ratio for proposed topology is attributed to higher I_{off} values.

4.5.1 Process variation analysis

The Monte-Carlo (MC) simulation of cell current with 4000 samples at 3σ process variations is investigated in this section. The variability results are compared with that of conv. 6T SRAM cell. Efficiency of projected topology is noticeable in weak inversion region. The simulations are performed with 4000 samples each at 27 °C temperature and 0.5V supply voltage. Figure 19(a) shows that projected topology is observed with lower variability and 18.68% higher mean cell current as compared to conv. 6T SRAM cell. Figure 19(b) depicts the MC simulation results for investigating variability of proposed ST12T SRAM cell at different supply voltages i.e. 0.5V,0.8V, and 1V. It can also be noticed from Fig. 19(b) that variability of read current increases with scaling of supply voltage. Additionally, mean read current, standard deviation and variability analysis of cell current at different process corners is shown in Fig. 20(a). This is thought provoking for researchers that although the cell current maximizes at FNFP (Fast NMOS, FAST PMOS) corner, the variability is least in this process corner. Besides, mean values of I_{on}/I_{off} ratio and variability for proposed topology with different bit voltages have been investigated and shown in Fig. 20(b).

4.6 Read/write access time

Access time is the major concern that dictates the performance of topologies while implementing low power strategies. In this section authors have explored read access time and write access time (T_{wa}) of the proposed circuit in comparison with considered topologies. Read delay or read

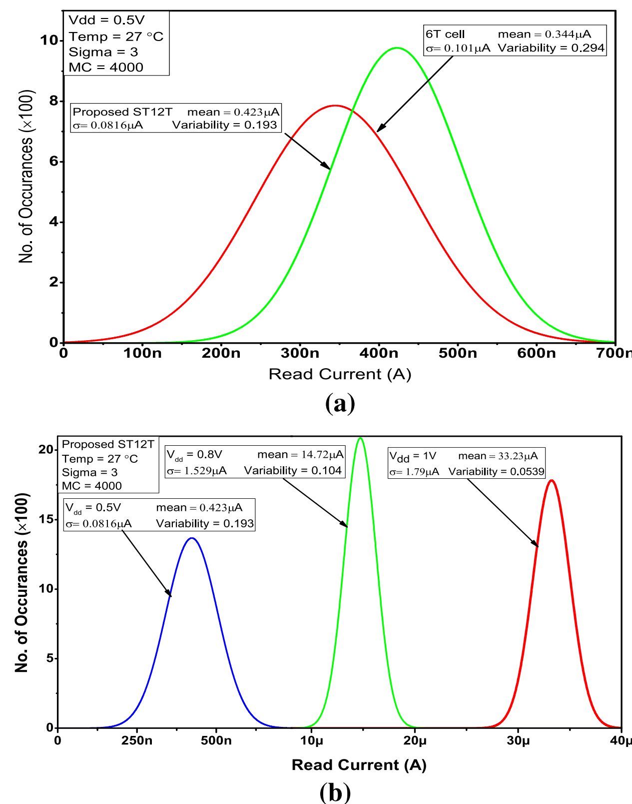


Fig. 19 Variability comparison of **a** Read current for Proposed ST12T cell with conv. 6T SRAM cell. **b** Read current for Proposed ST12T cell at different supply voltages

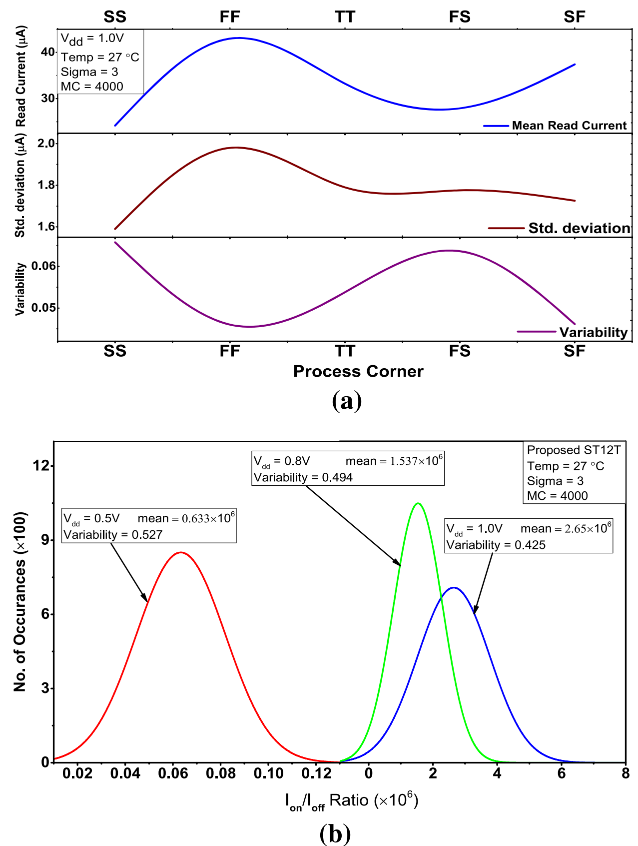


Fig. 20 **a** Read current variability at 1V for process corners and **b** variability comparison for I_{on}/I_{off} ratio at different supply voltages (4000 samples)

access time (T_{ra}) for a single ended bit-cell is the time elapsed while discharging bit line to a distinguishable gap from its initial pre-charge level after activation of read word line signal. Whereas, for differential SRAM cells, read access time is the time elapsed in discharging one of the bit-lines to a distinguishable gap from voltage level of other bit line after activation of read word line signal. With these methodologies, contrast of read access time for proposed ST12T cell with other considered cells is plotted in Fig. 21(a). The T_{ra} of proposed ST12T topology is calculated from the moment RD pin rise to $V_{dd}/2$ until the bit line is discharged to $V_{dd}/2$. The discharge via transistors N1, N2 and transistor N4 are accountable for delay of proposed bit cell. This can further be observed from Fig. 21(a) that, read delay of proposed ST12T topology at 1V supply voltage is minimum of all considered topologies at 1V supply voltage. Further, the proposed topology shows minimum write access time T_{wa} when compared with considered cells as the supply voltage is varied from 0.6V to 1V. At 1V supply voltage write access time is approximately 1.71× times lesser than that of conv. 6T SRAM cells as shown in Fig. 21(b). This is worthy to mention here that write methodology is differential in both cases i.e. proposed cell and conv. 6T SRAM cell. For all considered cells access time (both read and write) worsens with scaling of supply voltages. However, write back operation is tested for process corners also and it executed accurately.

4.7 Power delay product

Supply voltage reduction is widely accepted technique for reducing power dissipation. Though, rise in access is also observed with reduction in supply voltage. The novel proposed circuits usually claim of reduction in dissipated power with minimum effect on access time. Therefore, as a determining factor for potential enhancement for a certain topology, power delay product is calculated [55]. Read power delay product is calculated by multiplying read power and read access time for a particular supply voltage and similar pattern is followed for write power delay product. Figure 22(a) displays read power delay product (RPDP) plot for considered topologies to compare at different supply voltages. This can be observed from Fig. 22(a) that read power delay product of proposed ST12T cell is minimum at 1V supply voltage when compared with all considered cells. Furthermore, read power delay product for proposed SRAM cell is approximately

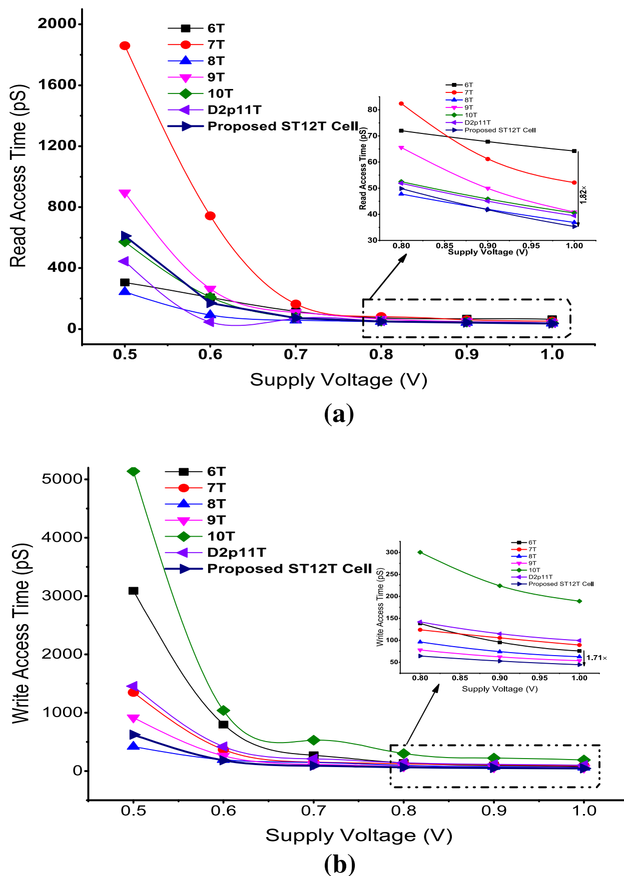


Fig. 21 **a** Read access time of considered cells versus Supply voltage. **b** Write access time of considered cells vs Supply Voltage

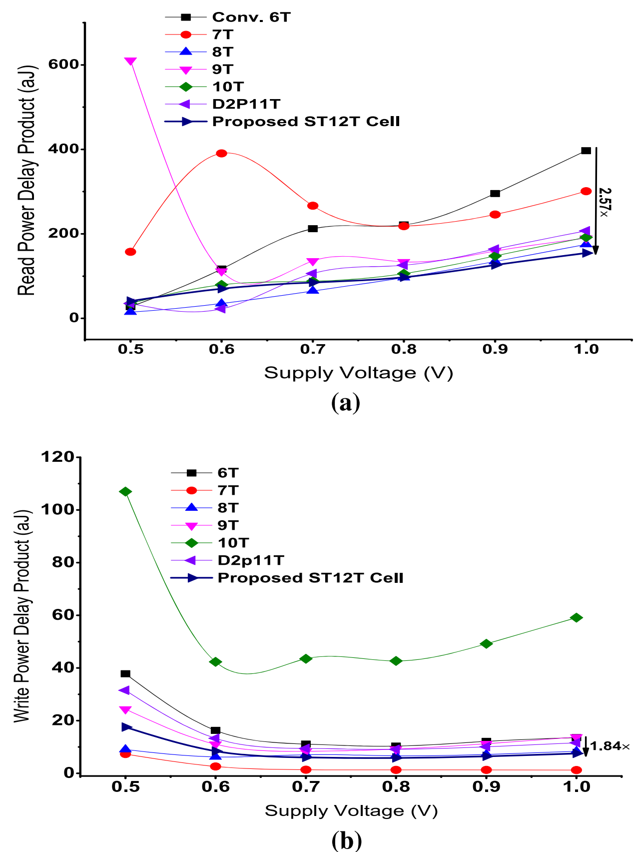


Fig. 22 **a** RPDP versus Supply voltage. **b** WPDP versus Supply voltage

2.57× less than that of conv. 6T cell. This improvement may be attributed to declined bit line capacitance on single ended read bit-line. Beyond, Fig. 22(b) shows write power delay product (WPDP) comparison of all considered cells. WPDP of proposed circuit is 1.8× less when compared with that of conv. 6T cell at 1V supply voltage. It is worthy to mention here that at this point the WPDP of proposed ST12T topology is minimum of all considered cells except 7T SRAM cell. Minimum value of WPDP of 7T SRAM cell may be attributed to minimal write power dissipation. It is interesting to note here that 7T SRAM cell dissipates 11.79× times less write power when compared to proposed topology. However, the WPDP of 7T SRAM cell is 5.86× times less when compared with proposed topology.

4.8 Area considerations

Fast differential sensing and simplified layout implementation are two basic advantages that have made conv. 6T SRAM cell an industry standard. Aspect ratio of devices must be considered essentially while achieving various performance factors such as leakage power, read/write power dissipation, stability and access time parameters up to their noteworthy level. We have already discussed the considerations for adjustment of width to length ratio of various transistors. Figure 23(a, b) shows the layout of proposed 12T cell and conv. 6T SRAM cell using 45 nm technology design rules. The cell areas are normalized to that of Conv. 6T SRAM cell. The proposed cell and 7T,8T,9T,10T and 11T SRAM cells show the area overhead of 2.96×, 1.41×, 1.44×, 2.13×, 2.57× and 2.44× as compared to conv. 6T SRAM cell. The area requirement in proposed cell is higher due to increased transistors number to get comparable performance. Layout has been tested primarily for DRS rules for 45 nm technology file and RC extraction is performed post checking LVS connections. For similar number of transistors, complexity of circuit is also an important measure for variation of area. Beyond, other design challenges while making layout of bit-cell include formulating a even layout, evading bends and avoiding misalignment etc. However, stricter micrometer rules usage may lead to further area reduction thereby realizing more compact cell.

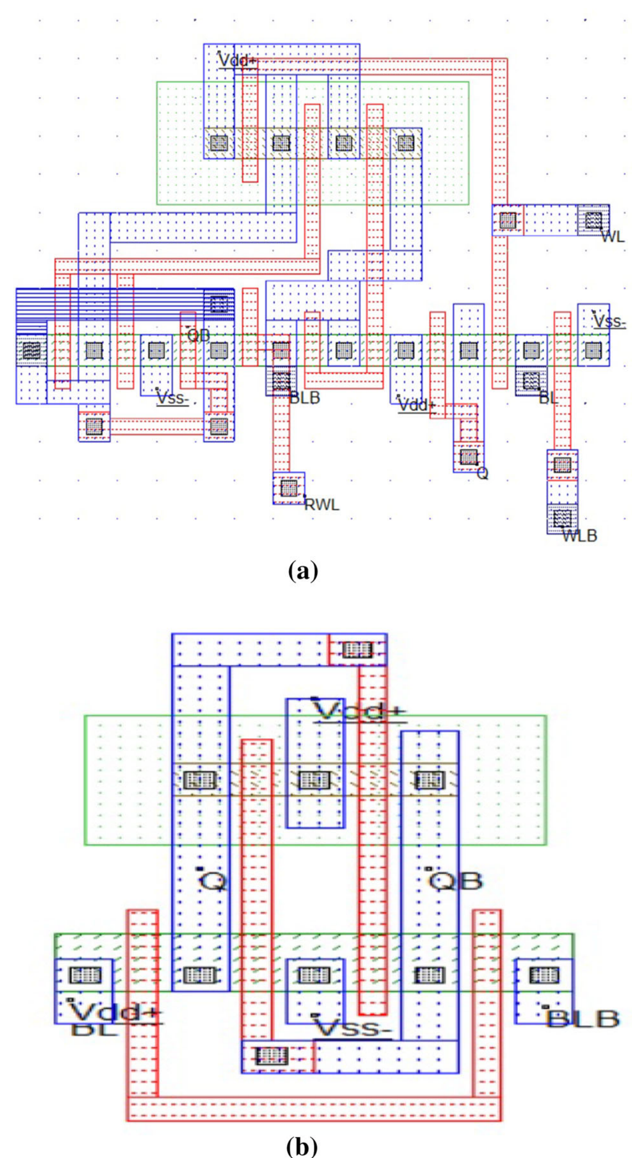


Fig. 23 Layout of **a** Proposed ST12T cell. **b** Conv. 6T SRAM cell

5 Conclusion

In this work, authors have proposed a reduced read power, minimum data retention voltage and variation-resistant Schmitt Trigger based 12-transistors static random -access memory bit-cell. Proposed ST12T cell resolves access transistor sizing issue by improving read static noise margin due to utilization of Schmitt trigger inverters in core latch. The stack transistor is added to ensure correct write operation. The proposed circuit also minimizes the impact of process variations and scaling of supply voltage on various parameters.

In addition to reduction of read power, other significant improvements of the proposed cell include enhanced read current, write noise margin, and read/write access time. The trade-off for these improvements of cell include reduced Ion/Ioff ratio and enhanced area overheads. The proposed bit-cell array is half select free and supports bit interleaving arrangement. The results of design parameters at 0.8V supply voltage are summarized in Table 4. Summarizing, this design presents a choice for low read power applications with low DRV and improved write access time in nanoscale technology generation.

Table 4 Comparison of various characteristics of considered SRAM designs at 0.8V supply voltage

	Parameters	Conv. 6T	7T	8T	9T	10T	D2p11T	ST12T
Power	Read power (μW)	3.07	2.649	2.017	2.04	2.019	2.422	**1.949**
	Write power (μW)	74.99	**10.6**	69.37	118.42	142.23	64.44	90.78
	Read current (μA)	14.32	14.18	14.8	14.82	14.328	14.573	**14.87**
	I_{on}/I_{off} ratio($\times 10^6$)	24.52	**157.73**	128.86	25.34	30.53	103.35	14.28
Stability	RSNM (mV)	150	85	165	**326**	318	192	205
	WSNM (mV)	296	**360**	288	325	285	350	325
	DRV(mV)	69	109	75	69	90	107	**62**
Speed	Read access time (pS)	72	82.39	**47.78**	65.57	52.5	51.88	49.33
	Write access time (pS)	138.4	123.9	96.22	77.94	300.3	141.8	**64.24**
PDP	Read PDP (aJ)	221.04	218.25	96.37	133.76	105.89	125.65	**96.16**
	Write PDP (aJ)	10.38	**1.31**	6.67	9.23	42.71	9.13	5.83

Bold values represent the best value of that parameter out of all compared designs

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