A single-ended low leakage and low voltage 10T SRAM cell with high yield

Nima Eslami[1] · Behzad Ebrahimi[1] · Erfan Shakouri[1] · Deniz Najafi[1]

Abstract
This paper presents a low leakage power 10T single-ended SRAM cell in the sub-threshold region that improves read, write, and hold stability. While at low voltages, the write-ability is increased by temporarily floating the data node, the read stability of the cell is maintained approximately as equal as the hold state by separating the data-storage node from the read bit line by using only a single transistor. According to Simulations using HSPICE software in 10 nm FinFET technology, the read stability of the proposed cell is approximately $4.8\times$ higher than the conventional 6T at 200 mV. Furthermore, the proposed cell is found to have the lowest static power dissipation, as it tends to be 4% lower than the standard six-transistor cell at this voltage. This study shows that the yield of the proposed cell is higher than 6σ in all operations, and supply voltages down to 200 mV.

Keywords 10T SRAM cell · FinFET · Stability · Low leakage power · Yield · Process variation

1 Introduction

Nowadays, as the demand for ultra-low leakage power applications such as implantable devices in the human body, wireless sensor networks, and other portable devices has increased, the need for managing power consumption in digital chips has become an important issue [1]. SRAM cells are one of the most important components of digital chips, which consume a large percentage of power [2]. Therefore, reducing the leakage power of these memories can significantly lower the leakage power consumption of an entire chip. One way to reduce the power consumption in a cell involves reducing the operating voltage of the cell near and under the threshold voltage. However, as the supply voltage of the cell decreases below the threshold voltage, the effects of variations in the manufacturing process increase, followed by short-channel effects in technologies below 100 nm [3]. Therefore, maintaining the stability of SRAM cells poses a significant challenge in the sub-threshold region [4]. As a result, new technologies

have been introduced to reduce the variations in the manufacturing process and diminish the short-channel effects of nanometer technologies. One of the promising candidates is the FinFET structure because of its better gate control over the channel [5]. Despite the benefits of this technology for memory cell design, conventional 6T cell (Fig. 1(a)) still not have a proper yield in the read and write operations at low supply voltages. This is because of conflicts in the read and write requirements of conventional 6T cells, leading to a trade-off in the sizing of the cells [6]. The width quantization property of FinFET aggravates this issue because of the constant height [7].

To overcome this issue, different SRAM cell structures have been proposed, such as conventional 8T SRAM cell (Fig. 1(b)). In this cell, the read operation is separated from the write operation by using two transistors. Considering this technique, the voltage division between the data node and the bitline does not occur, resulting in a read stability that is approximately equal to the hold stability. However, due to the existence of three bitlines in this cell, the cell overhead is increased. Furthermore, at low voltages, due to the positive feedback of the inverters, the cell suffers from a low write-ability [8]. To improve the write-ability, the inverters involved in the write operations are weakened to ease the operation. However, the ability to write "1" at low

✉ Behzad Ebrahimi
behzad.ebrahimi@srbiau.ac.ir

[1] Department of Electrical and Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran
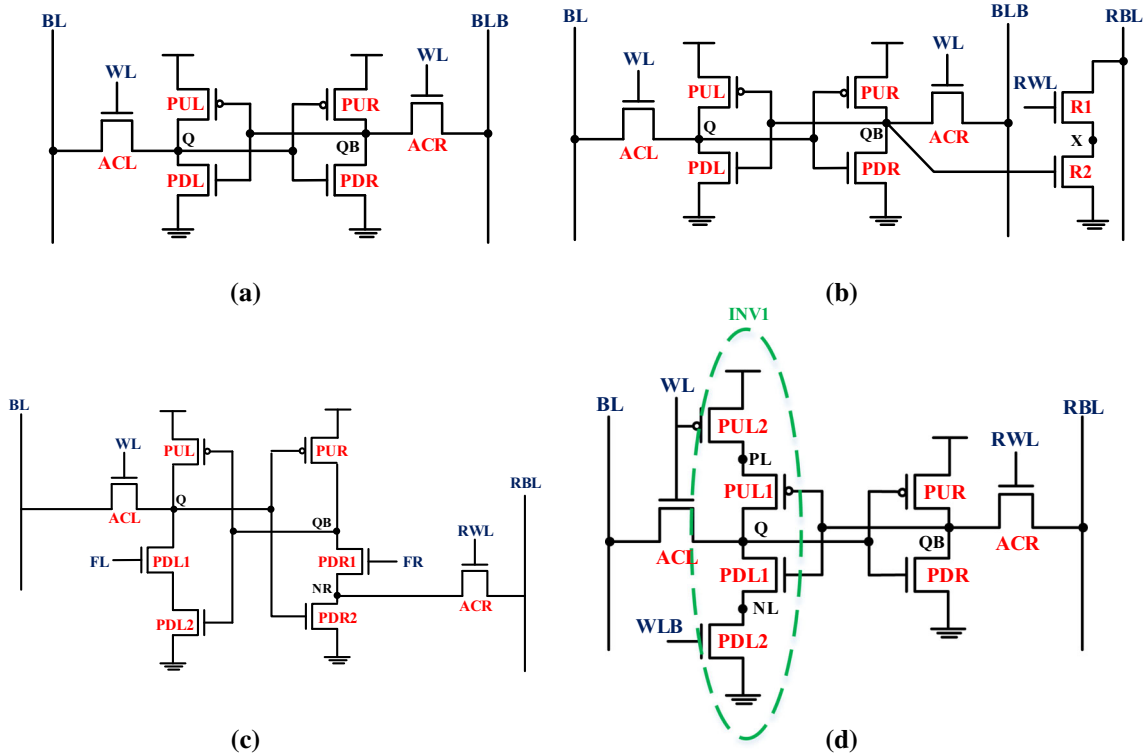
Fig. 1 Schematic of different SRAM cells. **a** 6T cell, **b** Conventional 8T cell [9], **c** 8T (SE-DFC) cell [23], **d** WRE8T cell [12]

supply voltages remains an important challenge in single-ended structures. The rest of this paper is organized as follows. Section 2 introduces the proposed structure and explains its operation in detail. Results and discussion are given in Sect. 3. Section 4 concludes the paper.

2 Proposed 10T SRAM cell structure

Figure 2 demonstrates the schematic of the proposed 10T SRAM cell. The cell is operational at low supply voltages down to the sub-threshold region. This cell consists of two back-to-back inverters, INVL (PDL1, PDL2, PUL1, and PUL2) and INVR (PDR1, PDR2, and PUR). We chose a tristate inverter with enable signals of WLB and WL for the INVL. On the other hand, the right inverter, INVR, has two series nMOS transistors as pull-down. A transmission gate (ACL1 and ACL2) is used for the single-ended write operation and a pass transistor (RD) as an access transistor is used for read operation. The read bitline (RBL) and the word line (RWL) are the control signals for the read operation. On the other hand, the write bitline (BL) and the write word lines (WL and WLB) are for the write operation.
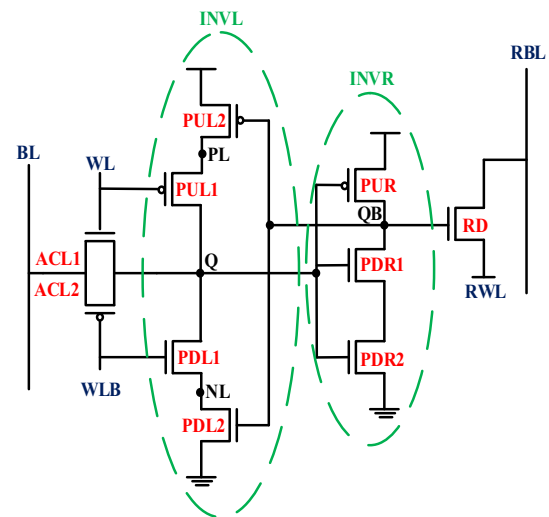

Fig. 2 Schematic of the proposed 10T SRAM cell

2.1 Hold state

In the hold state, data is stored in the cross-coupled inverters INVL and INVR. To have the maximum hold stability, the pull-up and pull-down strengths of the inverters should be equal. Due to the greater mobility of the n-type transistor than the p-type one, we exploit two series nMOS transistors in the pull-down of INVR to balance the pull-down and pull-up strengths. Besides, the stacked pull-

Table 1 Status of control signals in the proposed 10T cell

| Control signals	Hold	Read	Write "1"	Write "0"
BL	"1"	"1"	"1"	"0"
WL	"0"	"0"	"1"	"1"
WLB	"1"	"1"	"0"	"0"
RWL	"1"	"0"	"1"	"1"
RBL	"1"	Per-charge	"1"	"1"

down transistors are effective in lowering static power dissipation. Also, for the left inverter INVL, it has been investigated that by increasing the number of PUL1 fins to two, the strength of the pull-up network becomes close to the pull-down network leading to maximum hold stability. To increase the density, other transistors in the inverters are minimum-sized as one fin. The values of the control signals are also set as listed in Table 1.

2.2 Read operation

For the read operation, RWL is grounded and the operation is performed using the RD transistor. If QB = "1", RD turns on and discharges RBL and then a sense amplifier completes the read operation. If QB = "0", RBL remains pre-charged. As the RD transistor gate is connected to the QB node, no voltage disturbance occurs from the read bitline on the QB node. Hence, read stability is high, approximately equal to hold stability. However, as RWL is a row-based signal, the RWL driver must have the ability to sink currents from the read access transistors of the cells with QB = "1" in a row. The RWL driver is designed for the worst-case scenario, in which all cells in a row have QB = "1" [9]. Also, the readout circuitry may face the sneaking currents from unselected RWLs for the cells in the same column with QB = "1" as shown in Fig. 3. The sneaking current emerges as RBL discharges until the current becomes equal to the discharging current and RBL voltage saturates. To solve this issue, the proposed cell benefits from a sense amplifier that can discern a small voltage difference before sneaking currents emerge [10]. To increase the read performance, the size of the RD transistor is also selected two fins.

2.3 Write operation

The write operation of the proposed cell is done via a single bitline (BL). Since in single-ended structures, the n-type access transistors are weak in transferring "1", we exploit an extra p-type access transistor in parallel to the n-type access transistor similar to [11]. In this case, "1" is
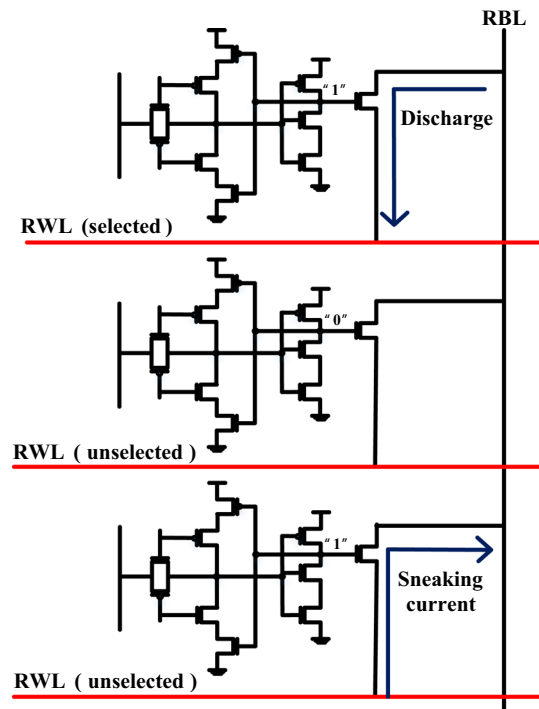
Fig. 3 Sneaking current flow in the proposed 10T SRAM

completely transmitted by the p-type access transistor to the data-storage node (Q). Further, we used the tristate inverter to facilitate the write operation, for the left inverter. During the write operation, WL and WLB control signals are "1" and "0", respectively.

Hence, PDL1 and PUL1 transistors are cut off, switching the INVL to the high impedance mode. Therefore, data can enter the cell easily augmenting the write performance and stability. A similar technique is used for WRE8T cell [12] shown in Fig. 1(d). For WRE8T, the left inverter becomes power gated during write easing the operation. As discussed later, our technique presents less leakage power. It should be noted that by asserting the row-based WL and WLB signals, the data of an unselected cell in the same selected row may be flipped. This is because for the half-selected cells, the write access transistors are ON and the left inverters are in the high impedance mode. To conquer this issue, an efficient write-back technique can be used [13]. In this technique, the data of the half-selected cells are first read by their read bitlines. Then the read data is put on the write bitlines of the half-selected cells by three n-type transistors and an inverter to restore the original data.

3 Simulation results and comparisons

In this section, metrics of the SRAMs such as stability, speed, power, and area are evaluated, and the results are analyzed. We compare the results of the proposed cell with the 6T and 8T cells and two similar single-ended 8T (SE-DFC) and WRE8T structures. HSPICE simulations were performed using 10 nm FinFET predictive technology model [14] to measure the performance parameters. To evaluate the timing of different operations and calculate the energy-delay product (EDP), all cells are examined in a 4 kb array (64 × 64 as shown in Fig. 4) and the interconnect capacitance is assumed 0.16 fF/μm [15]. In Fig. 4, we have shown the proposed cell array. Our results are supported by rigorous Monte-Carlo simulations performed for 5000 samples to analyze process variation effects.

Variations in the manufacturing process can be divided into global and local categories. Global variations for the channel length, fin width, and fin height are considered Gaussian with $3\sigma = 10\%$ of their nominal values and for the gate oxide thickness with $3\sigma = 5\%$ of its nominal value. Besides, local variations of the channel length and fin width are also considered Gaussian with $3\sigma = 5\%$ of the nominal value [16]. It has been shown that different stability parameters follow Gaussian distribution (Fig. 5). To compare the variability of the stability parameters, the mean of the corresponding parameter is divided by the standard deviation which is called yield. The amount of obtained yield represents the minimum variation needed to cause a failure. Today, Six-Sigma (6σ) yield or more is needed for big SRAM arrays [16].
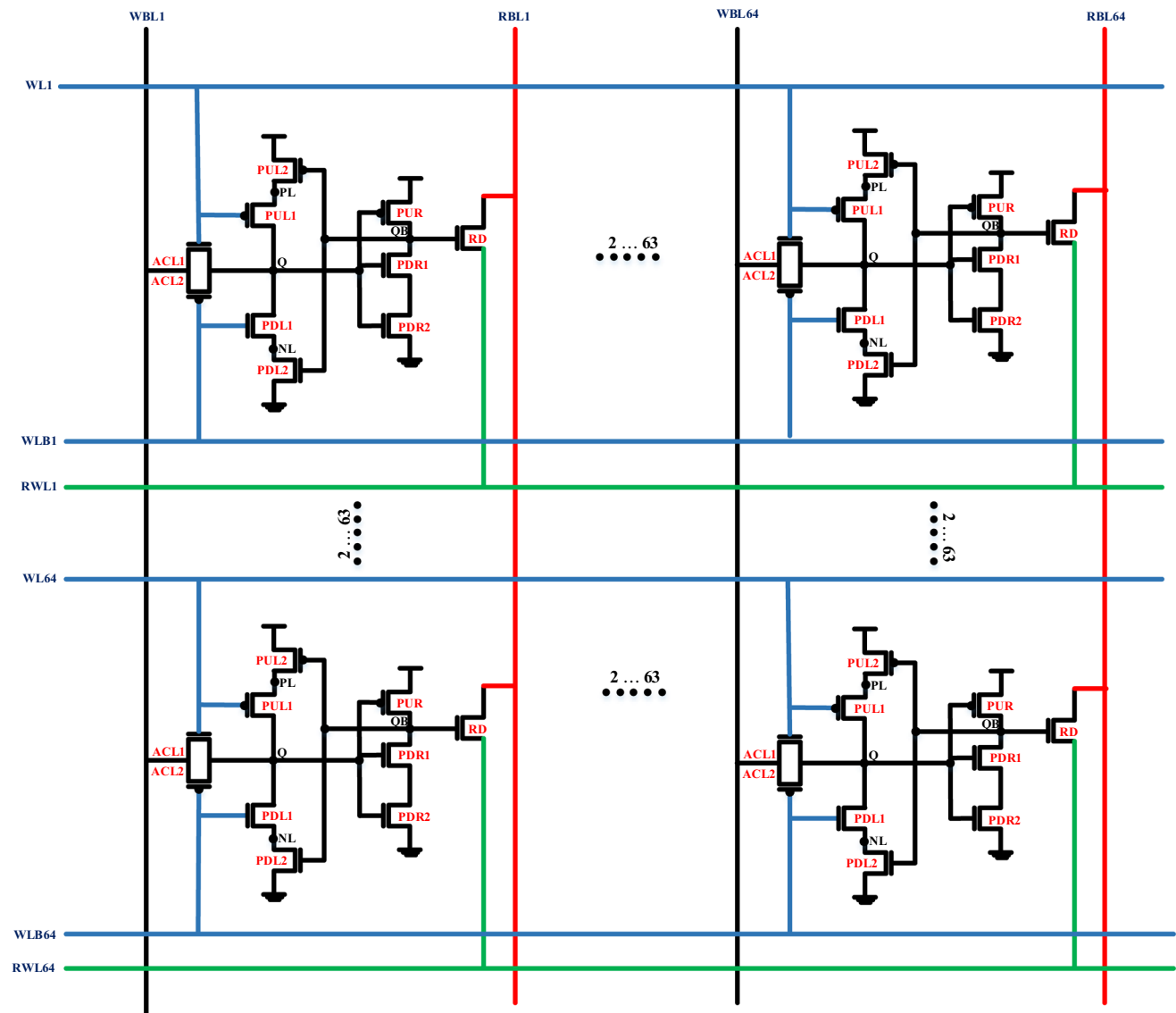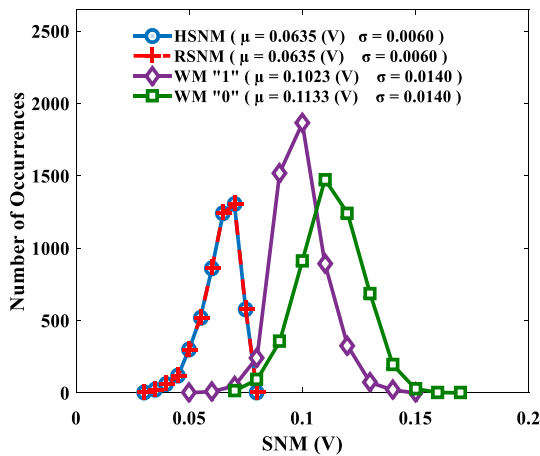

Fig. 4 Proposed 10T cell array

Fig. 5 HSNM, RSNM, WM "1" and WM "0" of proposed cell at a 200 mV supply voltage with 5000 samples of MC simulation

3.1 Hold stability

Hold stability is measured using the hold static noise margin (HSNM) metric, which is the length of the largest square encompassed in the butterfly curves in the hold state [17]. Figure 6 illustrates the hold butterfly curve of the proposed structure at 200 mV supply voltage. As shown in Fig. 7(a), HSNM of the proposed cell is slightly higher than all the investigated cells. Figure 7(b) shows the hold yield of the compared cells at different supply voltages. As displayed, the hold yield of this cell is lower than all other compared cells at a supply voltage of 600 mV (still higher than 20).

This may be attributed to the fact that the DIBL at high supply voltages is exacerbated by an increase in the drain-to-source voltage. Hence, the proposed cell is more sensitive to this phenomenon due to the use of two OFF access transistors (ACL1 and ACL2) with V_{ds} = VDD when
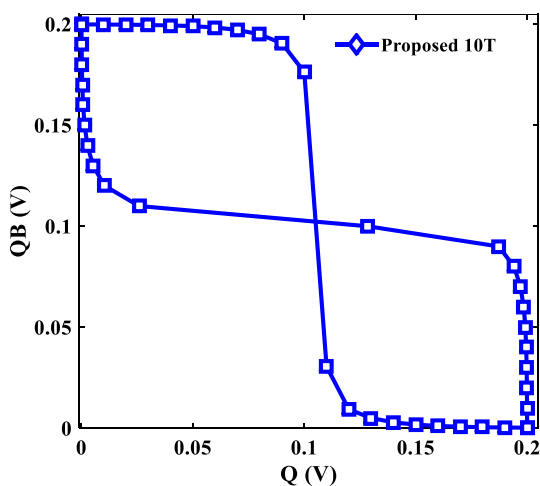

Fig. 6 Hold butterfly curves of the proposed cell at 200 mV supply voltage

Q = "0". However, by decreasing the supply voltage, the effect of DIBL is attenuated and the proposed cell shows good robustness against the process variability. For instance, at supply voltages below 300 mV, the proposed structure has the highest hold yield.

3.2 Read stability

Read SNM (RSNM) is the popular metric for read stability [18]. As shown in Fig. 8(a) the proposed cell, followed by the conventional 8T cell, has the highest RSNM among all the studied cells. In these cells, by decoupling the data-storage node from the read bitline, the voltage division between these two nodes will not occur. Hence the RSNM of the proposed cell and the conventional 8T cell is close to their HSNM. It should be noted that RSNM of the 8T (SE-DFC) cell has not been examined. Since for this cell, the PDL1 and PDR1 pull-down transistors are turned off during the read operation, no read butterfly curve is formed for this cell. As illustrated in Fig. 8(b), the read yields of the proposed cell and conventional 8T are higher than the other cells due to the higher nominal RSNM. According to Fig. 8(b), the yield of the proposed cell is approximately 5× higher than the WRE8T cell at 200 mV supply voltage. It should be noted that at this voltage, all the compared cells except the proposed cell and the conventional 8T cell, suffer from a read yield less than 6σ. It asserts that the other compared cells cannot have a robust read at sub-threshold voltages, except the proposed and the conventional 8T cells.

3.3 Write-ability

There are various methods to calculate the write margin. One of them is CWLM [19]. In this case, the desired data is first placed on the bitline, followed by sweeping the word line WL from the ground to the supply voltage. Meanwhile, when the Q voltage is equal to QB, the difference between the WL voltage and the supply voltage indicates the write margin. It can be seen from Fig. 9(a) that for write "1", the write margin of the proposed cell is higher than all the cells, including the WRE8T. This is attributed to the fact that in the proposed cell we exploit two write access transistors, which one of them is p-type passing "1" strongly. To facilitate the single-ended write further, the (PDL1 and PUL1) transistors also become off during write operation floating the Q node. This allows the strong write access transistors to easily write the data into the cell. Following the proposed cell, the WRE8T cell has the highest write margin. For write "0", the write margin of the proposed cell and WRE8T cell is approximately equal because the n-type write access transistor transmits "0" completely. Since the storage node of both mentioned cells
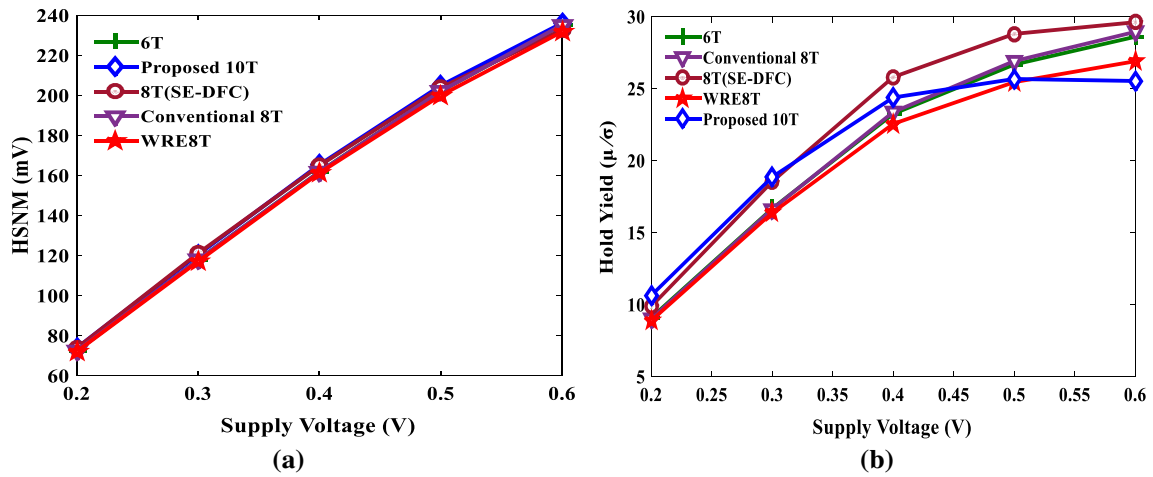
Fig. 7 **a** HSNM and, **b** hold yield of compared SRAM cells for different supply voltages
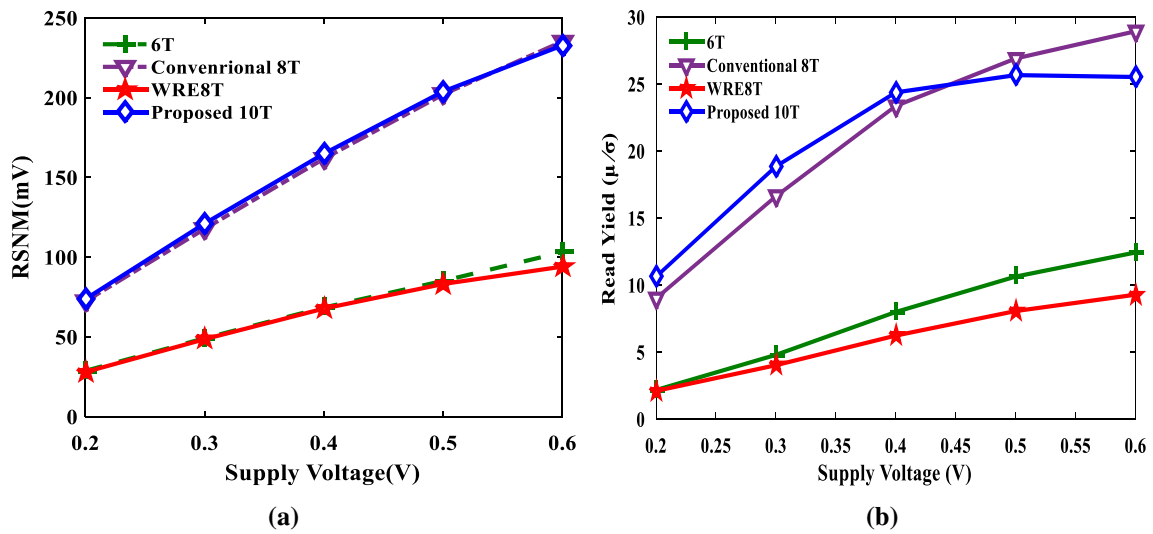

Fig. 8 **a** RSNM and, **b** read yield of compared SRAM cells for different supply voltages
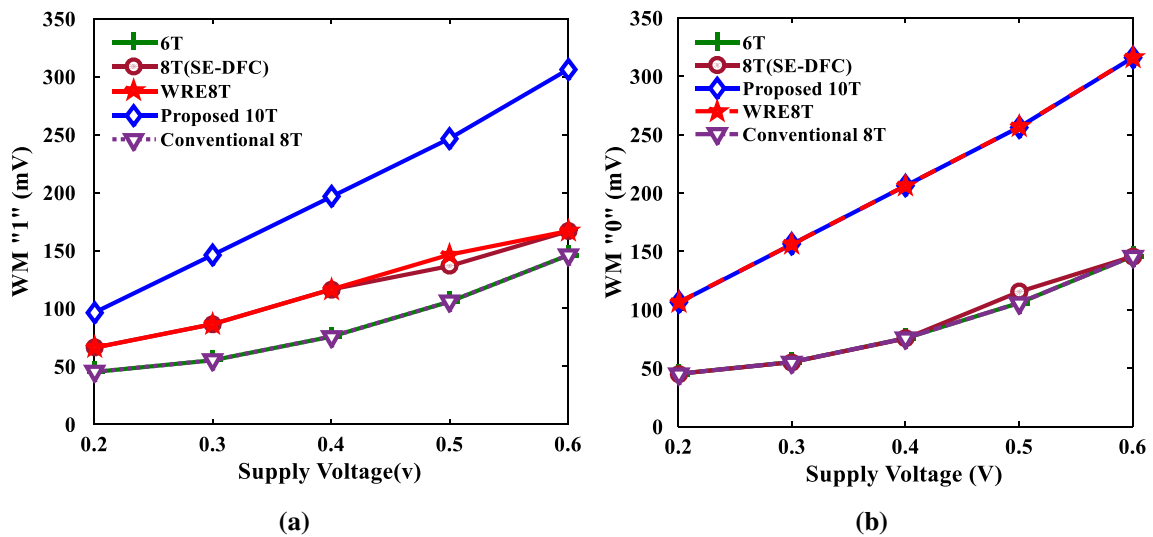

Fig. 9 Comparison of **a** WM "1" and, **b** WM "0" of compared cells for different supply voltages

is disconnected from supply and ground, these cells have the highest write "0" margin. Given that the write "1" margin of the proposed cell is higher than all the studied cells, the yield of the proposed cell for "write "1" is higher than all the compared cells. Also, the yield of write "0" operation is close to the WRE8T cell. It can be seen from Fig. 10 that for write "1" operation at a supply voltage below 300 mV, the yield of all investigated cells is below (6σ) except the proposed cell. Furthermore, for write "0", the yield is less than (6σ) among all of the cells except the WRE8T cell and the proposed cell. Therefore, the proposed cell is suitable for ultra-low voltage applications.

3.4 Read and write access times

Read time is defined as the time from when read word line reaches VDD/2 to when the voltage of read bitline reaches 90% of VDD as the used sense amplifier can sense 10% of VDD in this work [10]. For the proposed cell as the read access transistor RD is upsized, the read time is the least between the other compared cells for supply voltages below 400 mV as shown in Fig. 11. It should be noted during the read operation, the RWL control signal is grounded by the driver. However, for high supply voltages (upper than 400 mV), the driver cannot discharge RWL completely resulting in increased read time, which is still about equal to other structures.

Write time is defined as the time taken between VDD/2 of write word line and the time that voltages at the storage-nodes of the cell become equal. For writing "0" and "1" in the proposed cell, both the pull-up and pull-down transistors of the left inverter (PDL1 and PUL1) are turned off, making the write operation easy. Also, in the proposed cell, given the fact that two transistors of two different types (n
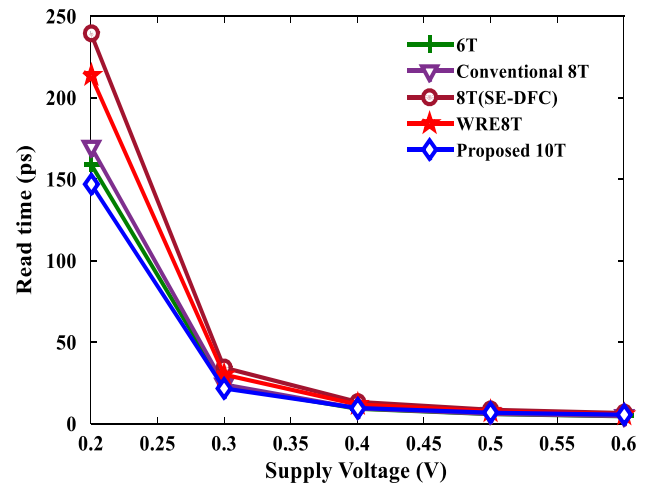

Fig. 11 Read time of compared SRAM cells for different supply voltages

and p) are used for write access, this operation is much faster than other single-ended cells where it is difficult to pass "1". However, the write operation is still slower than differential cells; because in differential cells, data is written from both sides of the cell, which speeds up the write operation. As shown in Fig. 12(a), for write "1", at 200 mV supply voltage, the speed of the proposed cell is 5.7x higher than the WRE8T cell. Moreover, as illustrated in Fig. 12(b), the write "0" time of the proposed cell is very close to the differential cells.

3.5 Read and write power

During read and write, dynamic power is consumed in SRAM arrays due to charging and discharging of long
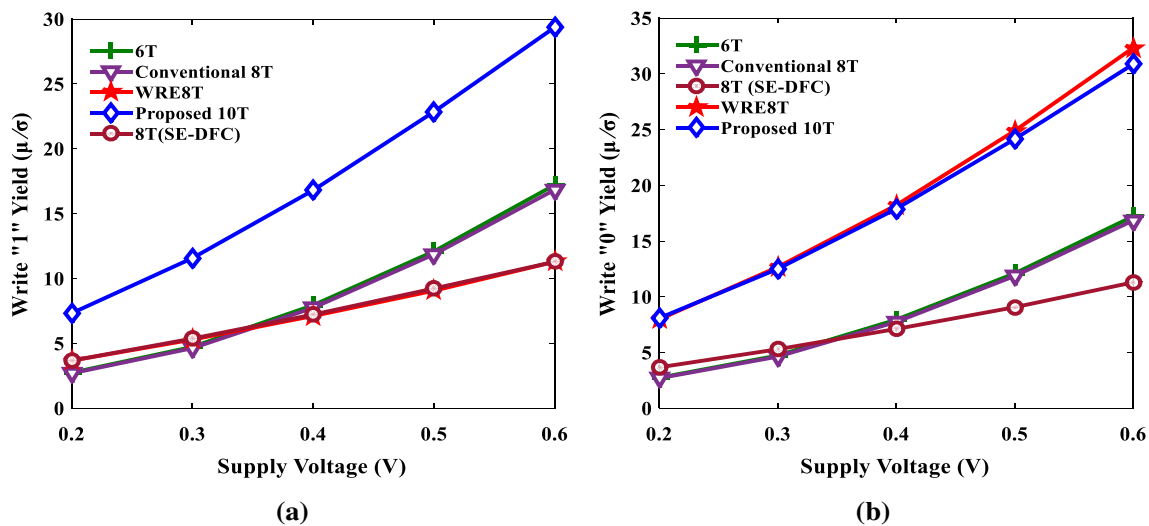

Fig. 10 **a** Write "1" yield and, **b** write "0" yield of compared SRAM cells for various supply voltages
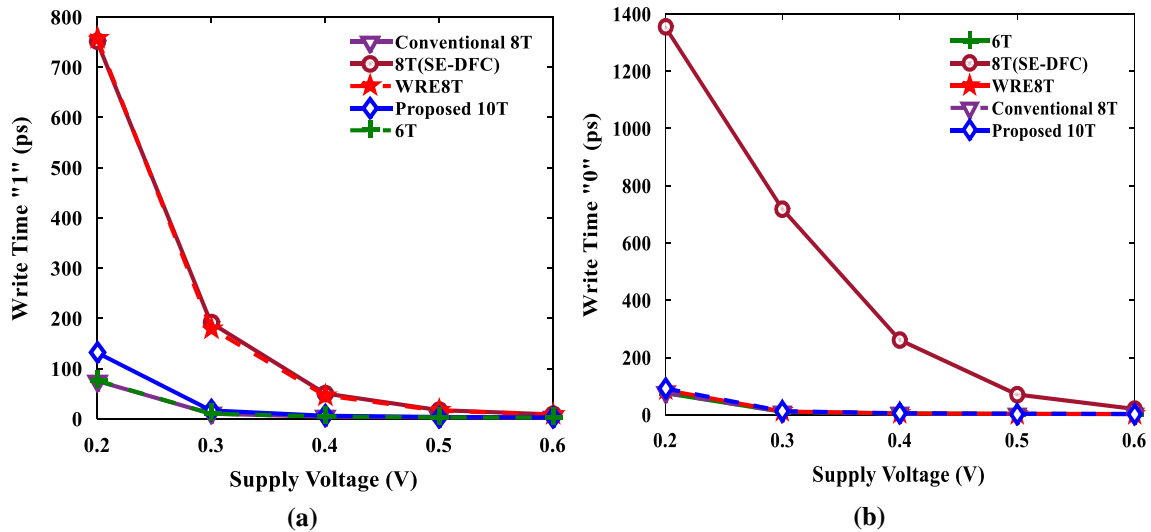
Fig. 12 **a** Write "1" time and, **b** write "0" time of compared SRAM cells for different supply voltages

bitline and word lines. Dynamic power consumption is formulated as

$$P_{Dynamic} = \propto CV_{DD}^2 f \qquad (1)$$

where $\propto$, C and f are activity factor, (bitline or word line) capacitance and frequency, respectively. As shown in Fig. 13. Read power consumption of the proposed structure and WRE8T with single-ended read is lower than other compared structures. This is attributed to the half activity factor of the bitline capacitance for the single-ended structures versus differential ones. Despite 8T (SE-DFC) is a single-ended structure, it has higher read power. This is due to the high word line capacitance and dynamic power because of the high height layout (see Table 2).

During "write" operation for single-ended structures like WRE8T and 8T (SE-DFC), the n-type access transistor is not capable to transfer '1' completely. Hence, the speed

Table 2 Area of different cells

Cell structures	Width (λ)	Height (λ)	Area (λ²)
6T	35	20	700
Conventional 8T	47	20	940
8T(SE-DFC)	38	36	1368
WRE8T	40	30	1200
Proposed 10T	38	30	1140

of writing '1' is low in these cells which leads to a reduction of frequency (*f*) during write '1'. According to Eq. (1), the power consumption of write '1' is low in these structures (Fig. 14(a)). In the proposed structure, both n-type and p-type access transistors are used for full transferability ('1' or '0'), meanwhile enhanced writing process and boosted write operation frequency are results that can be derived from this idea. According to Eq. (1), it increases write '1' and '0' power consumption as shown in Fig. 14.

3.6 Static power consumption

With technology scaling, static power consumption increases significantly due to the lower threshold voltages and severe short channel effects such as DIBL [20]. On the other hand, SRAM cells are mostly in the hold state consuming the static power consumption [21]. Using the tristate inverter INVL in the proposed cell (Fig. 2) leads to less subthreshold current than the INV1 in the WRE8T (Fig. 1(d)). Figure 15 depicts, the INV1 and INVL inverters used in the WRE8T cell and the proposed cell
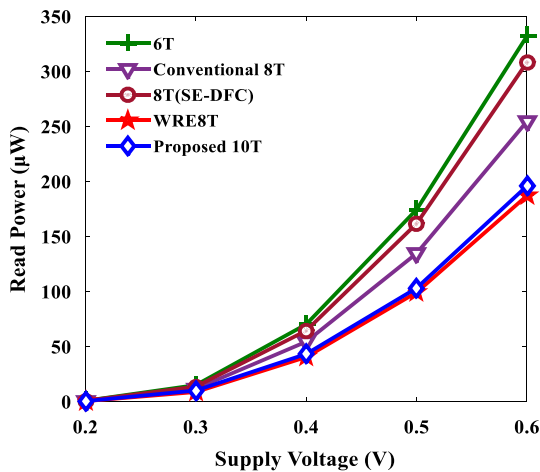

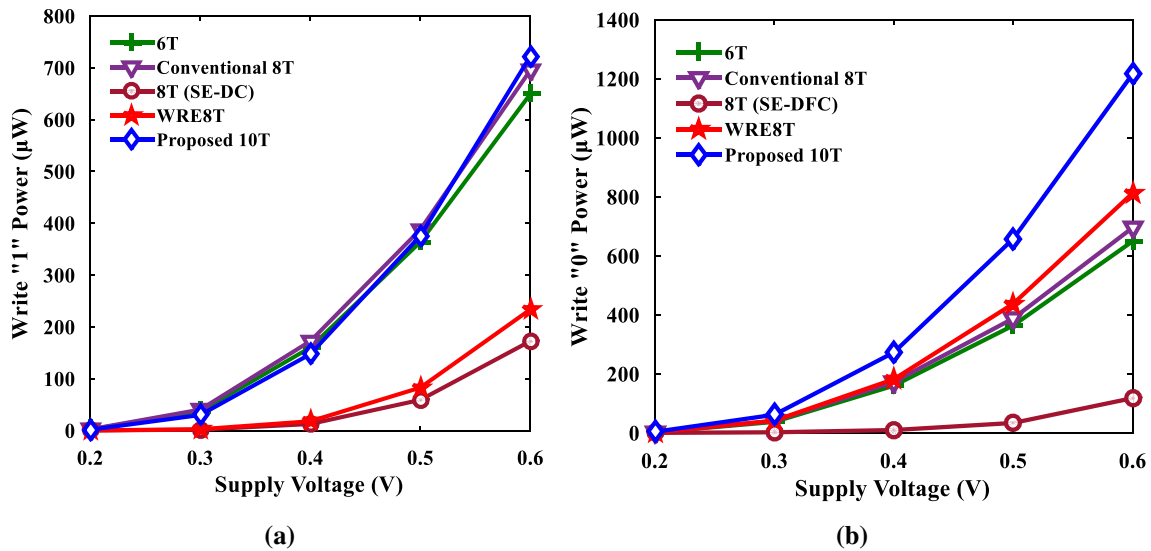Fig. 13 Read operation power of compared SRAM cells

Fig. 14 **a** Write "1" and, **b** write "0" power consumption of compared cells
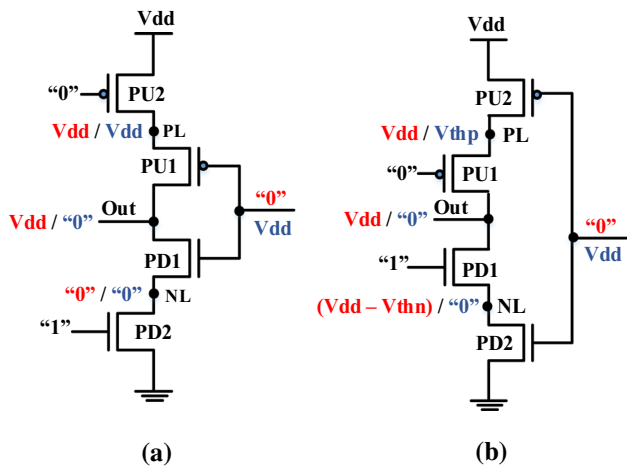

Fig. 15 Schematic view of **a** INV1 of WRE8T and, **b** INVL of the proposed cell during the hold state

during the hold state. In the hold state, WL and WLB are at zero and VDD respectively.

For the INV1 inverter, when the input is "0", the drain-to-source voltage of the OFF transistor PD1 is equal to VDD and if the input of this inverter is "1", the drain-to-source voltage of the OFF transistor PU1 is also equal to VDD. This causes maximum DIBL and leakage current for the inverter. However, for the proposed INVL, when the input is "0", the V_{ds} of the OFF transistor PD2 is equal to VDD-V_{thn} and when the input is "1", the V_{ds} of the OFF transistor PU2 is equal to VDD-V_{thp}. Therefore, the leakage power of the INVL is less than the leakage power of the INV1, as the leakage current has an exponential relationship with V_{ds} due to DIBL. Moreover, from the static power perspective, the right inverter of the proposed cell INVR benefits from stacked pull-down transistors.

Furthermore, only one transistor is used for the read operation, and the control signal of the transistor (RWL) in the hold state is set to VDD. This causes the V_{ds} of RD to be zero and thereby minimizing the transistor leakage current. As shown in Fig. 16, the proposed cell with these techniques has the lowest static power consumption among all the compared cells at all supply voltages.

3.7 Cell layout and area

Figure 17 shows the layout of the studied cells. The layouts were drawn based on FinFET design rules reported in [22]. The proposed cell has the least occupied area after the conventional 6T and 8T cells. Table 2 shows the height, width, and the area occupied by different cells. It can be seen from Table 2 that the area of the proposed cell is approximately five percent lower than the WRE8T cell.
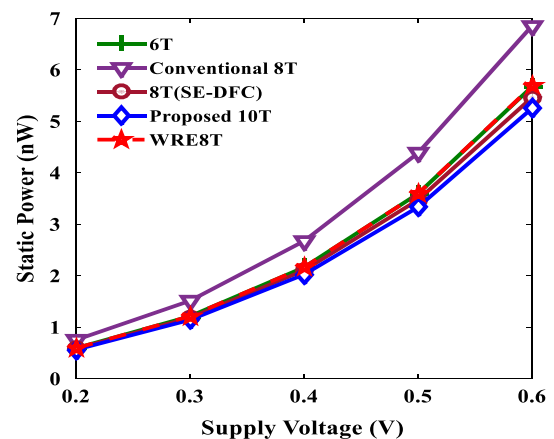
Fig. 16 Static power consumption of compared SRAM cells for different supply voltages
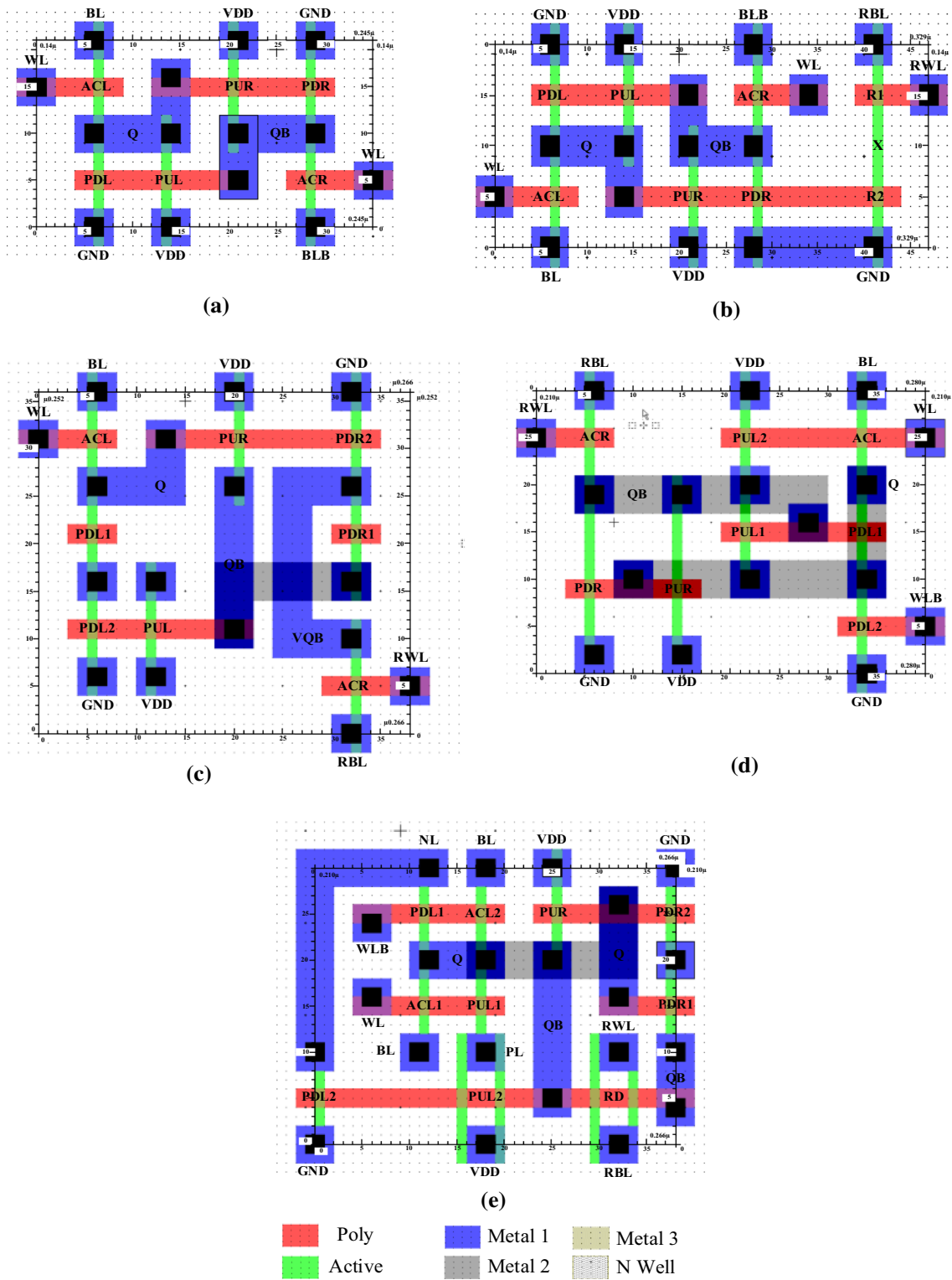
(a)

(b)

(c)

(d)

(e)

■ Poly   ■ Metal 1   ▨ Metal 3
▦ Active   ▨ Metal 2   ▨ N Well

Fig. 17 Layout of **a** 6T, **b** Conventional 8T, **c** 8T (SE-DFC), **d** WRE8T, **e** Proposed 10T SRAM cells

4 Conclusion

In this paper, a low-leakage single-ended 10T SRAM cell has been proposed. This cell improves read and write yields by decoupling the storage node from the read bitline and temporarily floating the left inverter during the write operation. Moreover, since writing '1' is difficult in single-ended SRAM cells, using an extra p-type access transistor parallel to an n-type access transistor mitigates the problem. Simulations in FinFET technology show that the proposed cell achieves a six-sigma (6σ) yield for read, write, and hold operations at a supply voltage down to 200 mV while other compared cells fail to have acceptable yield at the sub-threshold voltage. Also, by benefiting from the stack effect, reduced DIBL, and using only one transistor for the read operation, the proposed cell has the least static power, e.g., 4 and 24% lower than the conventional 6T and 8T cells at 200 mV, respectively. In conclusion, the proposed 10T cell is a suitable candidate for noise-immune, high-performance applications and a convenient option for low leakage demands.

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Nima Eslami was born in Tehran, Iran. He received the M.S. Degree in Digital Engineering from Science and Research Branch of Tehran, Iran in 2018. He is currently a Ph.D. Candidate in digital engineering at Shahid Beheshti University, Tehran, Iran. His main fields of research interest are nanoelectronic circuit design, Low-Power High-Performance VLSI design, SRAM design, FinFET circuit design and approximate computing.

Behzad Ebrahimi received the B.Sc., M.Sc. and Ph.D. Degrees all in electrical engineering from the University of Tehran, Tehran, Iran, in 2006, 2009, and 2014, respectively. He is currently an Assistant Professor at the Department of Electrical and Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran. His current research interests include low power, reliable, and high performance VLSI circuit design for emerging nanoscale technologies.

Erfan Shakouri was born in Tehran, Iran, in 1993. He graduated in Electrical Engineering, Electronics from Science and Research Branch, Islamic Azad University, Tehran, Iran with a master's degree. His current research interests include low-power and high performance circuit design and process variation tolerant circuit design in emerging and exploratory technologies.

Deniz Najafi was born in Tehran, Iran in 1994. She did her undergraduate studies in 2017 and she is currently pursuing her master's degree in digital electronics department as a senior student at SRBIAU (science and research branch Islamic Azad University)-Iran. Her research interest includes, low power VLSI circuit design, in memory computation, approximate SRAM memory design, memories and Nano Technology.