



Simple charge controlled floating memcapacitor emulator using DXCCDITA

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Abstract

This research article introduces generalized design procedure for incremental/decremental memcapacitor using analog active device that brings a charge controlled floating memcapacitor emulator. The demonstration of generalized model using Dual X current conveyor differential input transconductance amplifier (DXCCDITA) as an analog active device comes with grounded capacitor and single resistor. The important features of proposed memcapacitor emulator in comparison with other emulators are the absence of mutator and multiplier circuits that causes less design complexity, CMOS compatible circuits, high frequency operation and few more. The switching operation incorporated in proposed memcapacitor model provides incremental and decremental mode of operation to control the state of memcapacitor for real time application. The CMOS implementation of DXCCDITA uses 0.18 μm CMOS technology parameter for the design verification. The performance of the memcapacitor is verified using PSPICE simulation and the observation validates the synchronization of theoretical perspective. An adaptive learning circuit is examined as an application with the proposed memcapacitor model that validates the usage of proposed model.

Keywords Decremental/incremental mode · Dual-X current conveyor differential input transconductance amplifier (DXCCDITA) · Memcapacitor · Pinched hysteresis loop

1 Introduction

Nowadays, memristive systems have extended their domain in terms of memcapacitor and meminductor. These entire memristive family exhibit pinched hysteresis loop and depends on the past history of the system with memory ability. The success of Chua [1] contributed a new visualization approach for traditional passive elements to its memory domain. Among three memristive system (memristor, memcapacitor and meminductor), the basic one is memristor whose resistance changes with respect to past current or voltage [2]. The development of memristor based on boundary between two resistive regions, R_{on} and R_{off} using TiO_2 layers [3] have inspired the research

community. Hence, a numerous design procedure for the development of memristor using MOS based Memristor [4–6], current mode active block based memristor [7–10], PSPICE model [11–15] and few more are enriched in literature. But in recent time, a new kind of interest has been developed for the design of memcapacitor and meminductor by using various methods. This research interest arises due to easily available memristor but the other counterpart such as memcapacitor and meminductor are not easily available. Hence, researchers are very busy in implementing emulator that could exhibit the characteristics of memcapacitor [16]. However, few literatures are available for the memcapacitor models [17–30] and meminductor model [31–33]. In this scientific literature, the authors present a general procedure for memcapacitor. So this research article focuses on memcapacitor. The common procedure to realize memcapacitor is the use of mutator circuit that could transform a non-linear device characteristic to memcapacitor characteristics. Various emulator models based on mutator have memristor as a non-linear element is available in the literature [17–25].

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Some interesting results available in [21] that uses LDR based memristor to transfer V–I domain to q–V domain. While a universal mutator that is applicable for the transformation between either one of memristive devices such as memristor, memcapacitor and meminductor is presented in [25]. However, the mutator based circuit suffers from the matching constraint since all the memristor models either charge controlled or flux controlled cannot be compatible with mutator circuit. This issue may be rectified by using the mutator mentioned in [18] that is applicable for both charge and flux controlled memristor for memcapacitor emulator but still requires proper matching condition. The memcapacitor SPICE modeling is described in [26, 27] that facilitates the use of memcapacitor for simulation purpose. In these SPICE model, the time varying capacitance is achieved by a non-linear function in [26] whereas in [27] the thickness of capacitor dielectric is used to control the capacitance. In addition, a generalized memcapacitor model based on fractional order domain is also introduced in [28]. The method has two fractional orders (α , β) and these values determine the type of memristive system. An attempt is made for depiction of a charge controlled memcapacitor without the use of memristor based mutator in [29] where the time variant term is achieved by the voltage differences across a capacitor with single voltage feedback. Recently, a Memcapacitor Emulator design using single Differential Voltage Current Conveyor Transconductance Amplifier (DVCCCTA) [30] and two capacitors is presented which is restricted to grounded nature. The vigorous study of these literatures provides a significant boost for the design of memcapacitor without multiplier and emulator model with advance active block for high performance operation.

This paper comes with generalized design procedure of memcapacitor emulator along with its implementation using Dual X Current Conveyor Differential Input Transconductance Amplifier (DXCCDITA) and grounded passive components. This article is organized as follows: Sect. 2 brings the detailed design procedure for memcapacitor emulator followed by the emulator design using DXCCDITA in Sect. 3. Section 4 presents the simulation results of proposed memcapacitor characteristics namely pinched hysteresis loop, non-volatile nature and decremental/ incremental operation and a comparative study with the existing literature. The final section ends with concluding remarks of the proposed memcapacitor model.

2 General procedure for memcapacitor model

A memcapacitor is a family of a memristive system whose characteristics can be characterized by a relation between time integral of charge ($\sigma(t)$) and flux ($\varphi(t)$) [16]. In this regard, the design procedure of memcapacitor falls under two categories: (a) Charge controlled memcapacitor and (b) voltage controlled memcapacitor. The widespread representation of charge controlled Memcapacitor [29] is given by following mathematical equation as:

$$V(t) = [\beta \pm \alpha \sigma(t)]q(t) \quad (1)$$

where β and α represent the initial value of memcapacitance and variation of capacitance in terms of charge flowing through it respectively.

The conception of proposed model for memcapacitor is depicted in Fig. 1 that comprises decremental (Fig. 1(a)) as well as incremental model (Fig. 1(b)). The routine analysis of decremental mode operation for Fig. 1(a) have the input voltage V_{in} as:

$$V_{in} = V_+ \quad (2)$$

As per the charge controlled memcapacitor representation, the voltage V_+ across the non-inverting terminal (+) of Current Feedback Operational Amplifier (CFOA) should be in terms of charge ($q(t)$) and time integral of charge ($\sigma(t)$) which is achieved through a proper feedback network as shown in Fig. 1(a). The basic concept in order to incorporate $q(t)$ and $\sigma(t)$ the voltage across the capacitor (V_c) is defined by the following mathematical equation:

$$V_c = \frac{1}{C} \int Idt \quad (3)$$

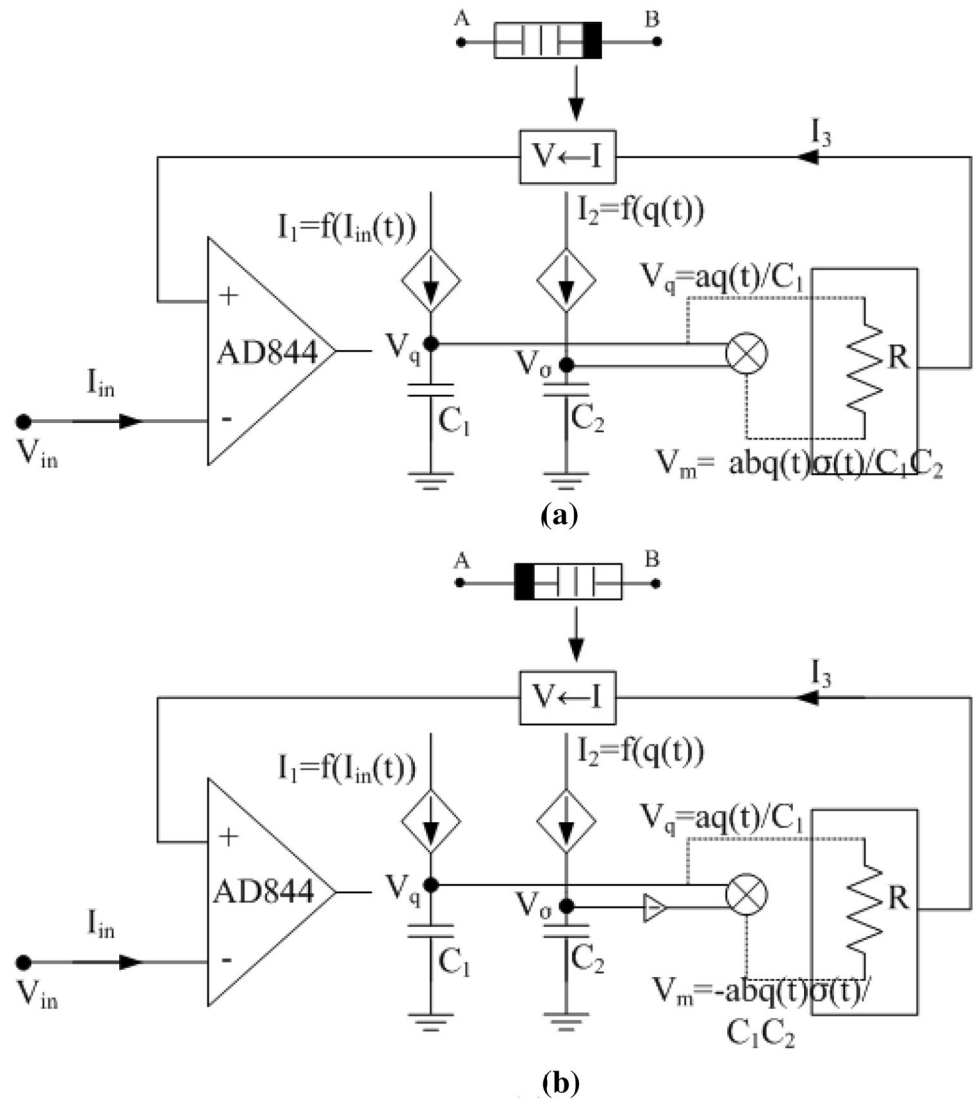
In the proposed model, two capacitors and a multiplier have an important role along with Current Feedback Operational Amplifier (CFOA) that fulfils the requirement of charge controlled memcapacitor characteristics. The fundamental variables for memcapacitor are $q(t)$ and $\sigma(t)$. Let us consider the current I_1 flowing through capacitor C_1 as a function of input current then the current and voltage become:

$$I_1 = f(I_{in}(t)) = aI_{in}(t) \quad (4)$$

$$V_{C1} = \frac{1}{C_1} \int aI_{in}(t)dt = \frac{a}{C_1} q(t) = V_q \quad (5)$$

A similar proceeding is used to obtain the time integral of charge $\sigma(t)$ by using a current source I_2 which is a function of charge $q(t)$. Hence, the current I_2 and voltage V_{C2} across the capacitor C_2 becomes:

Fig. 1 Proposed memcapacitor model. **a** Decremental mode and **b** incremental mode



$$I_2 = f(q(t)) = bq(t) \tag{6}$$

$$V_{C2} = \frac{1}{C_2} \int bq(t)dt = \frac{b}{C_2} \sigma(t) = V_\sigma \tag{7}$$

where a and b are constants. Now, the multiplier output V_m for the corresponding inputs V_q and V_σ results:

$$V_m = V_q \times V_\sigma = \frac{ab}{C_1 C_2} \sigma(t)q(t) \tag{8}$$

For the general implementation of memcapacitor model, we required two terms [16]. (a) Time invariant capacitance (β) termed as initial capacitance value and (b) time variant capacitance term (α) that offers rate of change of capacitance with respect to charge. The above mentioned terms can be intended by providing the voltages V_q and V_m respectively across a resistor (R) that results a significant current I_3 as:

$$I_3 = \frac{V_q - V_m}{R} = \left[1 - \frac{ab}{C_1 C_2} \sigma(t) \right] \frac{a}{RC_1} q(t) \tag{9}$$

The above equation can be modelled as per the basic charge controlled memcapacitor Eq. (1) by converting the current to voltage domain using (I to V) converter. Let us assume, the current to voltage conversion relation as: $V = cI$ where ‘ c ’ is a conversion constant. Then the new voltage $V_{in}(t)$ becomes

$$V_{in} = \left[\frac{ac}{RC_1} - \frac{a^2bc}{RC_1^2 C_2} \sigma(t) \right] q(t) = C_M^{-1} q(t) \tag{10}$$

Hence, the resultant inverse capacitance value will be:

$$C_M^{-1} = \frac{ac}{RC_1} - \frac{a^2bc}{RC_1^2 C_2} \sigma(t) \tag{11}$$

Finally by comparing Eq. (1) with Eq. (10), it yields

decremental memcapacitor with numerical value of β and α as:

$$\beta = \frac{ac}{RC_1}; \alpha = \frac{a^2bc}{RC_1^2C_2} \quad (12)$$

A similar approach as that of decremental mode memcapacitor can be applicable for incremental mode. The only change in this design requires an inverter before multiplier as depicted in Fig. 1(b) that gives same numerical values of α and β as that of decremental mode memcapacitor. The final expression for the charge controlled incremental memcapacitor becomes:

$$V_{in} = \left[\frac{ac}{RC_1} + \frac{a^2bc}{RC_1^2C_2} \sigma(t) \right] q(t) \quad (13)$$

$$C_M^{-1} = \frac{ac}{RC_1} + \frac{a^2bc}{RC_1^2C_2} \sigma(t) \quad (14)$$

3 Circuit description

In order to validate the general memcapacitor model, analog active building block named as Dual X Current Conveyor Differential Input Transconductance Amplifier (DXCCDITA) [34] based memcapacitor is incorporated in this paper. The DXCCDITA offers the combined flavour of DXCCII [35] and Operational Transconductance Amplifier (OTA) whose characteristics can be represented as:

$$\begin{bmatrix} I_Y \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \\ I_{O\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ \beta & 0 & 0 & 0 & 0 & 0 \\ -\beta & 0 & 0 & 0 & 0 & 0 \\ 0 & \alpha & 0 & 0 & 0 & 0 \\ 0 & 0 & \alpha & 0 & 0 & 0 \\ 0 & 0 & 0 & \mp g_m & \pm g_m & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X+} \\ I_{X-} \\ V_{Z+} \\ V_{Z-} \\ V_{O\pm} \end{bmatrix} \quad (15)$$

where g_m is the transconductance term at port $O\pm$; the non-ideal characteristics of DXCCDITA involves α and β terms that represent the current transfer gain and voltage transfer gain respectively. The transconductance term g_m can be represented as $g_m = K[V_{BO\pm} - V_{SS} - V_t]$ where $K = (k_{23,27}k_{24,28})^{0.5}$ and $k_i = \mu_i C_{ox}(W/L)_i$. The circuit symbol and the equivalent MOSFET based circuit of the DXCCDITA are illustrated in Fig. 2. The memcapacitor circuit based on DXCCDITA is depicted in Fig. 3 where the dual X ports of DXCCDITA facilitates the path of input and output current and the availability of Z_+ and Z_- offer selection of decremental and incremental mode.

The first case involves the theoretical description of incremental mode memcapacitor where the input current flows through X_- terminal and the input voltage V_{in} appears across V_A and V_B and the switch S_1 will be

connected to Z_- terminal and Z_+ will be grounded. By taking account of non-ideal (α, β) term of DXCCDITA in routine analysis gives the following set of equations as:

$$I_{in} = I_{Z-} = \alpha I_{X-}; V_{in} = V_A - V_B \quad (16)$$

$$V_{Z-} = \frac{\alpha q(t)}{C_1} = V_q \quad (17)$$

$$V_{O+} = \frac{\alpha g_m \sigma(t)}{C_1 C_2} = V_\sigma \quad (18)$$

Now in order to achieve the charge controlled memcapacitor model as in (1), the transconductance (g_m) is used with the application of bias voltage for O_- as $V_{BO_-} = V_\sigma$ that results:

$$V_{O-} = -K \left[\frac{\alpha g_m \sigma(t)}{C_1 C_2} - V_{SS} - V_t \right] \left(\frac{\alpha q(t)}{RC_1} \right) = V_Y \quad (19)$$

$$-V_{x-} = \beta V_Y = V_{x+} \quad (20)$$

Finally, the corresponding input voltage across the memcapacitor and its inverse memcapacitance are obtained as:

$$V_{in} = V_{x-} - V_{x+} = \left(\frac{2K\alpha\beta}{RC_1} \right) \left[V_{DD} - V_t + \frac{\alpha g_m \sigma(t)}{C_1 C_2} \right] q(t) \quad (21)$$

$$C_M^{-1} = \frac{2K\alpha\beta}{RC_1} \left[V_{DD} - V_t + \frac{\alpha g_m \sigma(t)}{C_1 C_2} \right] \quad (22)$$

From (22), we can observe that the initial memcapacitance and the rate of change value are $2K\alpha\beta(V_{DD} - V_t)/(RC_1)$ and $[2\alpha^2\beta g_m/(RC_1^2 C_2)]$ respectively. The decremental mode memcapacitor can be achieved with the application of input voltage port across V_B and V_A and the switch position will be changed to Z_+ and Z_- terminal will be connected to ground. A similar analysis as that of decremental mode memcapacitor yields the corresponding input voltage V_{in} and inverse memcapacitance are represented as:

$$V_{in} = V_{x+} - V_{x-} = \left(\frac{2K\alpha\beta}{RC_1} \right) \left[V_{DD} - V_t - \frac{\alpha g_m \sigma(t)}{C_1 C_2} \right] q(t) \quad (23)$$

$$C_M^{-1} = \frac{2K\alpha\beta}{RC_1} \left[V_{DD} - V_t - \frac{\alpha g_m \sigma(t)}{C_1 C_2} \right] \quad (24)$$

The Eqs. (21 and 23) clearly indicates the charge controlled memcapacitor model equation with the non-ideal parameter of DXCCDITA. The effect of non-ideal term may be discarded by considering operating frequency slightly smaller than pole frequencies of transfer gain (α, β) of DXCCDITA.

Fig. 2 DXCCDITA. **a** Block representation and **b** internal structure

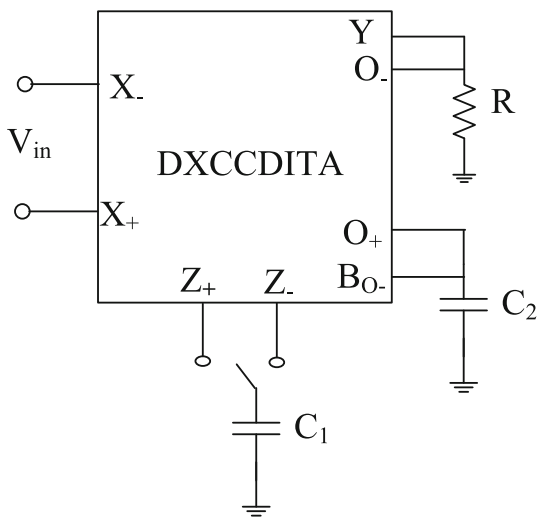
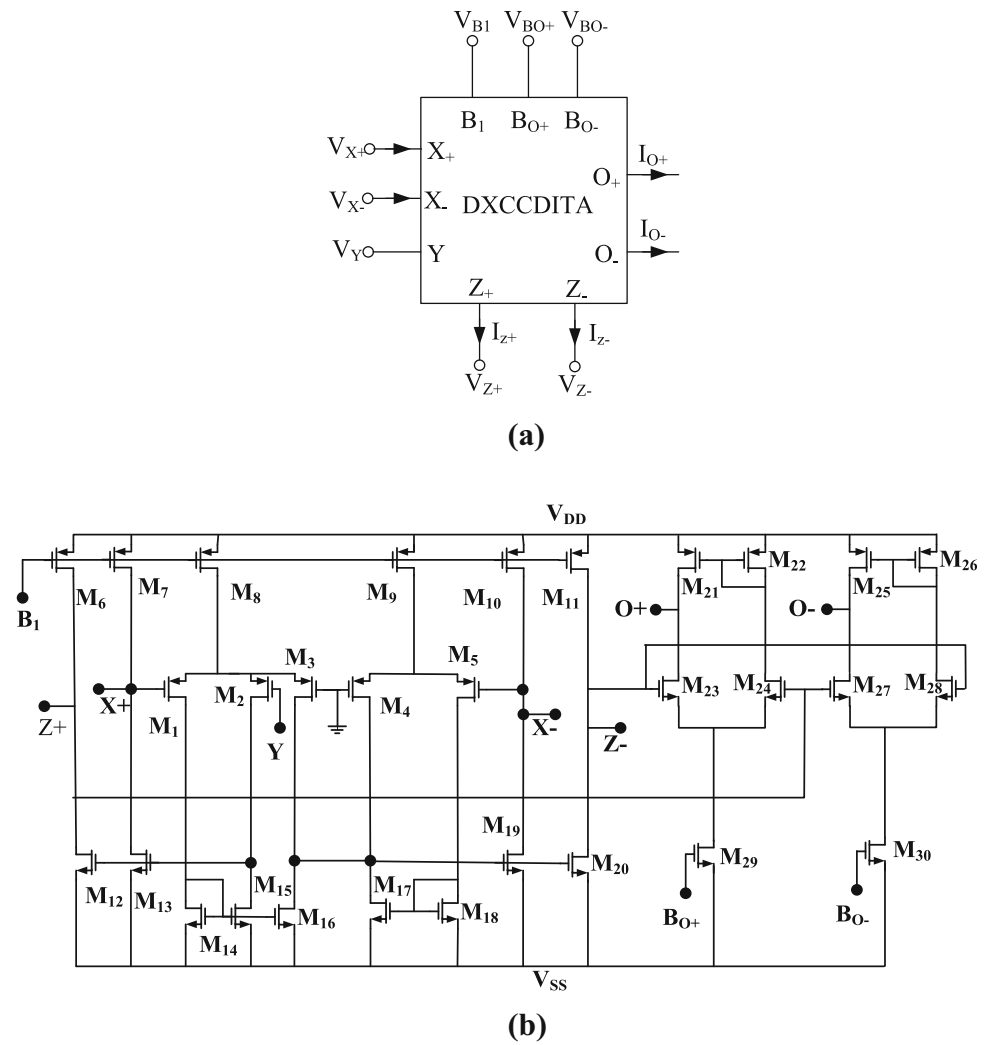


Fig. 3 Proposed memcapacitor model using DXCCDITA

4 Simulation results and comparison study

The justification of theoretical aspect of proposed mem-capacitor model as discussed in previous section is validated through PSPICE simulations. The internal structure of DXCCDITA as in Fig. 2(b) is made with 0.18 μm

Table 1 Aspect ratio of DXCCDITA

Transistors	W (μm)	L (μm)
M ₁ , M ₂	0.36	0.18
M ₃ , M ₄	0.72	0.18
M ₁₂ , M ₁₅	0.67	0.18
M _{16–18}	1.2	0.18
M _{6–13} , M _{19–20}	2.4	0.18
M _{21–22} , M _{25–26}	0.25	0.18
M _{23–24} , M _{27–28}	0.8	0.18
M _{29–20}	1.6	0.18

CMOS technology and the aspect ratio is given in Table 1. The current source in the DXCCDITA presented in [35] is replaced by MOSFETs in which M_{29-30} to facilitate the electronically tuneable transconductance term through bias voltages V_{BO+} and V_{BO-} . The supply voltages and bias voltages are $V_{DD} = -V_{SS} = 1.25$ V; $V_{B1} = 0.42$ V and $V_{BO+} = -0.6$ V respectively.

The transient response of the proposed floating memcapacitor is observed for the component values of $C_1 = 28$ pF, $C_2 = 250$ pF and $R = 100$ Ω . In order to observe the hysteresis curve, the proposed memcapacitor is examined with sinusoidal input current waveform with amplitude 50 μ A at 500 kHz with 90° phase shift. The corresponding charge is observed as the voltage V_q and the input voltage V_{in} across the terminal A and B. Figure 4 presents the transient response of incremental memcapacitor and the existence of pinched hysteresis loop. An important fingerprint of memcapacitor is pinched hysteresis loop where the area bounded by the hysteresis loop is inversely proportional to the frequency. Figure 5 shows the observed hysteresis loop for different frequencies say

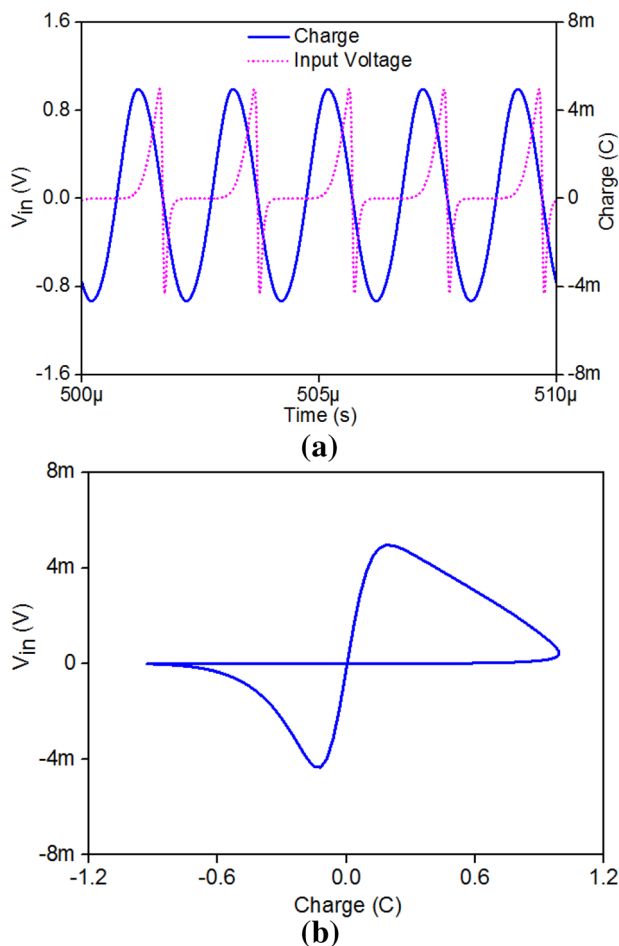


Fig. 4 Memcapacitor responses at 500 kHz. **a** Transient response of charge and input voltage and **b** pinched Hysteresis loop

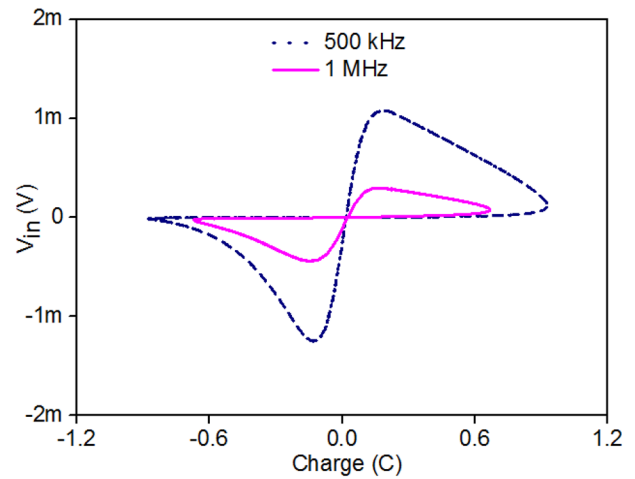


Fig. 5 Hysteresis Loop at various frequencies 500 kHz and 1 MHz

500 kHz and 1 MHz that depicts the reduction in hysteresis loop area for higher frequency. Further, the incremental/decremental mode of memcapacitor is tested for current pulse signal of amplitude 50 μ A and pulse width is 0.05 μ s over a period of 0.2 μ s whose response is presented in

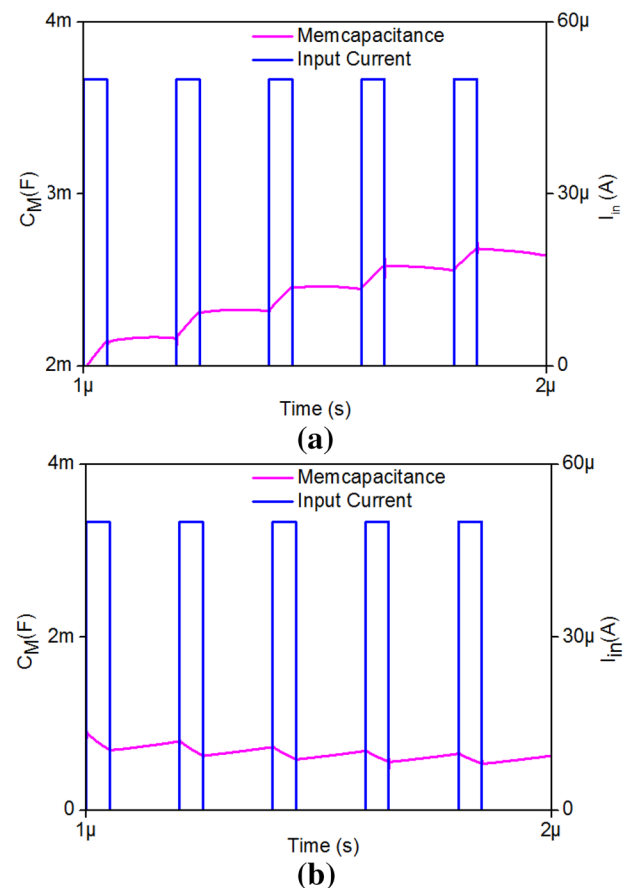


Fig. 6 Non-volatile responses. **a** Incremental mode and **b** decremental mode

Fig. 6 that informs the memcapacitance value remains constant even in the absence of pulse signal. This process is called as non-volatile nature. Hence, the proposed design for memcapacitor model confirms the workability test. In addition, the bias voltage V_{BO-} offers control over area of pinched hysteresis loop which is shown in Fig. 7.

The stability performance of the proposed memcapacitor model is examined through Monte Carlo simulation and tested for various temperatures and the results are shown in Figs. 8 and 9 respectively. In case of monte-carlo analysis the proposed model is observed for 100 runs with 5% component tolerance and from the Fig. 8, we can observe that the nature of hysteresis loop is persistent even the area of hysteresis loop is alerted for 100 runs. Likewise, in case of temperature analysis, due to the variation in temperature the current flow varies which results in change of charge accumulation in the circuit which is observed as variation in the hysteresis loop area as in Fig. 9. However the nature of pinched hysteresis loop is persistent through the temperature range – 40 to 40 °C.

A detailed comparison of the proposed charge controlled memcapacitor emulator with the existing methods is presented in Table 2. From the comparison table, we can observe that the existing emulator presented in [21–23, 25] have a mutator circuit with memristor to realize the memcapacitor emulators and certainly helped researchers to understand the behavior of memcapacitor. As the memristive devices are frequency sensitive and require adjustment of component values of memristor and mutator for the proper operational frequency of memcapacitor. This recommends a rigid procedure of constant change of passive component values in memristor and mutator circuits. In addition, the use of memristor facilitates design complexity whereas an additional effort for the design of memristor is missing in the proposed memcapacitor design.

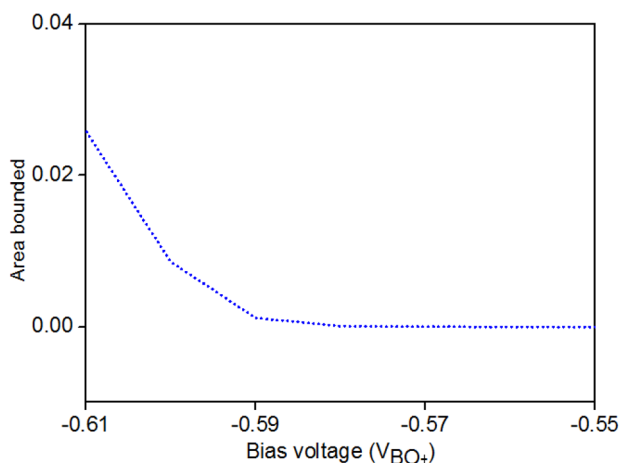


Fig. 7 Variation of pinched hysteresis area with respect to bias voltage

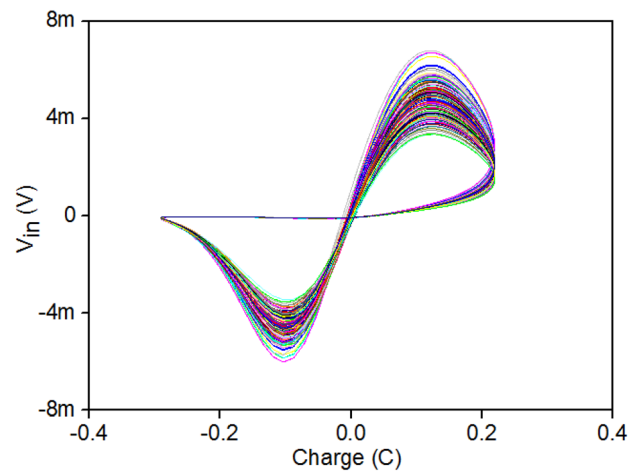


Fig. 8 Monte-Carlo response of proposed memcapacitor

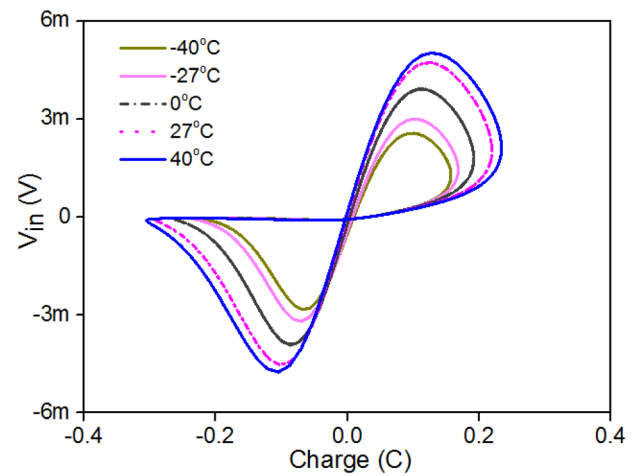


Fig. 9 Response of proposed memcapacitor at various temperatures

The recent usage of memcapacitor emulators in various applications requires a sophisticated memcapacitor model to examine further feasible applications.

Few important aspects are covered in the proposed memcapacitor design that needs to be met for a sophisticated memcapacitor design as follows: (a) free from mutator design (b) floating mode operation (c) wide frequency range. Moreover, a simple way to attain product of time integral of charge ($\sigma(t)$) and time integral of current ($q(t)$) as presented in literature [7, 9] is achieved using analog multiplier such as AD633 whose output corresponds to 1/10th of actual output which may cause reduction in the area of pinched hysteresis loop. But the proposed memcapacitor model uses transconductance term (g_m) to achieve multiplication operation. The proposed memcapacitor uses capacitor based integrator operation to achieve mutator less design as per the first (a) criteria. The second aspect (b) for a floating charge controlled memcapacitor emulator requires the feedback of input voltage (V_{in}) across

Table 2 Comparative study of proposed model with existing methods

References	Active component count	Passive component count	Type of active element used	Requirement of mutator/multiplier	Nature of MC (grounded/floating)	All passive elements are grounded	Frequency (Hz)
[21]	AD844-2	R-1, C-1, MR-1	ICs	Yes	Grounded	No	Few
[22]	CCII-2	R-1, L-1, MR-1	ICs	Yes	Floating	Yes	NA
[23]	AD844-4	R-2, C-1, MR-1	ICs	Yes	Grounded	No	< 100
[25]	AD844-3	R-3, C-1, MR-1	ICs	Yes	Grounded	No	< 100
[30]	DVCCTA-1	R-1, C-2	CMOS Technology	No	Grounded	No	1 M
This work	DXCCDITA-1	C-2, R-1	CMOS Technology	No	Floating	No	1 M

R resistor, *C* capacitor, *MR* memristor

X_- and X_+ terminals such that $V_{X_-} = -V_{X_+} = V_{in}$. The port relation of DXCCDITA offers very potent inbuilt characteristics such as $V_Y = V_{X_+} = -V_{X_-}$ which is shown in the Eqs. (20) and (21) for the calculation of V_{in} . Another prominent feature of the proposed memcapacitor emulator is the switching operation to facilitate in-situ control over memcapacitance by selecting either incremental or decremental mode of operation. The proposed memcapacitor offers a wide frequency range in comparison to [21–23, 25, 27] due to the absence of mutator and multiplier with wide bandwidth of DXCCDITA that ensures the fulfillment of third aspect (c).

5 Application

In order to explore the feasible application of the proposed memcapacitor, an Adaptive Neuromorphic structure [36] is examined. A general study based on the memristive system shows the ability of memristive system to imitate synapses nature in brain [37] and the implementation of well known associative behavior Pavlovian experiment using memristor [38] validates the above claim. This experimental test helps in the understanding of evolution over living organisms. In addition the exploration of unicellular organism named as Physarum Polycephalum [39] whose behavior is to identify the shortest distance between the mazes even though it has lack of neural network. The unique nature of Physarum Polycephalum is used in neural network implementation using memristor [40] which results in high end performance. Recently, amoeba which is the simplest unicellular organism whose existence dated till the beginning of life on earth has been examined. It is observed that amoeba has responsive nature towards temperature and

humidity in the surrounding environment. In other words, the locomotive speed of amoeba depends on environmental temperature as well as humidity. If there is a drop in temperature correspondingly amoeba will slow down its speed and also predicts the future temperature drop. This type of learning process follows three steps [41]: (a) storage of past occurrences, (b) future prediction, (c) understanding the timing of periodic events. This behavior is implemented using resistor, meminductor and capacitor [41] which shows the amoeba's adaptive behavior. A similar circuit is used by replacing the simple capacitor with memcapacitor and the adaptive behavior circuit that consists of resistor, inductor and memcapacitor as shown in the Fig. 10.

In general RLC circuit, the resonant frequency ($f = 1/(2\pi\sqrt{LC})$) will be contributed by capacitor and inductor where the resistor consumes power that results in the oscillation diminishment with respect to time. In case of memcapacitor, due to the change of capacitance in accordance with the previous current flow through it, the memcapacitor tunes to the frequency of temperature variations. Here, the temperature variations in the environment is considered as input voltage $V_{in}(t)$ and the output voltage is considered ($V_{out}(t)$) as the locomotive speed of amoeba with respect to temperature variations. The component values for adaptive learning are considered as follows:

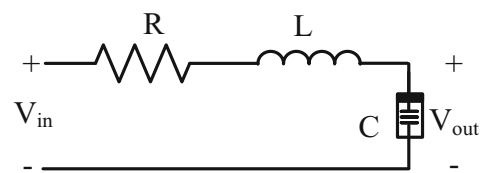


Fig. 10 Adaptive learning circuit using memcapacitor [41]

$R = 1 \text{ k}\Omega$ and $L = 1 \text{ mH}$ and the memcapacitor component value as $C_1 = 1 \text{ pF}$, $C_2 = 100 \text{ pF}$ and $R = 100 \Omega$. Figure 11 shows the responses of variation in the locomotive speed in terms of environmental temperature change. We can observe that at each point of temperature drop the voltage corresponding to locomotive speed drops. However, in the successive occurrences of the temperature drop due to the predication from the past occurrence, the locomotive speed voltage ($V_{\text{out}}(t)$) drops further in comparison with the previous voltage drop which confirms the three steps of learning process as mentioned prior in this section. Apart from this observation, we can observe the delay in the output with respect to input termed as “Delay Switching Effect” [42, 43]. Delay Switching Effect explains that the memristive systems such as memristor, memcapacitor and meminductor requires a considerable time to change its internal state from one to another which may results in the time delay in the responses. In case of the adaptive learning based on memcapacitor, the capacitor has to change its state to match the frequency of temperature variations that requires a considerable amount of time that results in a delay in the output response. From the adaptive learning using memcapacitor, we have observed that the proposed memcapacitor design is suitable for real time applications.

6 Conclusion

In this research article a new general model for the design of charge controlled memcapacitor is presented. The workability of this model is extended by a simple floating memcapacitor with two grounded capacitors, single resistor and an active block DXCCDITA. The most attractive advantages of the proposed memcapacitor model are: (a) simple design with minimum number of active and

passive components, (b) free from the limitation of memristor and mutator circuit, (c) higher operating frequency range (in Megahertz range), (d) floating nature that facilitates compatibility with other circuits, (e) electrical tunability through bias voltage of DXCCDITA, (f) control over memcapacitance through switching operation between incremental and decremental mode of operation. The viability of the proposed memcapacitor design is well verified using the PSPICE simulations. The simulation result matches well with the theoretical explanation that confirms the workability of the proposed design. In addition, the simple adaptive learning circuit implementation using memcapacitor is presented which shows the feasibility of proposed memcapacitor model for real time application. The simplicity of the circuit provides compatibility with other circuits that may extend the mem-system based application in near future.

References

1. Chua, L. O. (1971). Memristor-the missing circuit element. *IEEE Transactions on Circuit Theory*, 18(5), 507–519.
2. Chua, L. O. (1976). Memristive devices and systems. *Proceedings of the IEEE*, 64(2), 209–223.
3. Strukov, D. B., Snider, G. S., Stewart, D. R., & Williams, R. S. (2008). The missing memristor found. *Nature*, 453, 80–83.
4. Vista, J., & Ranjan, A. (2019). A simple floating MOS-memristor for high-frequency applications. *IEEE Transactions on Very Large Scale Integration System*, 27(5), 1–10.
5. Babacan, Y., Yesil, A., & Gul, F. (2018). The fabrication and MOSFET-only circuit implementation of semiconductor memristor. *IEEE Transactions on Electron Devices*, 99, 1–8.
6. Babacan, Y., & Kacar, F. (2017). Floating memristor emulator with subthreshold region. *Analog Integrated Circuits and Signal Processing*, 90(2), 417–475.
7. Yesil, A., Babacan, Y., & Kacar, F. (2014). A new DDCC based memristor emulator circuit and its applications. *Microelectronics Journal*, 45(3), 282–287.
8. Ranjan, R. K., Raj, N., Bhuwal, N., & Khateb., (2017). Single DVCCTA based high frequency incremental/decremental memristor emulator and its application. *AEU - International Journal of Electronics and Communications*, 82, 177–190.
9. Sözen, H., & Çam, U. (2016). Electronically tunable memristor emulator circuit. *Analog Integrated Circuits and Signal Processing*, 89(3), 655–663.
10. Abuelmatti, M. T., & Khalifa, A. J. (2016). A new floating memristor emulator and its application in frequency-to-voltage conversion. *Analog Integrated Circuits and Signal Processing*, 86(1), 141–147.
11. Benderli, S., & Wey, T. A. (2009). On SPICE macromodelling of TiO_2 memristors. *Electronics Letters*, 45(7), 377.
12. Rak, A., & Cserey, G. (2010). Macromodeling of the memristor in SPICE. *IEEE Transactions on Computer Design and Integrated Circuits Systems*, 29(4), 632–636.
13. Batas, D., & Fiedler, H. (2011). A memristor SPICE implementation and a new approach for magnetic flux-controlled memristor modeling. *IEEE Transactions on Nanotechnology*, 10(2), 250–255.

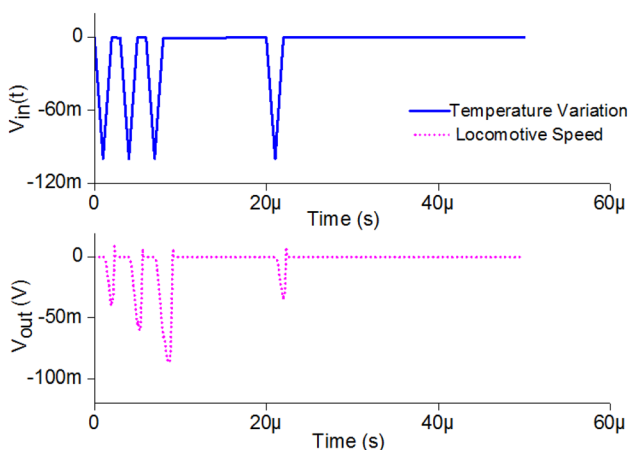


Fig. 11 Response of adaptive learning process

14. Abdalla, H., & Pickett, M. D. (2011). SPICE modeling of memristors. In *IEEE international symposium of circuits and systems (ISCAS)*, pp. 1832–1835.
15. Biolek, Z., Biolek, D., & Biolková, V. (2009). SPICE model of memristor with nonlinear Dopant Drift. *Radioengineering*, 18(2), 210–214.
16. Ventra, M. D., Pershin, Y. V., & Chua, L. O. (2009). Circuit elements with memory: Memristor, memcapacitors and meminductors. *Proceedings of the IEEE*, 97(10), 1717–1724.
17. Pershin, Y. V., & Ventra, M. D. (2010). Memristive circuits simulate memcapacitors and meminductors. *Electronics Letters*, 46(7), 17–18.
18. Biolek, D., Biolková, V., & Kolka, A. (2010). Mutators simulating memcapacitors and meminductors. In *Proceedings of IEEE Asia-Pacific conferences on circuits and systems 2010*, pp. 800–803.
19. Biolek, D., & Biolková, V. (2010). Mutator for transforming memristor into memcapacitor. *Electronics Letters*, 46(21), 1428–1429.
20. Sah, M. P., Budhathoki, R. K., Yang, C. J., & Kim, H. (2013). Expandable circuits of mutator-based memcapacitor emulator. *International Journal of Bifurcation Chaos*, 23(5), 1330.
21. Wang, X. Y., Fitch, A. L., Iu, H. H. C., & Qi, W. G. (2012). Design of a memcapacitor emulator based on a memristor. *Physics Letters-A*, 376(4), 394–399.
22. Pershin, Y. V., & Ventra, M. D. (2011). Emulation of floating memcapacitors and meminductors using current conveyors. *Electronics Letters*, 47(4), 243–244.
23. Yu, D. S., Lian, Y., Chen, H., & Iu, H. H. C. (2013). Design of a practical memcapacitor emulator without grounded restriction. *IEEE Transactions on Circuits and System II*, 60(4), 207–211.
24. Yu, D. S., Liang, Y., Iu, H. H. C., & Hu, Y. H. (2014). Mutator for transferring a memristor emulator into meminductive and memcapacitive circuits. *Chinese Physics B*, 23(7), 070702-1–070702-11.
25. Yu, D., Liang, Y., Iu, H. H., & Chua, L. O. (2014). A universal mutator for transformations among memristor, memcapacitor, and meminductors. *IEEE Transactions on Circuits and Systems II*, 61(10), 758–762.
26. Biolek, D., Biolek, S., & Biolková, V. (2010). Spice modelling of memcapacitor. *Electronics Letters*, 46(7), 520–522.
27. Biolek, D., Biolek, A., & Biolková, V. (2011). Behavioral modelling of memcapacitor. *Radioengineering*, 20(1), 228–233.
28. Guo, A., Si, G., Dia, L., Jia, L., & Zhang, Y. (2018). Generalized modeling of the fractional order memcapacitor and its character analysis. *Communications in Nonlinear Science and Numerical Simulation*, 59, 177–189.
29. Fouda, M. R., & Radwan, A. G. (2014). Charge controlled memristor-less memcapacitor emulator. *Electronic Letters*, 48(23), 1454–1455.
30. Vista, J., & Ranjan, A. (2019). Design of memcapacitor emulator using DVCCTA. *Journal of Physics: Conference Series*, 1172(012104), 1–8.
31. Liang, Y., Yu, D. S., & Chen, H. (2013). A novel meminductor emulator based on analog circuits. *Acta Physics*, 62(15), 158501.
32. Liang, Y., Chen, H., & Yu, D. S. (2014). A practical implementation of a floating memristor-less meminductor emulator. *IEEE Transactions on circuits and systems-II: Express briefs*, 61(5), 299–303.
33. Biolek, D., Biolek, Z., & Biolková, V. (2011). PSPICE modelling of meminductor. *Analog Integrated circuits and Signal Processing*, 66, 129–137.
34. Mohammad, F., Sampe, J., Shireen, S., & Md, S. H. (2017). Minimum passive components based lossy and lossless inductor simulators employing a new active block. *AEU-International Journal of Electronics and Communications*, 82, 226–240.
35. Myderrizi, I., & Zeki, A. (2017). Electronically tunable DXCCII-based grounded capacitance multiplier. *AEU-International Journal of Electronics and Communications*, 68(9), 899–906.
36. Pershin, Y. V., Fontaine, S. L., & Ventra, M. D. (2009). Memristive model of amoeba learning. *Physical Review E*, 82, 021926.
37. Pershin, Y. V., & Ventra, D. M. (2010). Experimental demonstration of associative memory with memristive neural networks. *Neural Networks*, 20, 881886.
38. Babacan, Y., & Kacar, F. (2017). FCS based memristor emulator with associative learning circuit application. *Istanbul University Journal of Electrical and Electronics Engineering*, 17(2), 3433–3437.
39. Alim, K., Andrw, N., Pringle, A., & Brenner, M. P. (2017). Mechanism of signal propagation in *P. Polycephalum*. *Proceeding of the National Academy of Science*, 114(20), 5136–5141.
40. Ntina, V., Vourkas, I., Sirakoulis, G Ch, & Adamatzky, A. I. (2017). Modeling Physarum space exploration using memristors. *Journal of Physics D: Applied Physics*, 50, 114004.
41. Wang, F. Z., Chua, L. O., Yang, X., Helian, N., Tetzlaff, R., Schmidt, T., et al. (2013). Adaptive neuromorphic architecture. *Neural Networks*, 45, 111–116.
42. Wang, F. Z., et al. (2010). Delayed switching in memristors and memristive systems. *IEEE Electron Device Letters*, 31(7), 1–9.
43. Wang, F. Z., et al. (2011). Delayed switching applied to memristor neural networks. *Journal of Applied Physics*. <https://doi.org/10.1063/1.3672409>.

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