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Multi-stage CMOS amplifier frequency compensation using a single MOSCAP

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Abstract
A multi-stage amplifier is a frequency compensated via a single and small MOSFET based capacitor. The idea reduces die occupation considerably since removes any passive elements in the compensation network. Also, a normal differential pair and a MOSFET based capacitor form compensation network and boost DC gain simultaneously. The proposed approach is symbolically described via MATLAB and numerically simulated via HSPICE circuit simulator using standard TSMC 0.18μ CMOS technology. According to mathematical justifications and simulation results, the proposed amplifier shows operation excellency especially in terms of die occupation and frequency response parameters which make it appropriate choice to realize larger analog and mixed mode systems like modulators and data converters.

Keywords CMOS · OTA · Frequency compensation · Multi-stage amplifiers · MOSCAP · Capacitor-less frequency compensation

1 Introduction

Amplifiers play an inevitable role in many electronics systems include modulators and data converters. Using an amplifier, almost any functional block can be realized, so the amplifier is considered as the most important block in analog and mixed mode electronics. Extensive researches are performed to design different configurations and improve basic techniques for more efficient amplifier design. Usually, to address advanced demands regarding DC gain and GBW requirements, two approaches are considered by circuit designers. Firstly, the tendency is to use Cascode structures, since appropriate DC gain and acceptable GBW are available. For instance, Akbari M et al. [1, 2] and Aghaee et al. [3] report improved folded Cascode (FC) amplifiers, reaching more than 70 dB as DC gain and more than 300 MHz as GBW while driving small load capacitors in a range of few pF. Cascode technique as depicted in Fig. 1 uses MOSFETs vertically which reduces output swing, depending on allocated drain-source voltage for each MOSFET. Considering the feature size and supply voltage reduction in advanced CMOS technologies, Cascode approach is not compatible with technology advancements. The reason is the fact that there is not enough voltage budget to allocate MOSFETs drain-source which have to work in the saturation region. In this region, the absolute value of drain-source voltage must be larger than $V_{GS} - V_{th}$. Where V_{GS} is gate-source voltage and V_{th} is threshold voltage value. So, satisfying MOSFETs to operate in the saturation region is a challenging and may impossible task to design Cascode structures in advanced CMOS technologies. This limitation becomes more rigid when demands are at a great level for high speed and high DC gain amplifiers. Therefore, the second approach as multi-stage amplifiers or Cascade configurations attracted designer attention. The cascade amplifies are able to provide very high DC gains (more than 100 dB for three-stage

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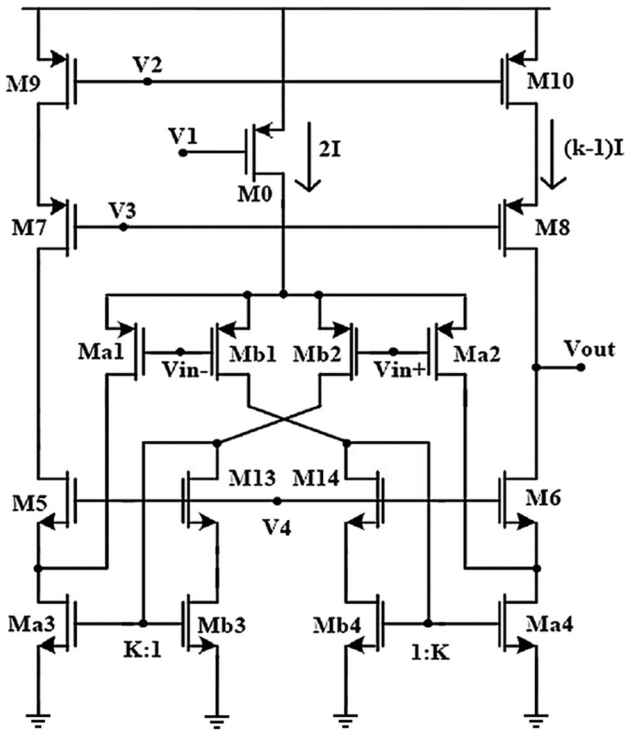

Fig. 1 Recycling folded cascode amplifier [3]

cases) and also can be realized via cascading simple gain stages like common source stage. But the main problem in dealing with the multi-stage amplifier is instability issues which are raised due to increasing nodes of the amplifier compared to Cascode structures. This problem is dominant since poles and zeros locations determine the amplifier response. The value of GBW and PM directly related to pole-zero map of the amplifier. In a simple view, poles and zeros positioning via circuit parameters (like gm, r, CC) is the subject of numerous multi-stage works. For instance, Grasso et al. [4] describes general methods for three stage cases manly based on NMC and RNMC approaches. Using differential current conveyor is investigated in Shahsavari et al. [5]. Also, Grasso et al. [6] presents details description of RNMC methods. As a complete new method, Largani et al. [7] is used differential block in compensation network and reduced size of compensation capacitor considerably. To boost bandwidth of the amplifier, Peng and Sansen [8] proposed a new scheme, exploiting direct injection via a separate feed forward path while Lee and Mok [9] tries to realize an active frequency compensation network using active transistor instead of passive elements like capacitors and resistors. As a high performance three stage amplifier, Biabanifard et al. [10] presents a novel scheme of compensation capacitor using a current subtractor. In addition, Grasso et al. [11] dedicated to improve RNMC using additional resistors and buffers. To reduce noise effects and its degenerations, Akbari et al. [12] introduces a simple design methodology via transistor sizing which is appropriate to consider in circuit design. Additionally, Aloisi et al. [13] investigates using buffers in RNMC configurations. To point out current mode operation, Shahsavari et al. [14] exploits current conveyors and benefits its high speed performance. As a control view, Leung et al. [15] discusses design via control theories while Largani et al. [16] attenuates feed forward paths to improve frequency response. Also, Akbari et al. [17] highlights noise performance for a multi stage amplifier and Biabanifard et al. [18] exploits a fully differential block to realize both output stage and frequency compensation network. In addition a comprehensive design using binary matrixes is proposed in Biabanifard et al. [19] which is appropriate for computer aided designs. At last, Chaharmahali et al. [20, 21] and Zaherfekr and Biabanifard [22] attenuate and amplify feed forward and feedback paths respectively which all improve frequency response compared to conventional NMC and RNMC approaches.

To specify the discussion atmosphere, Fig. 2 is presented. Nested Miller compensation [4] and revered nested Miller compensation [6] are considered as conventional approaches to design three-stage amplifiers. Both are simple while RNMC is more efficient than NMC. The nested loop in the RNMC structure is not loaded on the output node, leads to the smaller capacitor in the output node. Consequently, the possible dominant or first non-dominant pole is shifted to higher frequencies and more degree of freedom is provided compared to NMC. In

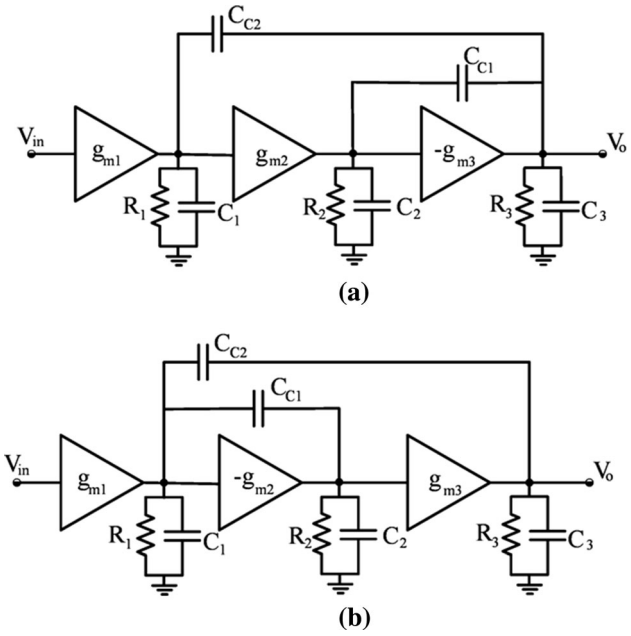

Fig. 2 Two general methods of three-stage frequency compensation [4] **a** nested miller compensation, **b** reversed nested miller compensation

addition, NMC and RNMC have to unlimber negative loop gains which guarantee proper Miller effect. So, the sign of stages is absolutely determined as depicted in Fig. 2.

Based on the previous state of the art [4, 6], these amplifiers are capable of driving capacitors as large as 100 pF while exhibiting 100 dB, 0.22 MHz, and 70° as DC gain, GBW, and PM, respectively. In addition, to driving a 100 pF load capacitor, NMC and RNMC need more than 100 pF as compensation capacitor (collecting both compensation capacitors). This is a very bad condition regarding die occupation. Usually, the load capacitor can be an off-chip one, so the compensation capacitor is the sole passive element in the circuit. The size of the compensation capacitor is determinative. Any effort to reduce the size of the compensation capacitor reduces die occupation proportionally. Also, lower capacitors lead to higher circuit dynamics (poles and zeros) which can improve frequency response parameters like GBW and PM.

In this content and mentioned environment, several works are reported to improve NMC and RNMC schemes. The improvements mean larger GBW, more stable circuits, less power consumption, more simple circuit design, and less die occupation.

Addition of nulling resistor to the Miller capacitor (compensation capacitor) provides more degree of freedom to control poles and zeros location. Even paved the way to pole-zero cancellation scenarios [11]. Using voltage and the current buffer is verified to increase GBW value since buffers are one-way blocks and can obstruct feedforward paths. This means that the Right Half Plan (RHP) zero shifts to very high frequencies and its effects are negligible [13].

At last, Largani et al. [7] is introduced to highlight the role of differential pair stage in the compensation network. Since the differential block can amplify and attenuate multiple paths simultaneously, it can be used as a multi-task block in the circuit. For instance, Largani et al. [7] uses a differential pair to form a compensation network, while it can be used to boost DC gain too. Also, by placing compensation capacitor in series with differential block, the capacitor value can be control via gain of differential stage [7], so smaller Miller capacitor can perform frequency compensation with the aim of virtual amplification. This is a great advantage to reduce die area. This type of amplifiers is used in many telecommunication systems such as Khalesi and Ghods [23].

Rest of this paper is organized as follows. Section 2 describes and discusses the proposed method which is based on RNMC scheme while compensation capacitors are replaced with a small MOSCAP. This reduces die occupation as low as possible and it can be said that there is no passive element to occupy die. So, die area is fully allocated to MOSFETs. Section 3 introduces circuit level implementation of the proposed device and reports simulation results which are extracted from MATLAB (symbolical and simplified TF) and HSPICE circuit simulator. Discussion around the proposed amplifier and its performance are brought in Sect. 4. Finally, the paper is concluded in Sect. 5 as the conclusion.

2 Proposed method

Using a fully differential block to form compensation network and boost DC gain besides realizing a small compensation capacitor via a MOSFET are suggested in this work. As depicted in Fig. 3, the proposed amplifier consists of two differential stages as the first and last stages. Also, the second and third stages are simple common-source gain stage. Also, just a single capacitor is shared in two loops include ($g_{m2}g_fr_{f+}C_C$) and ($g_{m2}g_{m3}g_fr_{f+}C_C$) which could be small with the existence of (g_fr_f) in loop gains terms. According to current allocations, this factor can be set in a relatively large range from 10 to 500 which is the gain of the differential block. So, the compensation capacitor value can be select 10–500 times smaller while the loop gain value remains unchanged compared to conventional RNMC configuration. This reduces die area considerably while increase chances to implement compensation capacitors via an active MOSFET similar to Fig. 3 as a controlled gate-bulk capacitor.

The Kirchhoff Current Law (KCL) is applied to the presented linear model in Fig. 3. Five nodes as five outputs of stages are considered. It should be noted that the last stage has two outputs. So five equations are obtained which variables are nodes voltages. The transfer function is calculable as ration of the output voltage to input. We solved the set of equation symbolically with MATLAB advanced toolbox for symbolical calculations. The obtained TF is heavy and complicated to deal with paper and pencil. So, a simple simplification is performed via two basic assumptions. First of all, we consider that each stage has DC gain ($g_{mi}r_i$) larger than unity and secondly we assume that $C_L > C_C > C_{Parasitics}$. These two assumptions help to find dominant terms and neglecting marginal terms. As a result, the simplified TF is described via (1). Where C_L is load capacitor, C_C is a compensation capacitor and g_{mi} is ith stage transconductance. Also, r_i represents ith stage output impedance while *s* denotes Laplace variable. From (1), two poles and a single RHP zero are calculated as (2), (3) and (4). It is obvious that both P_2 and Z are really large values and the system behaves like single pole systems.

$$H = \frac{\left(C_C g_{m1} r_1 r_f\right)s - g_{m1}g_{m2}g_{m3}g_f r_1 r_2 r_3 r_f}{C_C C_L r_1 r_f s^2 + \left(C_C g_{m2} g_{m3} g_f r_1 r_2 r_3 r_f\right)s + 1} \tag{1}$$

$$P_1 = \frac{1}{C_c g_{m2} g_{m3} g_f r_1 r_2 r_3 r_f} \tag{2}$$

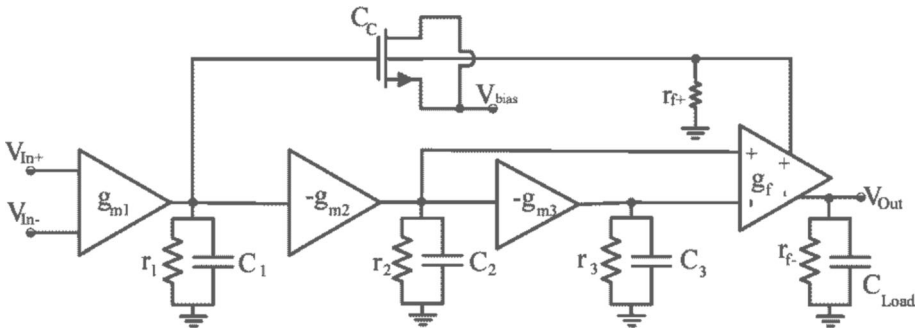

Fig. 3 The proposed multi-stage configuration

$$P_2 = \frac{g_{m2}g_{m3}g_f r_2 r_3}{C_L} \tag{3}$$

$$Z = \frac{g_{m2}g_{m3}g_f r_2 r_3}{C_C} \tag{4}$$

To more in-depth knowledge of poles and zero locations, numerical values are allocated to circuit parameters. The values are extracted from circuit simulation in the next stage. Table 1 reports numerical values for circuit parameters.

Based on the extracted values for circuit parameters, poles and zeros are settled which is shown in Fig. 4 as the system pole-zero map. According to this figure, the first pole is occurred in − 129 rad/s, the second pole occurs in − 2.29 G rad/s and the right side zero frequency is 255 G rad/s. The fact is that the second pole and the zero are in high frequencies and can be neglected without any error.

Additionally, GBW is defined as the product of DC gain and first pole. DC gain is described via (5) and GBW is calculated via (6).

Table 1 Circuit parameters and corresponding numerical values

Circuit parameter	Symbol	Value
First stage g_m	g_{m1}	60e−6
Second stage g_m	g_{m2}	185e−6
Third stage g_m	g_{m3}	820e−6
differential block g_m	g_{mf1} and g_{mf2}	100e−6
First stage output resistor	r_1	5.6e4
Second stage output resistor	r_2	12e4
The third stage output resistor	r_3	3.7e4
Differential block output resistors	r_{f+}	5.6e4
	r_{f-}	5.6e4
Compensation capacitors	C_C	0.9e−12
Load capacitor	C_L	100e−12

$$A_{DC} = g_{m1}g_{m2}g_{m3}g_f r_1 r_2 r_3 r_f \tag{5}$$

$$GBW = A_{DC} \times P_1$$

$$GBW = \frac{g_{m1}}{C_C} \tag{6}$$

Based on reported values in Table 1, the system behaves like a single pole system which means shows 90° as PM. Depends on the application, may lower PM be more desirable since the single pole system with PM equal to 90° is slow compared to systems satisfying Butterworth criteria (PM = 63°). So, the second pole is determinative. Considering the fact that each pole degenerates PM in a frequency range of one decade before and one decade after its occurrence, it can be concluded that to reach PM equal to 90°, the second pole must be at least ten times bigger than GBW frequency. While to obtain PM equal to 63°, the second pole has to be two times bigger than the GBW frequency. This condition is formulated via (7) and (8) respectively.

$$PM = 90^\circ \rightarrow P_2 = 10 \times GBW \tag{7}$$

$$PM = 63^\circ \rightarrow P_2 = 2 \times GBW \tag{8}$$

Replacing (3) and (6) in (7) and (8), the g_f or C_C can be developed further. For instance, the g_f for each state can be described as below:

$$PM = 90^\circ \rightarrow g_f = \frac{10 \times g_{m1} \times C_L}{g_{m2} \times g_{m3} \times r_2 \times r_3 \times C_C} \tag{9}$$

$$PM = 63^\circ \rightarrow g_f = \frac{2 \times g_{m1} \times C_L}{g_{m2} \times g_{m3} \times r_2 \times r_3 \times C_C} \tag{10}$$

It should be noted that (7), (8), (9) and (10) specify borders for PM and g_f values. Any other value between two borders is acceptable which results in PM in the range of 63° to 90°.

The next section reveals more details on simulation results and operational performance of the amplifier.

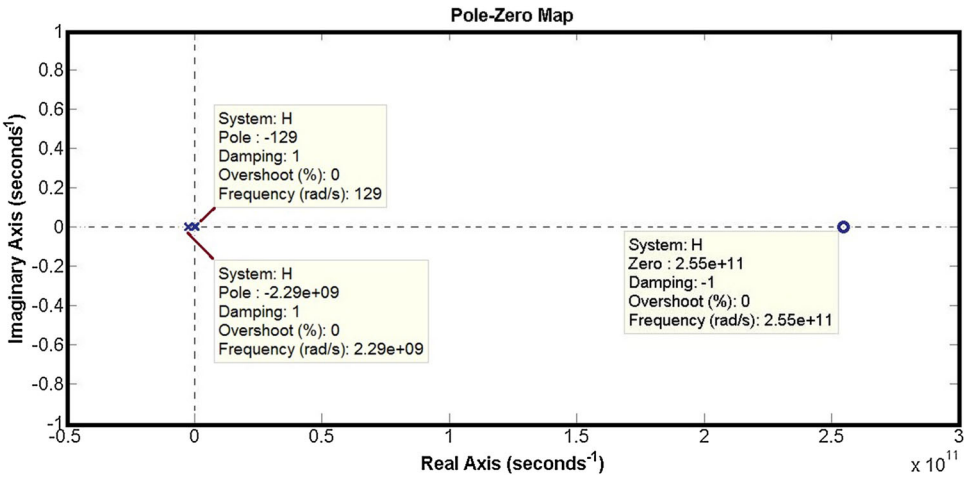

Fig. 4 Pole-zero map of the proposed structure (two left side poles and a single right side zero are shown with their frequencies)

3 Simulation results

The proposed method is simulated using standard TSMC 0.18 μm CMOS technology and HSPICE circuit simulator. The circuit schematic is depicted in Fig. 5. All MOSFETs are set to operate in saturation region and the MOSCAP is designed to show 0.9 pF capacitance. MOSFETs dimensions and corresponding bias values are tabulated in Table 2.

The most important response for an amplifier is Bode diagram since reveals DC gain, GBW and PM values. It also can report a simple vision of poles and zerosfrequencies. TF described in (1) and frequency domain simulation of Fig. 5 is presented in Fig. 6 as the frequency response of the proposed circuit. According to this figure, both the theory and simulation are matched together in the operational frequency of the amplifier which is considered GBW. After this frequency mismatch exists which is ignorable. In addition according to this figure, DC gain, GBW, and PM are obtained equal to 120 dB, 18 MHz and 89°, respectively. The reported power consumption via simulator is 545 μW, which is needed to provide relatively large transconductances as reported in Table 1.

Table 2 MOSFETs dimensions

MOSFET	W (μm)/L (μm)	MOSFET	W (μm)/L (μm)
M_1 and M_2	2.5/1.44	M_8	9/1.44
M_3 and M_4	19.8/1.44	M_{f1} and M_{f2}	22/1.8
M_5	10./1.44	M_{f3} and M_{f4}	3.4/0.18
M_6	28/0.72	M_{f5}	1.55/0.18
M_7	83.2/1.44	MOSCAP	7.8/1.44
M_9	62./1.44		

Considering circuit dependency to compensation capacitor, Figs. 7 and 8 are presented. These figures report GBW and PM versus compensation capacitor deviation. Since, MOSCAP is exploited and mismatches may exist in

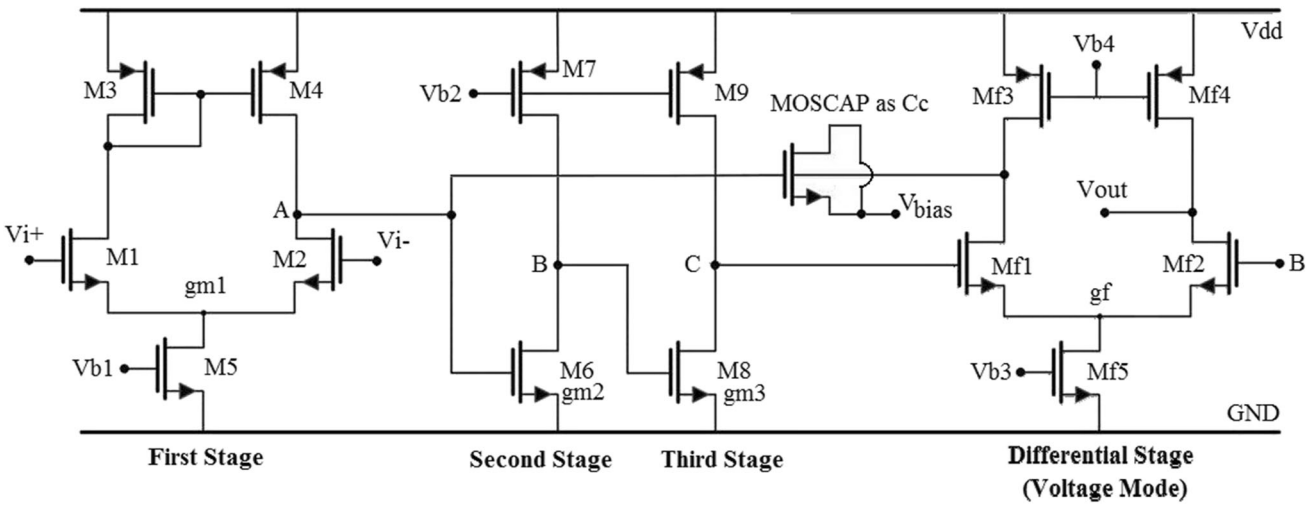

Fig. 5 The proposed circuit implementation

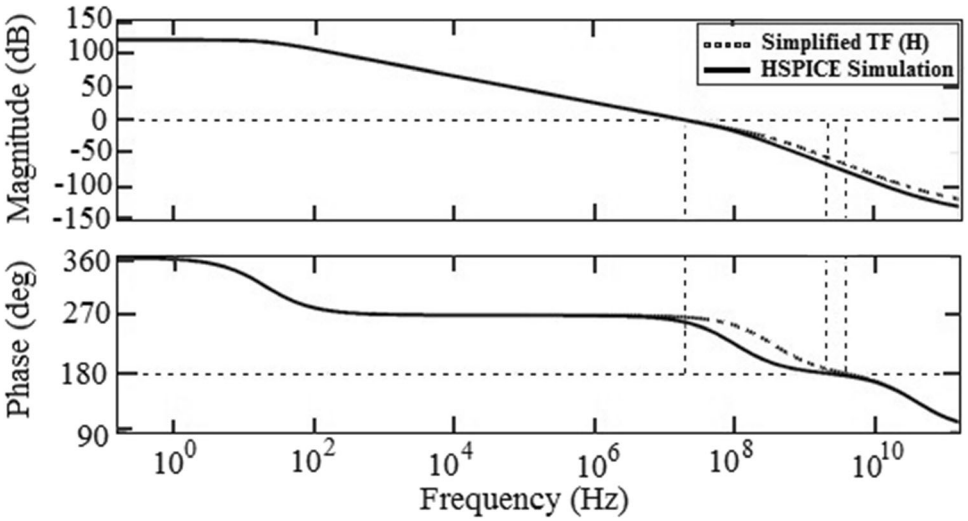

Fig. 6 The frequency response of simplified TF versus HSPICE simulation

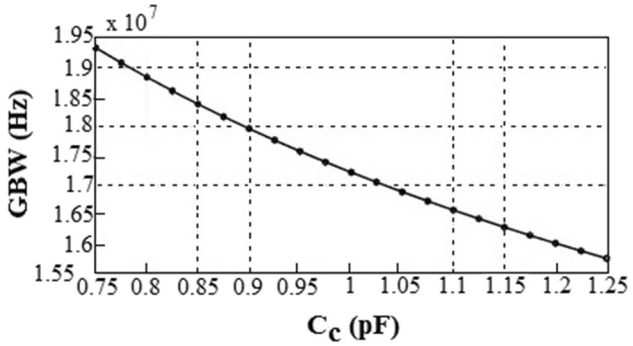

Fig. 7 GBW versus MOSCAP value

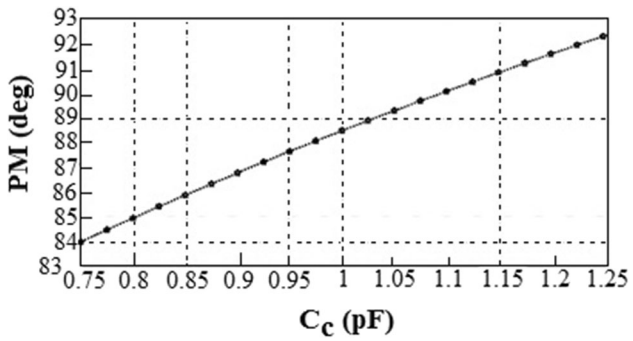

Fig. 8 PM versus compensation capacitor

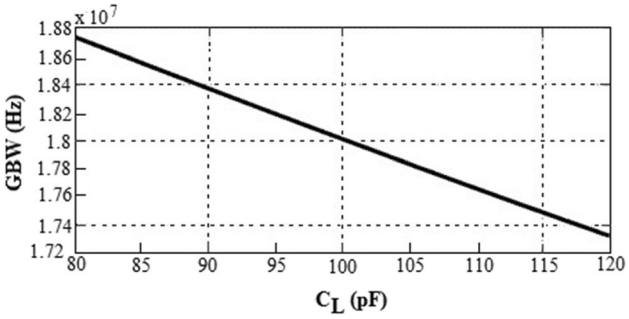

Fig. 9 GBW versus load capacitor variation

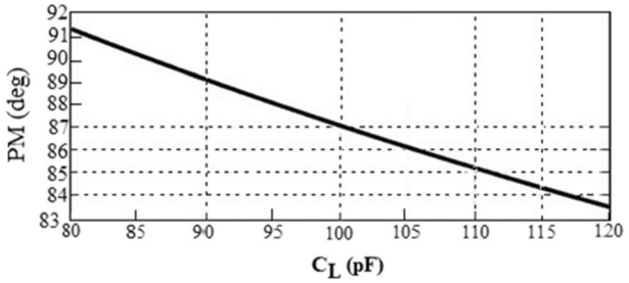

Fig. 10 PM versus load capacitor variation

the fabrication process. According to these figures, the proposed circuit is appropriately robust against MOSCAP mismatches.

Also, Figs. 9 and 10 report GBW and PM against load capacitor variation. The load capacitor variation is ± 20%, while GBW deviates less than 1 MHz and PM deviation is less than 4°.

To investigate the transient response of the proposed circuit, Fig. 11 is presented as the step response. Both rising and falling edges are included. Based on the presented step response, the settling time is 23 ns. Also, the response is similar to single pole systems without any overshoot.

Circuit dependency on transconductances is always important since several errors and mismatches are inevitable such as noisy condition and fabrication errors. To investigate the proposed circuit dependency to stages transconductances, Figs. 12 and 13 report GBW and PM versus g_{mf} variations. Figures 14 and 15 show circuit dependency versus g_{m1} variations while Figs. 16 and 17 illustrate GBW and PM deviations against g_{m2} changing. At last but not least Figs. 18 and 19 are presented to show GBW and PM deviations versus g_{m3} variation. According

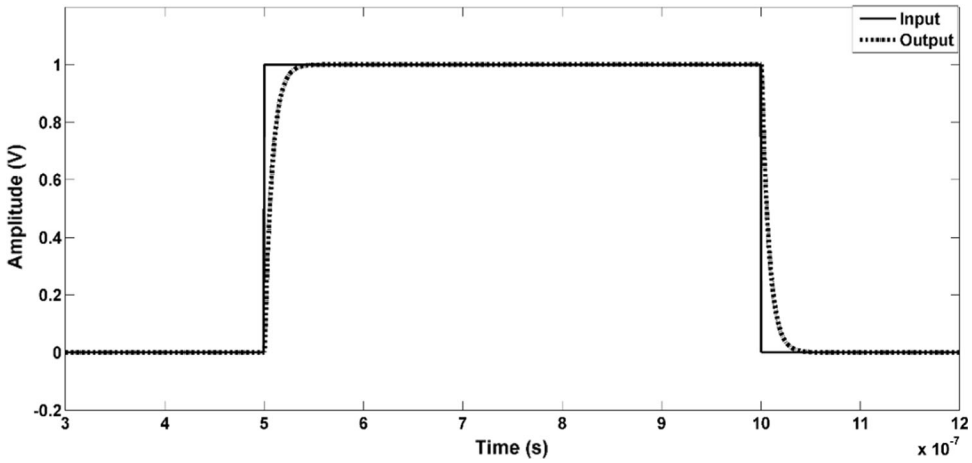

Fig. 11 Step response of the proposed amplifier

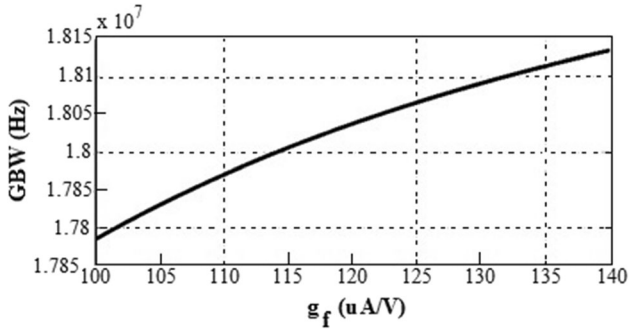

Fig. 12 GBW versus g_f

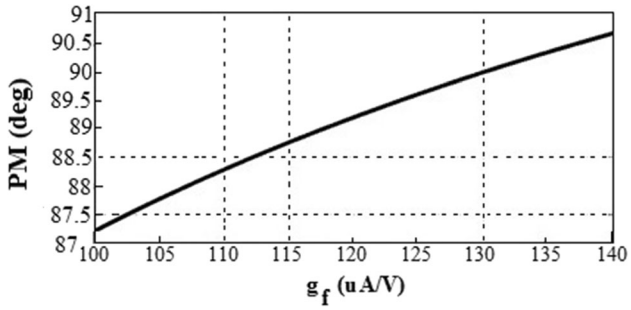

Fig. 13 PM versus g_f

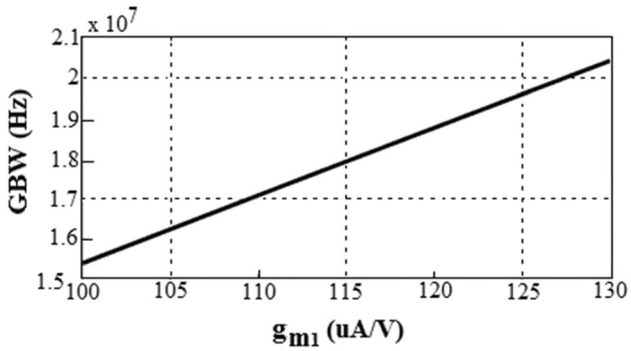

Fig. 14 GBW versus g_{m1}

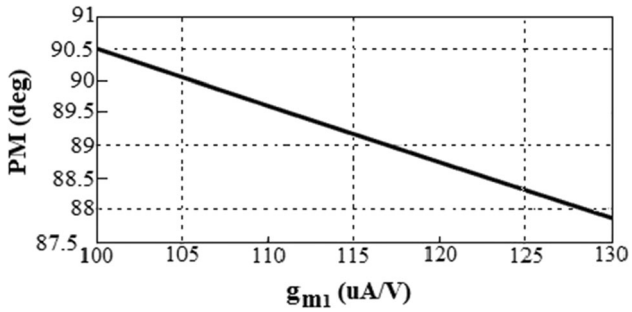

Fig. 15 PM versus g_{m1}

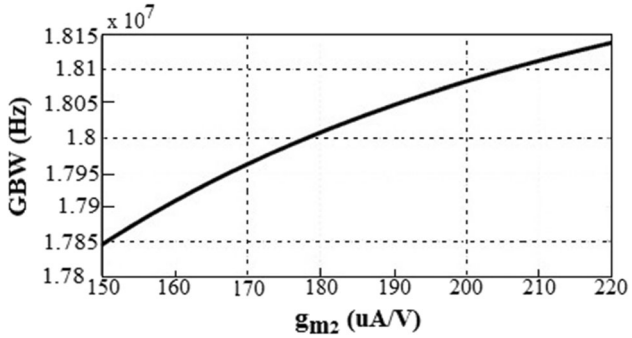

Fig. 16 GBW versus g_{m2}

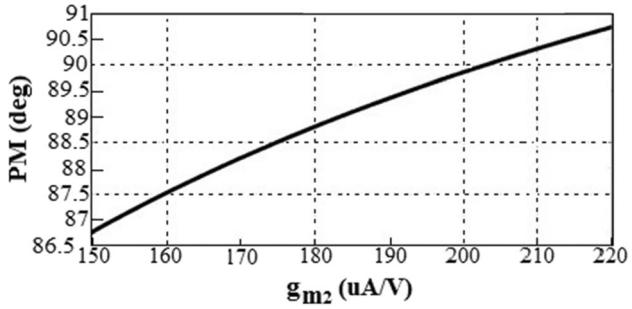

Fig. 17 PM versus g_{m2}

to this analysis, the proposed circuit could be considered as a robust amplifier against transconductances values.

In addition, Monte-Carlo simulation is performed and circuit parameters set to 30% variations on normal values under Gaussian distribution. The circuit is simulated using 100 iterations which results are shown in Fig. 20.

4 Discussion

To compare the proposed circuit with other existing works, tradeoffs have to be considered. Using defined figure of merits (FOM) in Biabanifard et al. [19], the comparison table reports amplifier parameters and FOM values of the proposed work along with another state of the art in Table 3. The defined FOMs are highlighting small and large signal behavior via (11) and (12). Also, the compensation capacitor is considered in (13) to magnify the effect of the compensation capacitor. Finally, PM is placed on the numerator of (14) to express stability merit.

$$FOM_S = \frac{\omega_{GBW} \times C_L}{Power}\left(\frac{Hz \times F}{W}\right) \tag{11}$$

$$FOM_L = \frac{SR \times C_L}{Power}\left(\frac{1}{V}\right) \tag{12}$$

$$FOM_1 = \frac{\omega_{GBW} \times C_L^2}{Power \times C_{Ctot}}\left(\frac{Hz \times F}{W}\right) \tag{13}$$

$$FOM_2 = \frac{\omega_{GBW} \times P \cdot M}{Power}\left(\frac{Hz \times {}^\circ}{W}\right) \tag{14}$$

According to Table 3, the proposed amplifier shows higher performance especially the compensation capacitor value is reduced notably while is realized via MOSCAP. Also, the defined FOMs values verify the efficiency of the simulated amplifier.

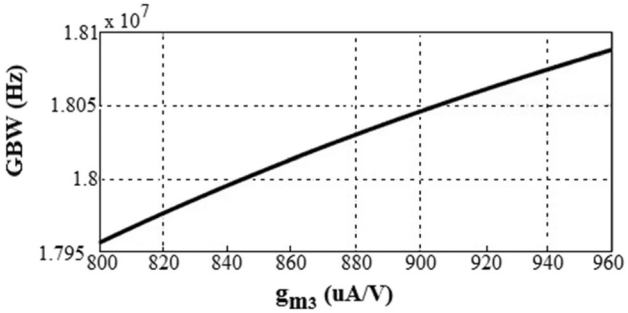

Fig. 18 GBW versus g_{m3}

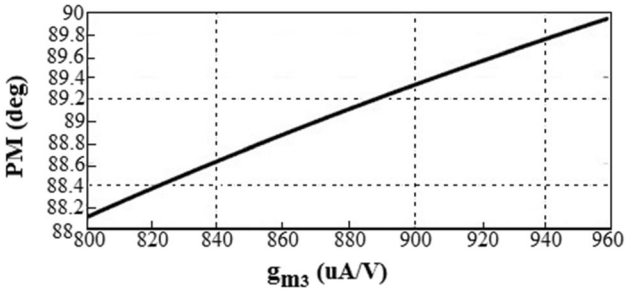

Fig. 19 PM versus g_{m3}

5 Conclusion

A MOSCAP based frequency compensation method is discussed. Exploiting differential block to realize compensation network, reduced size of compensation capacitor. Also, the differential block boosts DC gain of overall amplifier. The proposed approach modeled via symbolical TF and simulated via TSMC 0.18 μm CMOS technology while HSPICE circuit simulator is used. Based on theoretical and obtained simulation results, the circuit is capable of driving a 100-pF as a load capacitor just by a single 0.9 pF compensation capacitor. This reduces the die area considerably. Also, ample simulations are performed to

Fig. 20 Monte-Carlo results

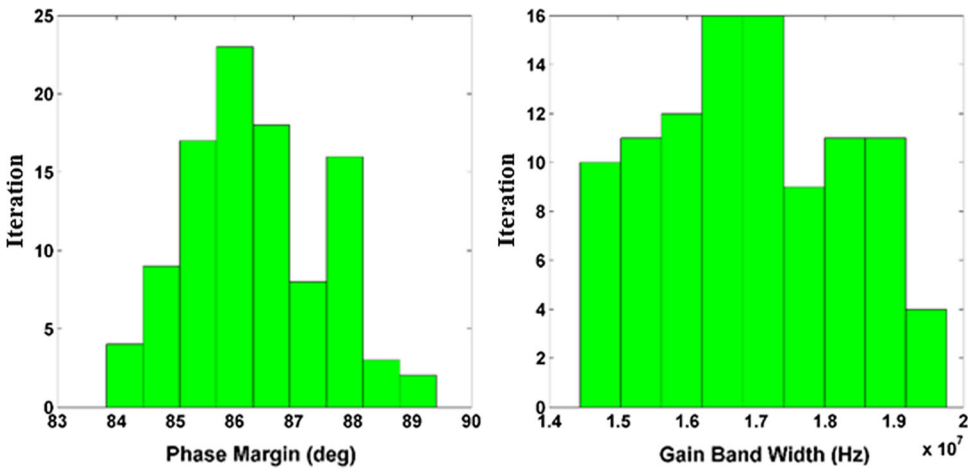

Table 3 Comparison table of the amplifier parameters and FOM values

	DC gain (dB)	Load (pF)	Power (μW)	GBW (MHz)	Compensation capacitor (pF)	Slew rate (V/μS)	P·M (°)	FOM_s	FOM_L	FOM_1	FOM_2
NMC [4][b]	100	100	345	0.22	110	0.25	68.3	0.06	0.07	0.054	0.04
NMCNR [4][b]	100	100	345	0.32	78	0.30	70.5	0.09	0.08	0.115	0.06
DPZC [6][b]	100	100	345	0.40	49.5	0.39	90.5	0.11	0.11	0.222	0.10
MNMC [6][b]	90	100	431	0.54	141	0.35	40	0.12	0.08	0.085	0.05
NGCC [6][b]	> 100	100	365	0.25	96	0.33	69.1	0.06	0.09	0.062	0.05
NMCF [4][b]	102	100	345	0.67	34	0.57	69.6	0.19	0.16	0.558	0.13
NMCFNR [13][b]	> 100	100	345	0.80	28.7	0.63	72.1	0.23	0.18	0.801	0.16
DFCFC [15][a]	> 100	100	372	0.96	35	0.80	66.6	0.25	0.23	0.714	0.17
AFFC [9][a]	> 100	100	424	2.60	15	12.00	70.4	0.61	2.83	4.066	0.42
ACBC [8][a]	> 100	100	365	2.06	18	1.22	69.6	0.56	0.33	0.311	0.38
RNMC [11][a]	> 100	120	330	2.50	8	–	50	0.90	–	13.50	0.37
NFRNMC [13][b]	> 100	120	360	2.50	8	–	66	0.83	–	12.45	0.45
CFRNMC [13][b]	> 100	120	400	2.50	8	–	71	0.75	–	11.25	0.44
[18][a]	114	100	360	6.66	4	1.12	90	1.85	0.31	46.25	1.66
ACBC [20][a]	> 100	100	365	3.2	8.4	5	69	0.87	1.36	10.43	0.59
This work[a]	120	100	545	18.2	0.9	2.12	89	2.09	0.38	115	1.02

[a]Simulated

[b]Fabricated (test chip)

illustrate the proposed amplifier excellency over previous works.

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