



Design analysis of high level inverter with EANFIS controller for grid connected PV system

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Abstract

For providing better reliability and getting minimal harmonics, multilevel inverters are commonly employed in grid connected photovoltaic systems. This paper presents 27 level inverter with reduced switch topology to get better reliability with low harmonics. This inverter performance completely relies on EANFIS controller which is the combination of ANFIS and Emperor Penguin Optimization (EPO) algorithm. Working procedure of ANFIS will be optimized by EPO to make us easy to deal MLI switching angle and produce harmonic-less control voltage. EPO provides efficient result by means of computational complexity, time and space complexity. In our work, this is the main reason to select EPO for optimizing ANFIS controller. The proposed work will be implemented in Simulink working environment. Resultant outcomes like inverter output, controller output and THD analysis will be compared with recently developed existing works.

Keywords Multilevel inverter · Harmonics · EANFIS controller · Emperor penguin optimization · Control voltage

1 Introduction

Role of multilevel inverters in numerous application like flexible AC transmission devices, grid interfaces, renewable energy system and medium voltage drives. Multilevel inverters have lot of advantages like electromagnetic interference, total harmonic distortion, and lower values of voltage on switches etc. [1]. It provides right way for average and high power system to synchronize the desired yield voltage that allow harmonic decrease in current and voltage waveform [2]. As a result, the output waveform quality increases and total harmonic distortion decreases are the main two benefits of MLI [3, 4]. It is one of the power electronic converter, from several levels of DC voltages multi-level inverter can synthesize the output voltage as input sources [5]. Multilevel refers to the multiple connection of individual inverters names as stage with required levels to provide the output voltage. A stair case

waveform can be synthesized based on proper pulse width modulation and identical voltage levels control of switching angles [6]. Through unique important series due to transferring operation of on and off the switching losses reduction in the inverter device is the major benefits of stair case output waveform. Moreover, in the stair case output voltage low order frequency harmonic can be observed with reduced switching frequencies. Increasing the demand of high power and high voltage and it is difficult to interface the power semiconductor switch [7].

The inverters are mainly divided into three categories. The first one MLI is neutral point clamped other is cascade and last is flying capacitor [8]. For big automotive electronic drives, the cascaded inverter is used. However, the necessity of increasingly number of switches and dispersed dc source for every cell turns into an issue particularly at larger amount [9]. Solar PV built schemes are presence as a main contributor to the current power production knowledge. To feed the produced power (DC) into grid (AC) is the main significant presentation of solar PV based power production. Solar photovoltaic panel have been among the quickest developing vitality source on the world. The PV scheme being additional gorgeous and likely green resources due to abundant availability, cost free, safe

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resources [10]. The PV elements directly changes light energy into electrical energy however energy gotten after the PV modules acts as small voltage dc source and has comparatively small transformation energy effectiveness [11]. The electronics power changes are utilized to change DC to AC to expand the effectiveness and change small voltage DC source to AC. Conventional topologies like current and voltage basis inverter are utilized to convert solar power generation [12]. Mostly, various literatures are fed in cascade multilevel inverter but it intends for low level and low voltage configuration [13]. For 5 and 7 level cascaded multilevel inverter Photovoltaic system is addressed with pulse width modulation technique [14].

In MLI topologies, flying capacitor wants only DC sources this is the real disadvantage, however it become famous if there should arise an occurrence of the framework PV on the grounds that for assembled solar based cells needs singular generator [15]. The structure of flying capacitor inverter is like that of clamped inverter diode yet the fundamental distinction is that as opposed to cinching diodes, flying Capacitors are utilized [16]. For eliminating low order frequency harmonics many approaches are focused, the method of selective harmonic elimination is widely preferred in multilevel inverter [17]. By solving non-linear transcendental equations characterizing harmonics to compute exchanging points the particular harmonic removal pulse width modulation exchanging systems can be utilized [18]. By assuming the proper initial guess to solve the non-linear transcendental equations resulting in multiple or one solution technique many iteration technique can be reported [19]. To estimate switching angles several traditional methods are used, however a few of them computationally expensive. The technique of soft computing like adaptive Neuro fuzzy inference system (ANFIS) and artificial neural network (ANN) and adapt to great diversity of data to estimate switching angles it can be excellent option [20].

Now a days, power generation from solar system is widely applicable in various fields like micro grids, fact devices, distributed generation systems. Such kind of transformer-less PV grid linked scheme is attractive due to their cost effectiveness, tiny size and reliability. Use of MLI in PV grid connected system to synthesize preferred output voltage from various level of DC input voltages. MLI produces stepped resultant voltage as clean sine wave to show minimization of THD. Traditional MLI topologies need separate driver circuits, individual DC sources for every stepped output. Especially in high power applications, failure of certain inverter portion contributes whole switching loss and power rating of inverter topology enhanced through reduction of switching frequency. But this condition leads to raise of current THD and which is very difficult to minimize. These findings says that,

minimization of switches, DC sources and gate drivers improves voltage levels. Raise in voltage level results better power quality with considerable reduction in size, THD and cost. This motivates us to make use of high level MLI with an optimized switching scheme for addition of PV grid connected scheme.

The remaining of research work is planned as follow, the next part gives certain examination of related works beside through the involvement of the proposed technique. The third section gives the brief explanation about the mathematical model of PV with MPPT, Buck converter, 27 level multi-level inverter with reduced switch and EANFIS controller that is the combination of ANFIS and EPO algorithm. The fourth part give evaluation of planned work through the Simulink platform. Conclusion of this work is given in last section with various proposal for upcoming work.

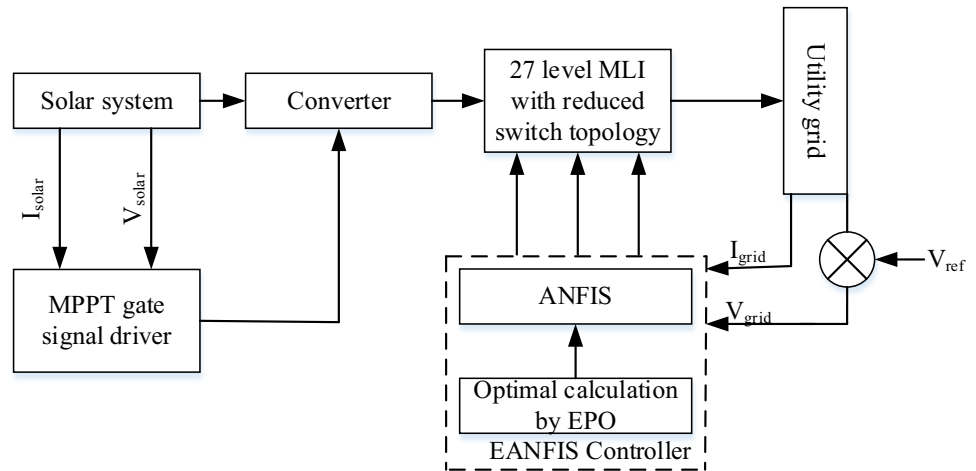
2 Related works

For selective harmonic elimination, a firefly assisted genetic algorithm was introduced by Priyanka et al. [21] in PV interfacing reduced switch multilevel inverter. This article provides an innovative 5-level MLI by utilizing less switch sum which is appropriate for separate PV scheme. Moreover, depends upon the method of selective harmonic elimination (SHE) a firefly assisted genetic algorithm (FAGA) is established to effectually controller and diminish the harmonics from the deliberate scheme. Through the FAGA procedure, the directed order of less harmonics was eradicated which obtained from yield voltage of recommended PV-MLI. An investigational evaluation setup is grown at last to approve the functioning of PV incorporated MLI through PWM control plot which is additionally contrasted and the conventional PWM control framework.

A swarm optimization-based improved excellent harmonic removal PWM method presentation was intended by Yatindra et al. [22] in Symmetrical H-Bridge Type Multilevel Inverters. To diminish the harmonics, an original variant swarm optimization (SO) based selective harmonic elimination (SHE) method is designated in MLIs that is a multifaceted optimization difficult connecting nonlinear mystical calculation. By the proposed algorithms, optimum switching angles are calculated considering minimum total harmonic distortion (THD) and the best outcomes are taken for controlling the operation of MLIs.

A compact switch cascaded mli with novel selective harmonic removal switch was presented by Kaibalya et al. [23] for Standalone Renewable Energy System. This article grants plan and device of a switched-diode double basis particular change MLI (SDDS MLI). By utilizing an

Fig. 1 Work flow



unequal simple unit, the comprehensive SDDS MLI was initially planned. Planned SDDS MLI needs fewer switch tally and the circuit of driver tally contrasted with the couple of as of late created RS MLI topologies. By evacuating coordinated low-course harmonics, an improved type of algorithm FSO was concentrated to improve the voltage quality for ascertaining best moving positions fundamental to gadget the SDDS MLI.

A Harmonic Study of PV-Fed Symmetric MLI was described by Maheshwari and Chandrasekaran [24] using Modified Artificial Neural Network. In a symmetric cascaded multilevel inverter-connected grid system, this article presents a control scheme to reduce the harmonics. It is controlled by modified artificial neural networks and genetic algorithm. The solar photovoltaic acts as input source and the output power is synchronized with grid. The switching angles are acquired such that the fundamental component of output voltage is kept steady and lower-order harmonics are limited or removed. The equipped system is coordinated with sun-oriented photovoltaic framework to decrease the harmonics.

A Harmonic Reduction for Grid-Connected Photovoltaic System based on Multilevel Inverter was introduced by Zeina et al. [25]. To reduce the harmonics of grid-associated photovoltaic (PV) scheme, this article examines the operation of Multilevel Inverter (MLI). MLIs act as a promising interface in medium voltage networks for many usages because their modularity and lower voltage stress towards the switches. In addition, they provide a high-form output with low symmetric deformation. It is proposed to use a Cascaded H-Bridge MLI (CHB-MLI) with network-linked PV systems since they require many sources on the DC side with phase shifted carriers pulse width modulation. The mission of these converts is to manufacture a staircase AC output voltage from numerous DC voltage stages.

3 Proposed methodology

The proposed work uses 27 level inverter with reduced switch topology to get better reliability with low harmonics. This inverter performance completely relies on EANFIS controller which is the combination of ANFIS and Emperor Penguin Optimization (EPO) algorithm. Working procedure of ANFIS will be optimized by EPO to make us easy to grip transferring position of MLI and make less harmonic controller voltage. Main concept of EPO based on huddling characteristics of emperor penguins. While comparing with other meta-heuristic algorithms, EPO provides efficient result by means of computational complexity, time and space complexity. This is the main reason to select EPO for optimizing ANFIS controller in our proposed work.

Diagrammatic flow of proposed work given in Fig. 1. Solar fed to 27 level MLI with minimize switch topology. Data required for EANFIS obtained by solving harmonic equations by considering various modulation indices. THD evaluated from output voltage generation of EANFIS controlled MLI. Main focus of EANFIS controller is to make inverter to harmonic free output voltage similar to grid voltage. Here, no essential of filter circuit to improve inverter output because of generation of harmonic less output at inverter side. Thus proposed EANFIS controller perform better in THD and reduce design complexity of whole system.

3.1 PV system model with MPPT

To monitor the multilevel inverters input voltage a novel controller is used and the grid voltage as reference magnitude to be employed by ANFIS with EPO algorithm. From a conventional phase-locked loop (PLL) the stage angle (θ_{grid}) of reference voltage is obtained to ensure the grid synchronization. Solar based radiation information is

gathered on a level surface. If the PV cluster is introduced confronting the sun the created control from PV framework could be expanded significantly. Numerous designs can be utilized as a part of this respect. The least expensive and least difficult to pick the annual finest tilt angle. The scope points of the site are the best angle edge; the PV exhibits tilted best-case scenario tilt edge, some different setups utilized two hub or one pivot sun followers to expand the created control after PV framework yet it builds the structure and cost complexities. To path the greatest power engendered from PV the most extreme power point trackers ought to be utilized. From the following equation the universal solar emission on the greatest gradient angle can be gotten.

$$G_{G, \text{titled}} = G_{\text{dir titled}} + G_{\text{diff titled}} + G_{\text{ref titled}} \quad (1)$$

where $G_{\text{ref titled}}$, $G_{\text{diff titled}}$ and $G_{\text{dir titled}}$ are the hourly reflected, diffused and direct emissions on the skewed surface. From hourly solar radiation values of these variables can be calculated on a horizontal surface. The improved radiation documents on a skewed surface and the hourly yield power from PV range is set by the below equation:

$$P_{pv} = P_R F_{pv} \left(\frac{\bar{G}_T}{G_{T, STC}} \right) [1 + \alpha p (T_C - T_{C, STC})] \quad (2)$$

where P_R represents the PV unit capacity, F_{pv} is denoted as PV unit de-rating factor, $G_{T, STC}$ is the event irradiance at standard conditions, G_T is represented by event irradiance on the skewed PV element, $T_{C, STC}$ is denoted by PV temperature under standard conditions, T_C is represented as PV temperature and αp is denoted as temperature coefficient of the power.

3.2 Buck converter

It changes unregulated DC supply into regulated DC voltage and its output is smaller than input. It is otherwise identified as step down converter. It comprises capacitor C , inductor L , a diode and a semiconductor switch. The load resistance is denoted by R and input voltage is represented by V_s . Figure 2 shows the converter of buck circuit.

If switch S is on condition, the inductor accumulate the energy that is $V_L i t_{on}$ and current equation and voltage equation can be expressed as follow,

$$\frac{di_L}{dt} = \frac{V_{in}}{L} - \frac{V_o}{L} \quad (3)$$

$$\frac{dV_c}{dt} = \frac{I_L}{C} - \frac{V_o}{R \times C} \quad (4)$$

If switch S is the condition of off, then the diode gets ON and provide a current flow path, the stored energy in the inductor will dissipate through load resistance. The

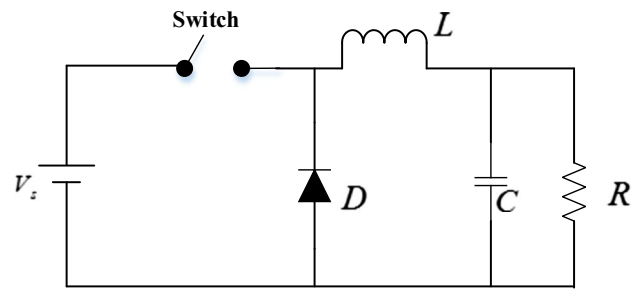


Fig. 2 Buck converter circuit

current equation and voltage equation can be expressed as follow,

$$\frac{di_L}{dt} = \frac{-V_C}{L} \quad (5)$$

$$\frac{dV_c}{dt} = \frac{I_L}{C} - \frac{V_C}{R \times C} \quad (6)$$

where V_C and I_L are considered to be two state of the system. The buck converter important uses is to manage the supply of DC power and control the DC engine speed. The yield voltage of the converter differs linearly with voltage control. For getting fixed DC voltage the output capacitor value is assumed to be very large for steady state analysis.

3.3 Cascade H bridge multilevel inverter

Figure 3 shows the circuit diagram of proposed cascade H Bridge MLI for single phase. It contains 3 cascaded H bridges with asymmetric voltage source feeding each H Bridge. 1:3:9 is the ratio of voltage source magnitudes. Between the ranges + 13 V and – 13 V, 12 switches are switched to produce different levels that are depicted in Table 1. Contingent upon the exchanging state of switches in the circuit, every one of the circuit comprise of four dynamic exchanging components that can make the yield voltage source in the positive or negative extremity, or it tends to be basically zero volts. Empirically when we give each voltage source as $V_{dc1} = 1V_{dc}$, $V_{dc2} = 3V_{dc}$, $V_{dc3} = 9V_{dc}$ then we will be able to get a 27 level output waveform ranging from + 13 V to – 13 including zero level. Output voltage of every H-bridge is equated as bellow:

$$V_{oi} = V_{dc} (S_{1i} - S_{2i}) \quad (7)$$

where $i = 1, 2, 3$ is represented by the amount of H-bridge inverter and $S_{1i} - S_{2i}$ is the higher switch of every filled bridge inverter. Eventually for the level of inverter 27 is represented by

$$V_{oN} = \sum_{i=1}^3 V_{oi} \quad (8)$$

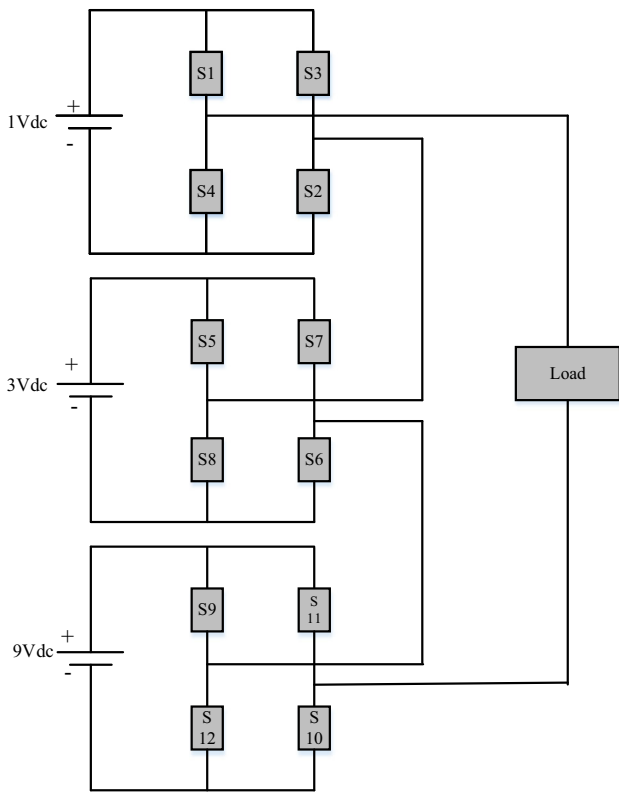


Fig. 3 Proposed cascade H bridge multilevel inverter

Multilevel inverters discover its well presentation by resources of less switching loss, better voltage, harmonic reduction and improved reliability on fault acceptance. Multi-level inverter decreases the procedure of flying capacitor, clamping diodes and heavy transformers. Later, cascade H Bridge MLI broadly applied in RES application because of the necessity of distinct DC source. In MLI amount of stages resulting waveform based on the amount of H-bridge component. There is continuous decrease in THD dimensions of MLI increments. The waveform of staircase is spoken to by yield voltage which shows switching angle and effects of harmonics.

Relationship among current and DC voltage should be analysed to make mathematical calculation for CHB. The *i*th cell (*S_i*) waveform modulation discovery by separating AC harmonics voltage $(V_{HI})_{Ac}$ with Dc voltage across capacitor of *i*th cell $(V_i)_{Dc}$.

$$S_i = \frac{(V_{HI})_{Ac}}{(V_i)_{Dc}} \tag{9}$$

$$\frac{dI_{in}}{dt} = \frac{1}{L} \left(\sum_{k=1}^3 S_i(V_i)_{Dc} - RI_{in} - V_G \right) \tag{10}$$

$$\frac{d(V_i)_{Dc}}{dt} = \frac{1}{C_k} (I_{battery,i} - S_i I_{in}), \quad i = 1, 2, 3 \tag{11}$$

where to discover dynamics of inverter current (10) and

Table 1 Switching operation for 27 level cascade H bridge multilevel inverter

Vout	1Vdc	3Vdc	9Vdc
+ 13Vdc	P	P	P
+ 12Vdc	0	P	P
+ 11Vdc	N	P	P
+ 10Vdc	P	0	P
+ 9Vdc	0	0	P
+ 8Vdc	N	0	P
+ 7Vdc	P	N	P
+ 6Vdc	0	N	P
+ 5Vdc	N	N	P
+ 4Vdc	P	P	0
+ 3Vdc	0	P	0
+ 2Vdc	N	P	0
+ 1Vdc	P	0	0
0Vdc	0	0	0
- 1Vdc	N	0	0
- 2Vdc	P	N	0
- 3Vdc	0	N	0
- 4Vdc	N	N	0
- 5Vdc	P	P	N
- 6Vdc	0	P	N
- 7Vdc	N	P	N
- 8Vdc	P	0	N
- 9Vdc	0	0	N
- 10Vdc	N	0	N
- 11Vdc	P	N	N
- 12Vdc	0	N	N
- 13Vdc	N	N	N

voltage (11) the parameters of grid voltage is V_G and inverter input current I_{in} . To get a determination for CHB variability problem phasor model of inverter activity spoken in (12).

$$\sum_{i=1}^3 \overrightarrow{S_i(V_i)_{Dc}} = V_G + (i\omega L + R)\overrightarrow{I_{in}} \tag{12}$$

From AC to DC (ρ_i) the power transmission will be estimated over multiplication of input current with harmonic voltage at ac side.

$$\rho_i = \overrightarrow{I_{in}} \times (V_h)_{Ac} \tag{13}$$

$$V_{MLI} = \sum_{n=1}^{\infty} (\mu_{on} \sin n\theta_n + \mu_{en} \cos n\theta_n) \tag{14}$$

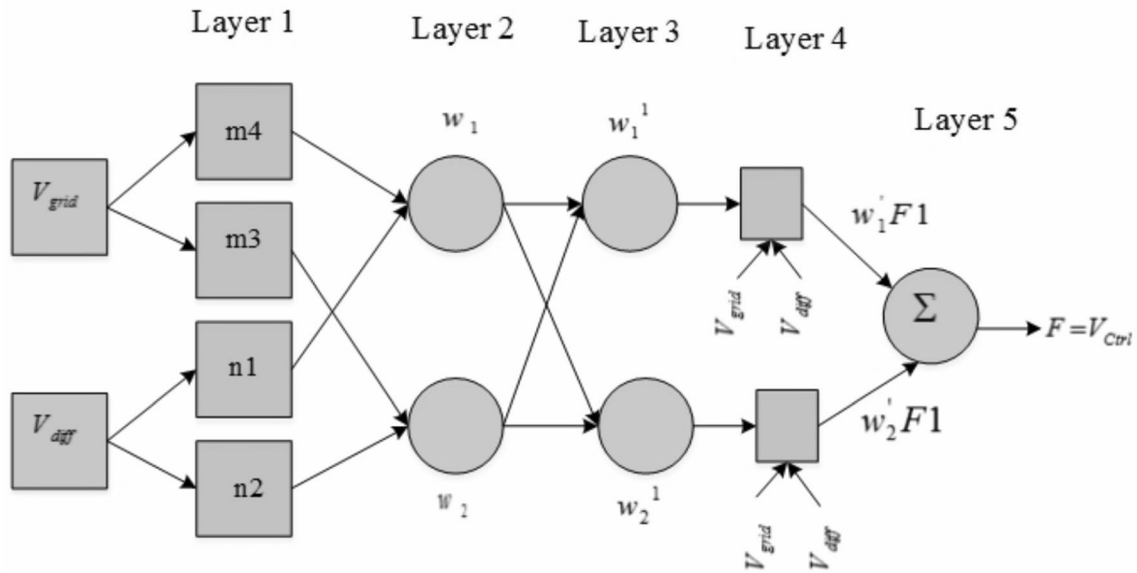


Fig. 4 ANFIS structure

$$\mu_{odd} = \frac{4}{n\pi} \sum_{n=1}^{\infty} V_{in}^n [\cos(n\theta_1) + \cos(n\theta_2) + \dots + \cos(n\theta_8)] \sin(n\omega t) \tag{15}$$

$$\mu_{Twenty\ Seven\ level\ CHB-MLI} = \sqrt{\frac{\sum_{k=2}^n (V_{MLI})^2}{V_{in}}} \tag{16}$$

where μ_{en} is denoted as even harmonics, μ_{on} is the representation of odd harmonics that is with output voltage (V_{MLI}) and input voltage (V_{in}) of MLI. To assemble MLI with switching angle θ the amount of bridges (n) is used and MLI without display even harmonics ($\mu_{en} = 0$). To direct current and voltage of the inverter each MLI configuration ought to have a controller device for desired applications to make it as without harmonic output. Design of proposed controller framework clarified in detail as pursues.

3.4 Proposed EANFIS controller

For twenty-seven level MLI, the present work uses the mix of EPO and ANFIS to make a controller plot. ANFIS displays the conduct of ANN and fuzzy that dispenses with the constraint of their individual use. It pursue the performance of feed forward back propagation network. If that target capacity isn't characterized the ANFIS achieve ideal arrangement quickly quicker than NN even. The error free outcomes and accomplish ideal arrangement quick are gotten by using ANFIS because of training the data. ANFIS design contains five layer, they are fuzzy layer, product layer, normalized layer, defuzzy layer and summation

layer. The parameter of ANFIS are determined with voltage and switching angle. The angle of switching increase with harmonics decline is through process of ANFIS controller. Consequently, to oversee ideal switching angles EPO calculation is utilized in proposed framework with harmonic reduction.

$$Objfun(fn) = \min(\mu_{Twenty\ Seven\ level\ CHB-MLI}) \tag{17}$$

Consider Eq. (17) as the objective function where μ represents THD of twenty-seven level CHB-MLI means. EPO work depend upon huddling behaviour of emperor penguin that is decomposed into four steps, first is produce and decide the cluster limit of emperor penguins, ascertain the temperature profile is the second condition, third is determine the distance between emperor penguin and fourth one is relocate the effective mover. Difference voltage (V_{diff}) and grid voltage (V_{grid}) are set as input to ANFIS and (V_{ctrl}) will be the production of ANFIS construction. It effortlessly alters its comments for guiding drive by using above factors. For solving several issues, the model of 1st order Sugeno fuzzy is the maximum used adaptive method with computational efficiency and high interoperability. The FIS guideline of Sugeno fuzzy model can be expressed as:

$$\begin{aligned} \text{Rule 1 : if } V_{grid} \text{ is } m1 \ \& \ V_{diff} \text{ is } n1 \ \text{then} \\ F1 &= U1V_{grid} + V1V_{diff} + W1 \\ \text{Rule 2 : if } V_{grid} \text{ is } m2 \ \& \ V_{diff} \text{ is } n2 \ \text{then} \\ F2 &= U2V_{grid} + V2V_{diff} + W2 \end{aligned} \tag{18}$$

where $m1, m2, n1$ and $n2$ are non-linear and $U1, U2, V1, V2, W1$ and $W2$ are direct parameters. Linear blend of

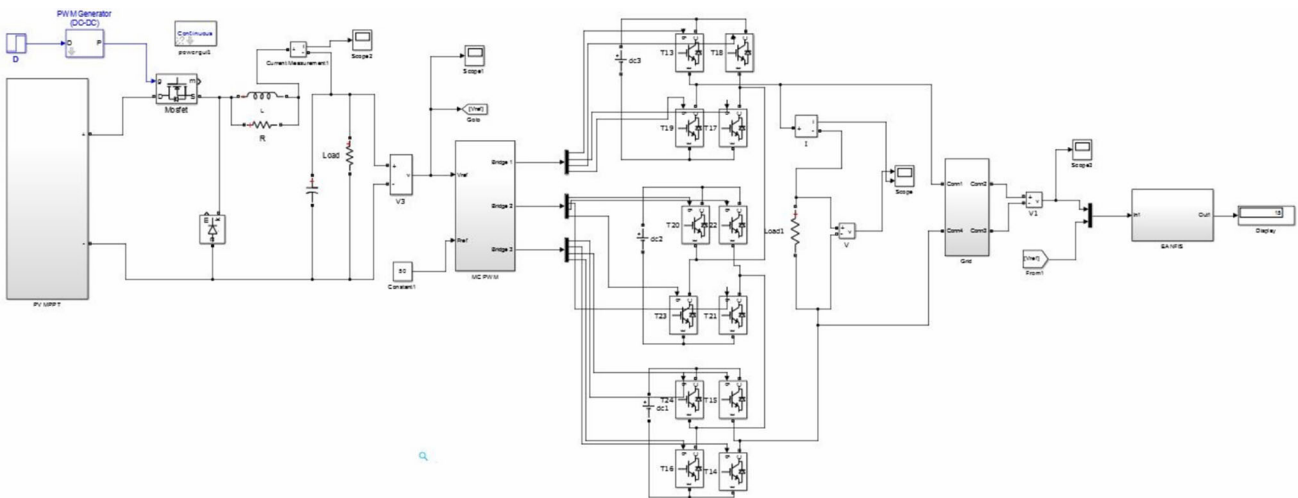


Fig. 5 Proposed simulink model

forerunner guidelines shapes individual outcome for each standard as condition (19). Layer 2 creates w_1 and w_2 that is standardized by layer third thus generate w_1 and w_2 separately. Figure 4 represents ANFIS construction to provide harmonic allowed voltage control.

$$F = UV_{grid} + VV_{diff} + W \tag{19}$$

Two sources of info (V_{grid} and V_{diff}) are set to semantic names of fuzzy theory in layer 1 (fuzzification) to separate membership functions as below.

$$\begin{aligned} L1_{out} &= \delta m_i(V_{grid}) \quad i = 1, 2 \\ L1_{out} &= \delta n_j(V_{diff}) \quad j = 1, 2 \end{aligned} \tag{20}$$

Equation (20) displays first ANFIS layer wherever fuzzy membership functions (MF) are $\delta m_i(V_{grid})$ & $\delta n_j(V_{diff})$. The layer of product is the second one (w_1 and w_2) that achieves legitimate AND operation of MF.

$$\begin{aligned} w_1 &\Rightarrow L2_{out} = \delta c_i(V_{grid}) \cdot \delta d_i(V_{diff}) \quad i = 1, 2 \\ w_2 &\Rightarrow L2_{out} = \delta c_j(V_{grid}) \cdot \delta d_j(V_{diff}) \quad j = 1, 2 \end{aligned} \tag{21}$$

The layer of normalization is (w_1' and w_2') that each nodes are stable demonstrating *if* measure of rule fuzzy.

Based on adaptive functioning pre-decided fuzzy standards is activity of de-fuzzification level.

$$\begin{aligned} w_1' &\Rightarrow L3_{out} = \frac{w_i}{w_1 + w_2} \quad i = 1, 2 \\ w_2' &\Rightarrow L3_{out} = \frac{w_j}{w_1 + w_2} \quad j = 1, 2 \end{aligned} \tag{22}$$

In fourth layer, the output of the every node is

$$\begin{aligned} w_1'F1 &\Rightarrow L4_{out} = \frac{w_i}{w_1 + w_2} [U1V_{grid} + V1V_{diff} + W1] \quad i = 1, 2 \\ w_2'F2 &\Rightarrow L4_{out} = \frac{w_j}{w_1 + w_2} [U2V_{grid} + V2V_{diff} + W2] \quad j = 1, 2 \end{aligned} \tag{23}$$

$$F = V_{ctrl} = \frac{\sum w_i'F_i}{\sum w_i} \quad i = 1, 2, \dots \tag{24}$$

ANFIS structure final result is determined utilizing then piece of fuzzy idea spoke to in (24). ANFIS routinely produce harmonic free control voltage once training is finished for different V_{grid} and V_{diff} . Planned work utilized the algorithm EPO for training ANFIS construction founded on Eq. (17). Here, we take certain amount of value for training process to control the voltage.

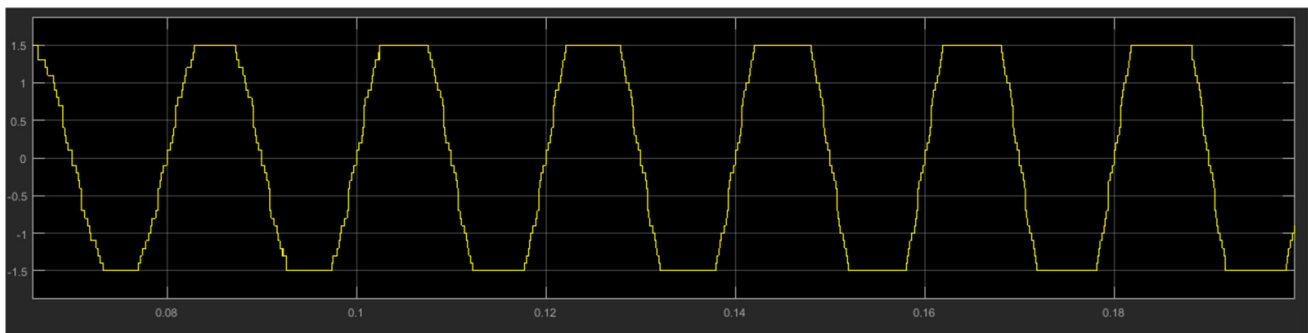


Fig. 6 Inverter current

$$V_{Ctrl} = \left(V_{grid} - \frac{Max_{iteration}}{x - Max_{iteration}} \right) \quad (25)$$

$$V_{grid} = \begin{cases} 0, & \text{if } V > 500 \\ 1, & \text{if } V < 600 \end{cases} \quad (26)$$

where V_{grid} is represented by grid voltage, x is represented as current iteration and $Max_{iteration}$ is denoted as the maximum number of iteration. So we take maximum range to minimum range of voltage for training process. Other voltage sources are eliminated with the condition. This make control the voltage very quickly in the iteration manner. In this manner the proposed work accomplish error free quick training of EANFIS, hence over-all effectiveness of work is enhanced.

4 Expected outcome

The proposed work will be implemented in Simulink working environment. Resultant outcomes like inverter output, controller output and THD analysis will be compared with recently developed existing works. Our proposed work is compared with existing PID and PI controllers. Figure 5 displays the proposed model of Simulink.

4.1 Inverter current

Figure 6 displays the performance of inverter current. By varying EANFIS controller, the inverter current performance are taken. By using this controller for tuning the purpose of the inverter we got stable inverter current. Our

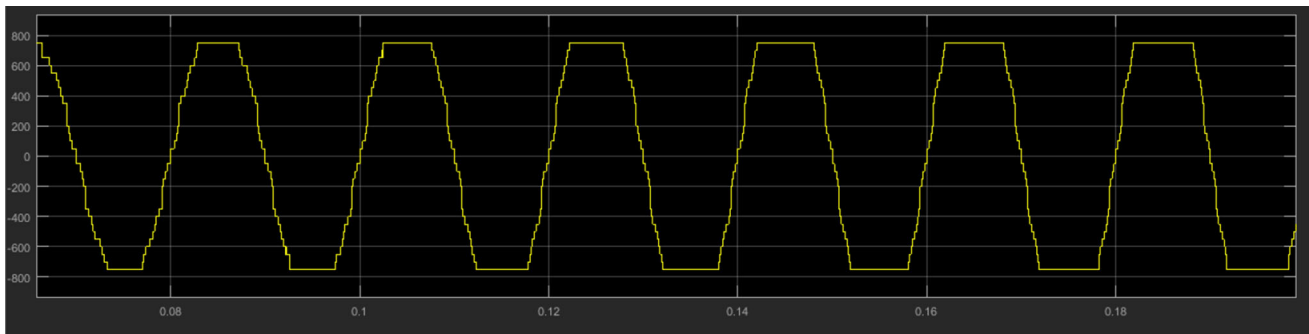


Fig. 7 Inverter voltage

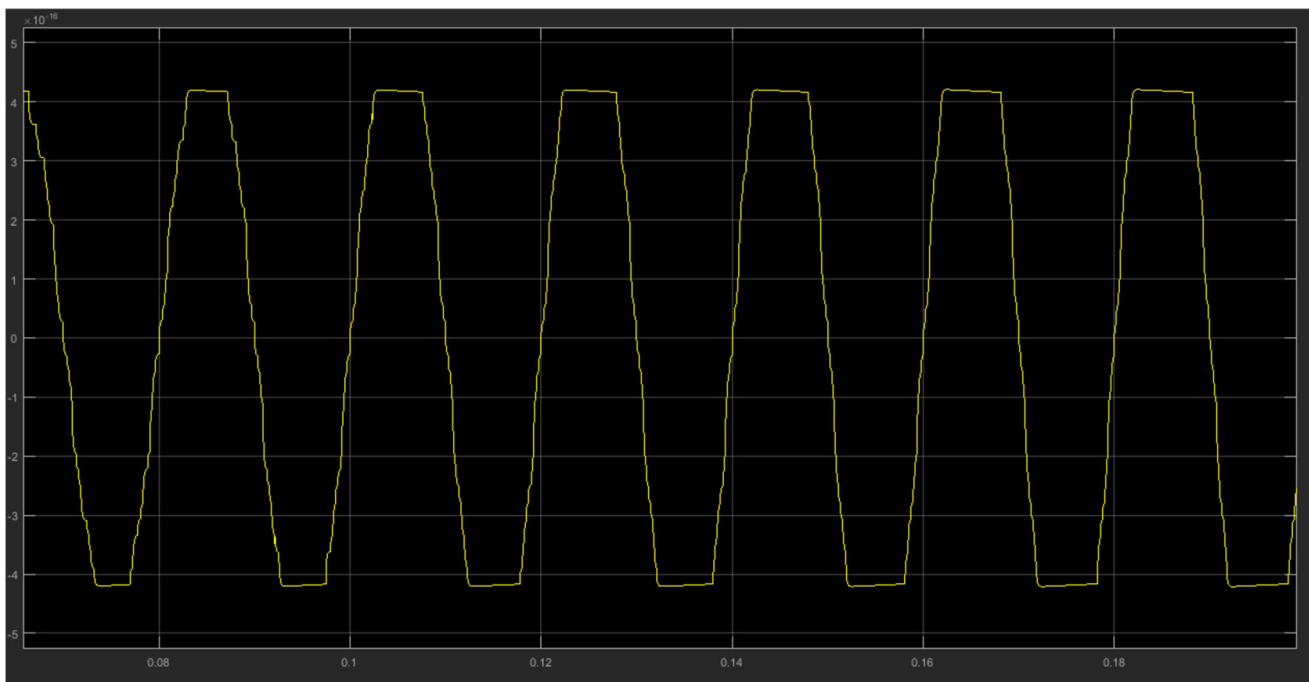


Fig. 8 Grid current

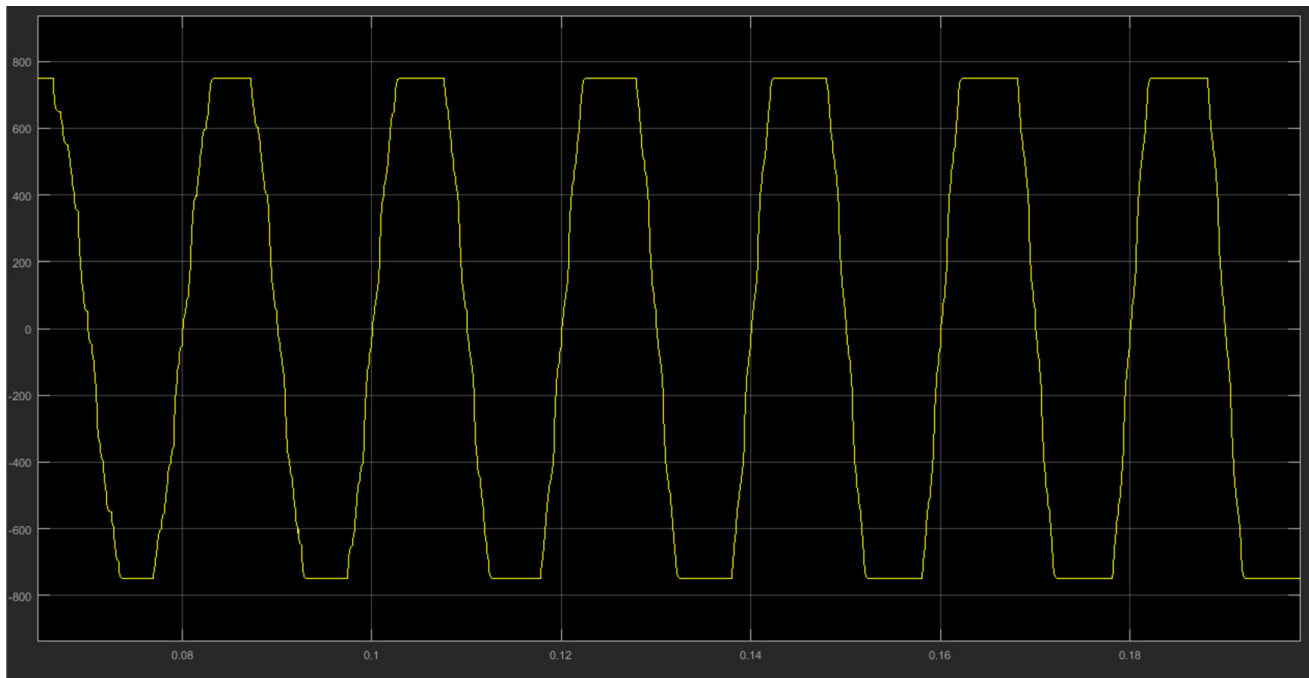


Fig. 9 Grid voltage

proposed method give better result give better results compared with others.

4.2 Inverter voltage

Figure 7 gives the performance of inverter voltage. By varying EANFIS controller, the inverter voltage performance are taken. By using this controller for tuning the purpose of the inverter we got exact inverter voltage. Our proposed method give better result give better results compared with others.

4.3 Grid current

Figure 8 shows the performance of grid current. By varying EANFIS controller, the grid current performance are taken. By using this controller for tuning the purpose of the inverter we got exact grid current. Our proposed method give better result give better results compared with others.

4.4 Grid voltage

Figure 9 shows the performance of grid voltage. By varying EANFIS controller, the grid voltage performance is taken. By using this controller for tuning the purpose of the inverter we got exact grid voltage. Our proposed method give better result give better results compared with others.

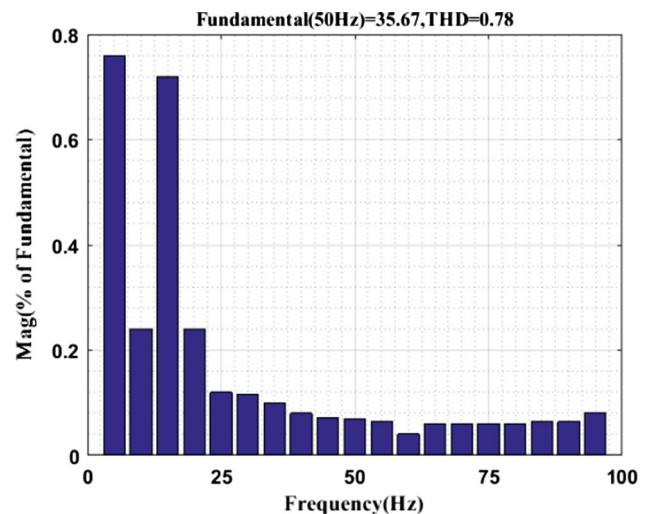


Fig. 10 THD performance

4.5 Total harmonic distortion

Figure 10 shows the performance of THD waveform for the yield voltage at the load side. In the proposed system the THD value in load side is 0.78%.

4.6 Existing PID-inverter current and voltage

Figure 11 shows the performance of existing PID controller of inverter current and inverter voltage. By varying PID controller, the inverter current and inverter voltage

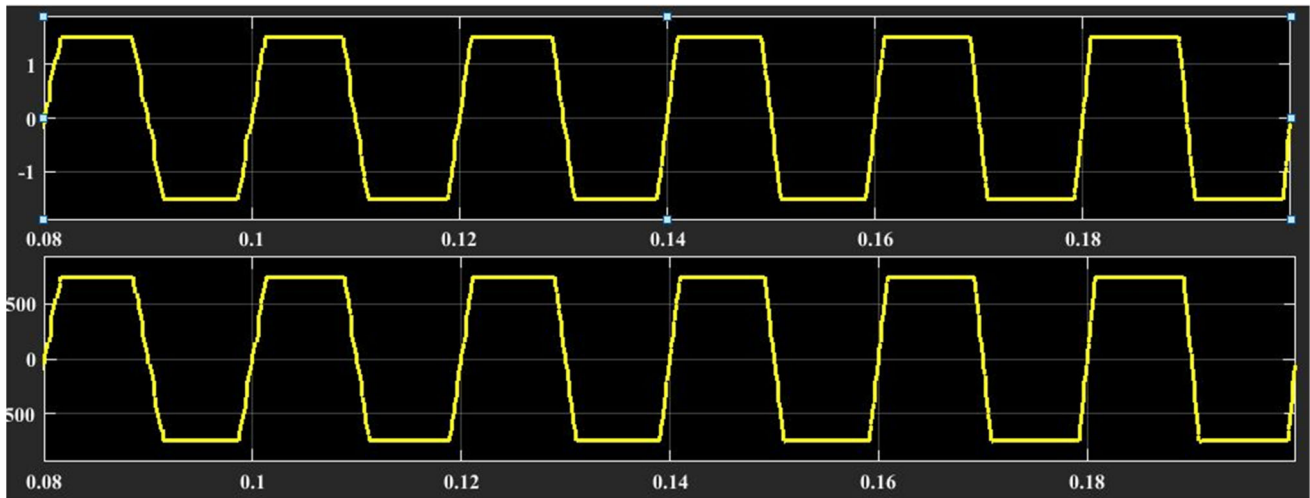


Fig. 11 Existing PID-inverter current and voltage

performance are taken. By using this PID controller we does not get the stable inverter current and inverter voltage performance.

4.7 Existing PID-grid current and voltage

Figure 12 shows the performance of existing PID controller of grid current and voltage. By varying PID controller, the grid current and voltage performance are taken.

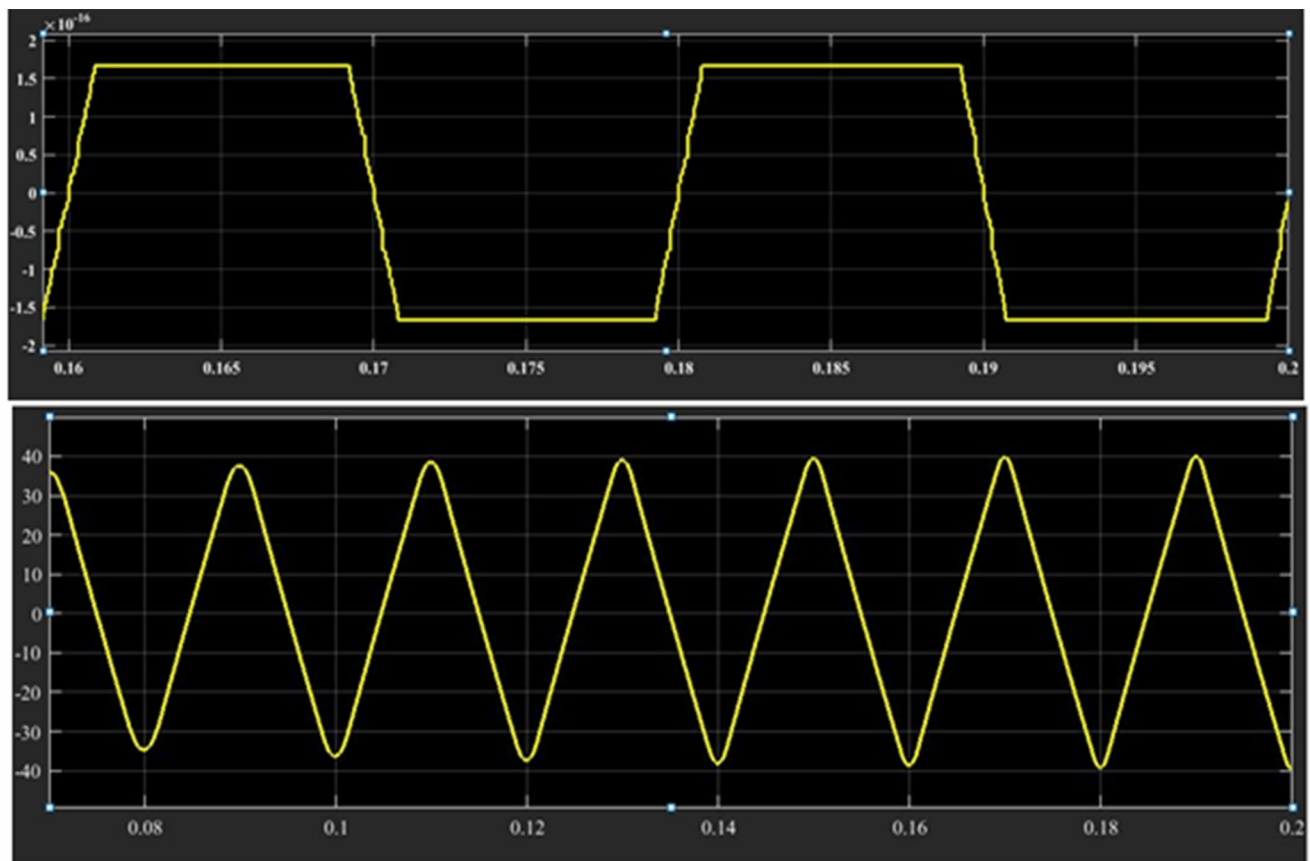


Fig. 12 Existing PID-grid current and voltage

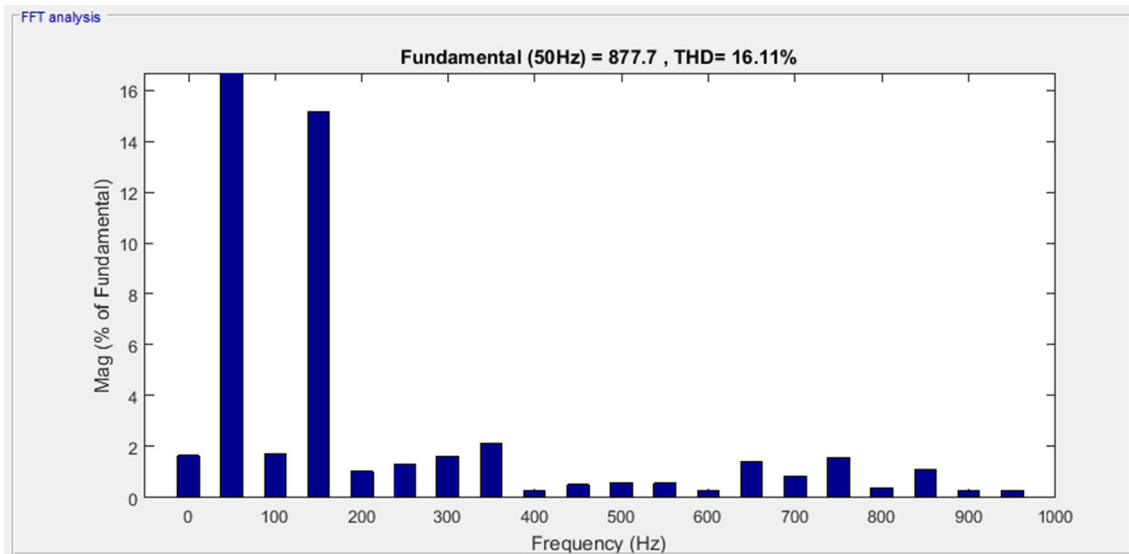


Fig. 13 Existing PID-THD

By using this PID controller we do not get the stable grid current and grid voltage.

4.8 Existing PID-THD

Figure 13 shows the performance of THD waveform for the yield voltage at the load side. By using existing PID controller the THD value of load side is 16.11%.

4.9 Existing PI-inverter current and voltage

Figure 14 shows the performance of existing PI controller of inverter current and inverter voltage. By varying PI controller, the inverter current and inverter voltage performance are taken. By using this PI controller, we do not get the stable inverter current and inverter voltage performance.

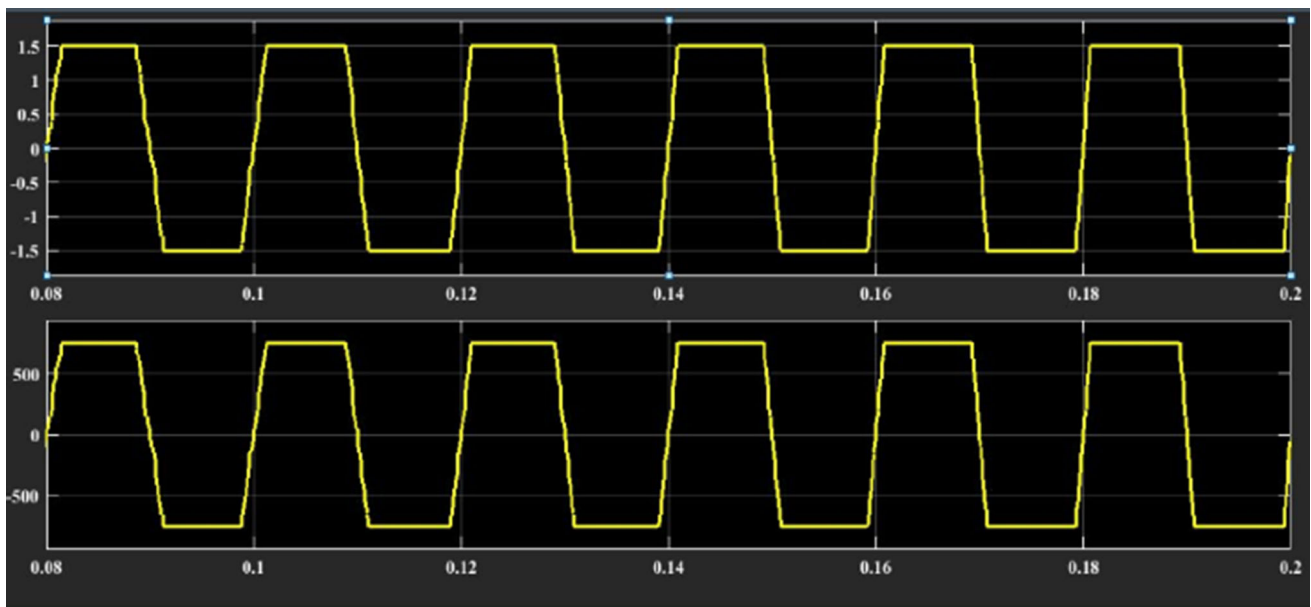


Fig. 14 Existing PI-inverter current and voltage

4.10 Existing PI-grid current and voltage

Figure 15 shows the performance of existing PI controller of grid current and voltage. By varying PI controller, the grid current and voltage performance are taken. By using this PI controller, we do not get the stable grid current and grid voltage.

4.11 Existing-THD

Figure 16 shows the performance of THD waveform for the yield voltage at the load side. By using existing PI controller, the THD value of load side is 18.19%.

Table 2 shows the comparison of THD. Here, by using our proposed controller the THD value is less because proposed controller reduces the harmonics and produce the exact output. The existing PID and PI controller are high THD value when compared with proposed THD. In this manner the proposed work accomplishes error free quick

training of EANFIS, hence total effectiveness of planned work is enhanced.

5 Conclusion

In this paper solar fed to 27 level MLI with minimize switch topology. Data required for EANFIS obtained by solving harmonic equations by considering various modulation indices. THD evaluated from output voltage generation of EANFIS controlled MLI. Main focus of EANFIS controller is to make inverter to harmonic free output voltage similar to grid voltage. The proposed work has implemented in Simulink platform. The expected outcomes like inverter current and voltage, grid current and voltage and THD analysis will be compared with recently developed existing works. Our work is compared with existing PID and PI controller. In future, the level of multilevel inverter is analysed in real time environments with the help of experimental setups.

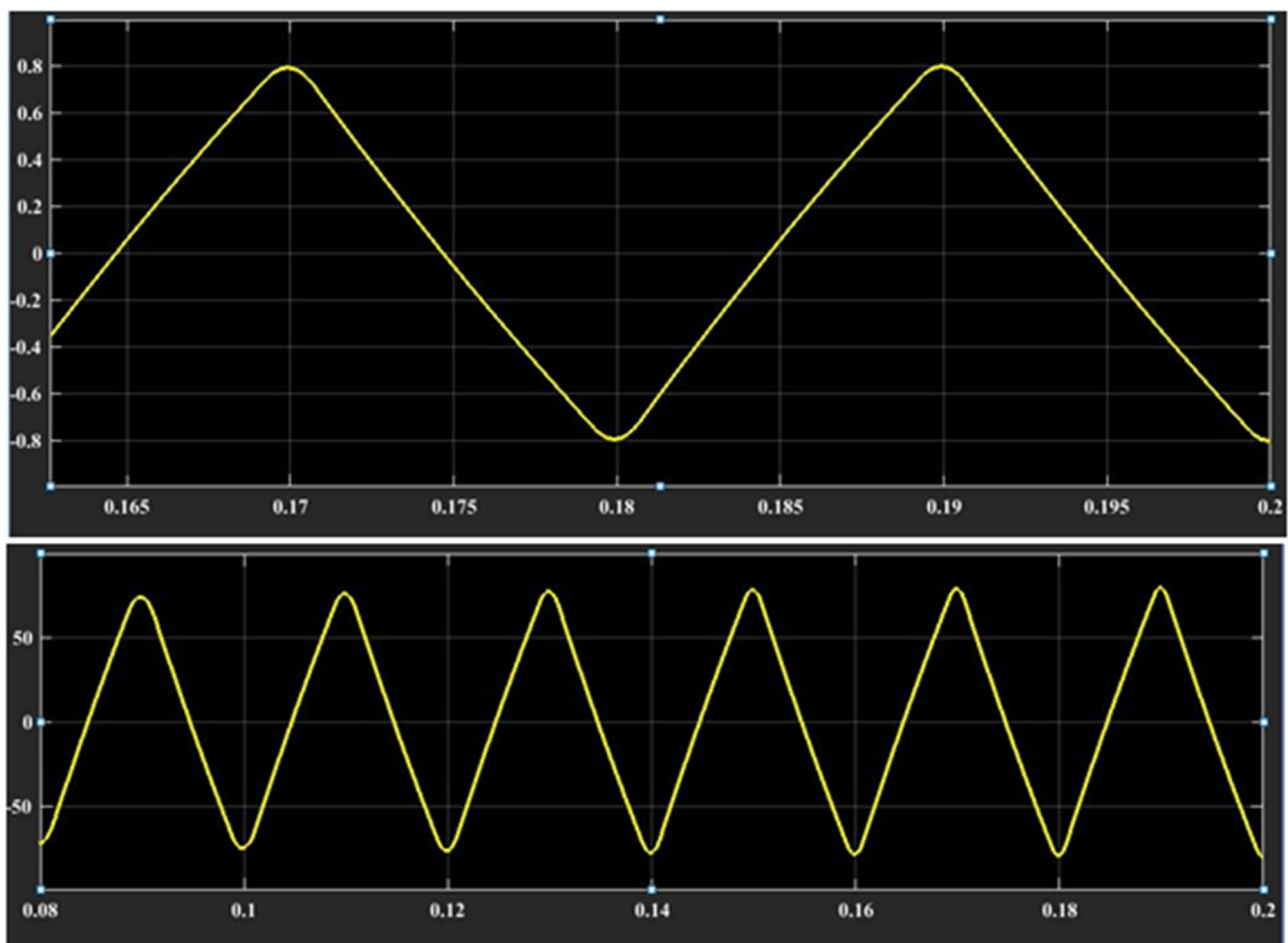


Fig. 15 Existing PI-grid current and voltage

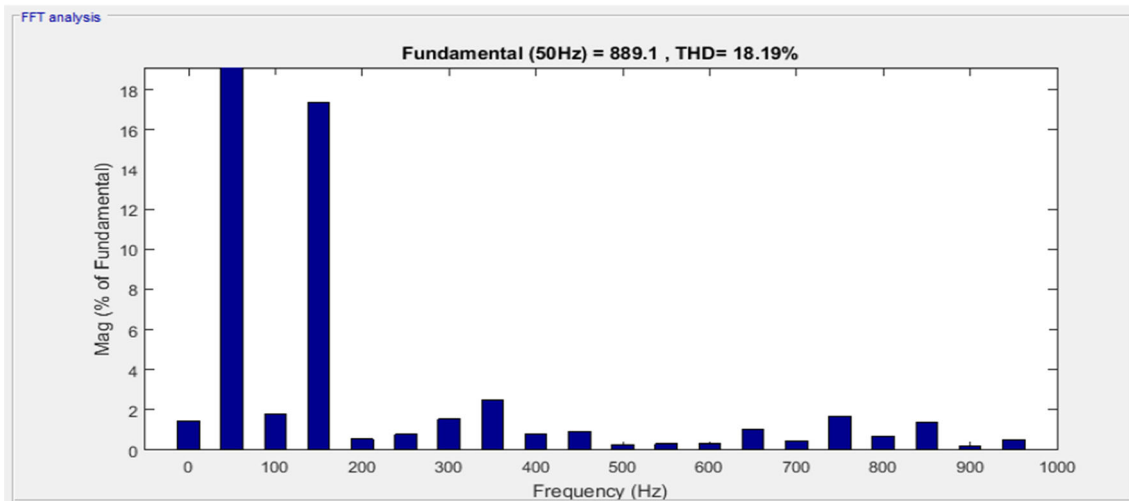


Fig. 16 Existing PI-THD

Table 2 Comparison of THD

S. no.	Controller used	THD%
1	PI	18.19
2	PID	16.11
3	EANFIS	0.78

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