Analog Integrated Circuits and Signal Processing (2020) 104:47–59
https://doi.org/10.1007/s10470-019-01575-y

A VDTA-based robust electronically tunable memristor emulator circuit

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Received: 21 January 2019 / Revised: 21 November 2019 / Accepted: 12 December 2019 / Published online: 23 December 2019
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Abstract

In this paper, a fully-integrated tunable grounded memristor emulator circuit based on voltage differencing transconductance amplifier (VDTA) has been proposed. The proposed memristor emulator circuit utilizes two VDTA active building blocks, two grounded resistors, a grounded capacitor and a four-quadrant analog multiplier. The working concept along with the detailed derivation of the mathematical model of the circuit has been discussed numerically and analytically to validate the operation of the proposed emulator. The operations of the proposed emulator circuit, as governed by the established model, have been verified by performing simulations in Cadence Virtuoso at 45 nm technology node. Robustness analyses performed, reveal significant process-variation tolerance at deep sub-micron technology node.

Keywords Voltage differencing transconductance amplifier · Memristor emulator · Memductance · Robustness

1 Introduction

The memristor, often attributed as the "*Missing Element*" was postulated by Chua [1]. This fourth circuital element serves to provide the missing link between flux and charge. The developed mathematical model of the memristor, depicted the memritor's unique property of retaining the value of its resistance. Further, the memristor was first fabricated in 2008 by using TiO_2, by Hewlett-Packard (HP) laboratory [2]. The capability of the device to provide nonvolatile memory functionalities has attracted the attention of the scientific community for its potential in diverse fields of application. The discovery of the device has significantly impacted the advancement in neuromorphic circuits and their applications by featuring promising results in providing implementable compact synapses in neural networks. Extensive amount of research in this field has brought forth new resistive RAMs [3] and adaptive transistors [4, 5] which portray promising results in developing neuromorphic systems that can imitate the brain.

The TiO_2-based memristor, as described by Strukov et al. [2] is uniquely characterized by a frequency-dependent pinched hysteresis loop in its *I–V* plot for sinusoidal excitations. The resistance of this two-terminal device depends on the voltage across its terminals or the amount of charge that has flowed through it. The operation of the memristor can be expressed mathematically by two non-linear functions $M(q)$ and $W(\varphi)$, which are referred as memristance and memductance respectively, [6] i.e.,

$$\frac{\delta\varphi}{\delta q} = M(q), \quad \frac{\delta q}{\delta\varphi} = W(\varphi), \tag{1}$$

where q is charge and φ is the flux.

From (1) we obtain a constitutive relationship between the memristor terminal voltage (v) and current (i), i.e.,

$$v = M(q)\cdot i, \quad i = W(\varphi)\cdot v \tag{2}$$

The relationships derived from (1) and (2) suggest that when φ–q curve is nonlinear, the resistance of the

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memristor will change with the variation in operating point $q = q_o$ at time t. The operating point (q_o) does not change without applying any external voltage or current, thus the resistance of the memristor or the memristance (M) remains constant and consequently the signal is memorized.

The characteristic pinched hysteresis dependence between voltage and current are depicted for sinusoidal periodic excitations at relatively low frequencies. However, with increase in the frequency of excitation, the area of lobes of the hysteresis curve decrease and the whole curve gradually approaches the shape of a straight line. Thereby, at higher frequencies of operation, the memristor behaves like a linear resistor. Such unique features owe to its nonlinear properties which impart immense potential in high performance and high-density memory technology.

Despite its potential for widespread utilization, the TiO_2-based memristor is still not commercially available as a result of technological difficulties and cost in fabrication of nanoscale devices. Recently, significant research work has been observed in the area of memristor emulator circuits which can mimic the unique properties of the TiO_2 memristor and are also physically realizable [7–18]. Authors in these papers have proposed new memristor emulator circuits by using active building blocks (ABBs) and a number of passive elements. However, these emulators are lacking in certain novel features like, electronically tunable characteristics, occurrence of pinching of the hysteresis loop at relatively low-frequencies, range of operation and low power consumption, etc.

This paper presents a memristor emulator using CMOS-based voltage differencing transconductance amplifier (VDTA) as an active building block, which imparts characteristics like electronic tunability, improved range of frequency of operation, lower power consumption. Integration of the design with other VLSI circuits, while maintaining a simple structure and compatibility of the memristor characteristics with CMOS technology are the key features of the proposed circuit. Table 1 summarizes a comparative study between the proposed emulator circuit and pre-existing memristor emulator designs. The proposed memristor emulator utilizes two VDTA active elements, three grounded passive elements (i.e., two grounded resistors, a grounded capacitor) and an active analog voltage multiplier. The remainder of the paper is arranged as follows. Section 2 describes the operation of the VDTA and illustrates the CMOS implementation of it; followed by Sect. 3, which features the proposed emulator circuit along with the detailed mathematical explanation of its operation. Section 4 presents the results of various analyses performed and provides a brief explanation of the characteristics obtained. Section 5 concludes the paper by summarizing the various observations obtained.

2 Circuit description of VDTA

The VDTA is a versatile active building block [19] that is primarily used for analog signal processing applications/circuit designing such as filter [20], oscillator [21] etc. This state-of-the-art analog building block is a transconductance amplifier with multiple outputs and has the capability of electronically tunable transconductances. The advantages of utilizing VDTA as an active device are as follows: (a) VDTA does not require the use of external resistors and are substituted by internal transconductances, (b) it exhibits two different values of transconductances, which are electronically controllable by external bias currents, (c) It has the capability of operation in voltage mode, current mode as well as transconductance mode as compared to other active devices reported (d) All the ports of VDTA exhibit high impedance, (e) VDTA-based filters allow independent controllability of resonant frequency and quality factor as compared to other active devices (f) VDTA-based designs also possess low active and passive component sensitivities. Further, no component matching conditions are also required for VDTA-based designs. Moreover, VDTA-based designs provide electronically tunable active synthesis.

The equivalent representation of the VDTA with transconductance amplifiers is shown in Fig. 1. This active building block has six- terminals (as in Fig. 1) which are labelled as p, n, z, zc, x^+, and x^-. It also has the flexibility of both voltage and current modes [19] of operation. The VDTA is composed of two cascaded transconductance amplifiers (T-I and T-II). The differential-input differential-output transconductance amplifier of the first stage (T-I) has two high impedance inputs terminals 'p' and 'n'; the terminal 'z' generates an output current (i_z) which is proportional to the difference in the voltages at two input terminals 'p' and 'n' (i.e., $v_p - v_n$). The voltage drop at the 'z' (v_z) terminal produces output current at the terminals 'x^+' and 'x^-' of the second transconductance stage (T-II). The currents at the terminals 'x^+' and 'x^-', are equal and opposite in directions. The 'zc' terminal is used for producing multiple copies of i_z. Figure 2 illustrates the CMOS realization of the VDTA [22]. The mathematical equations that govern the relationship between the terminals are given as follows,

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ g_{mf} & -g_{mf} & 0 \\ 0 & 0 & g_{ms} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix}, \tag{3}$$

where g_{mf} and g_{ms} are the first and second transconductances of the VDTA respectively and are termed as Arbel-Goldminz transconductances.

Table 1 Comparative literary survey between the proposed memristor emulator and pre-existing memristor emulator designs

References	Number of active components	Number of floating passive elements	Number of grounded passive elements	Power supply	Grounded or floating memristor emulator	Electronically tunable
Alharbi et al. [7]	STBM model: 2 CCII s (AD844), 2 TL084 s, 2 multipliers (AD633), 2 transistors (PN3565) TEAM model: 2 CCII s (AD844), 3 multipliers (AD633)	STBM: 4 resistors TEAM: 1 resistor	STBM model: 1 resistor, 1 capacitor TEAM model: 1 capacitor, 2 resistor	± 12 V	Grounded	No
Elwakil et al. [8]	2 CCII s (AD844), 1 buffer (TL082), 1 multiplier (AD633)	1 Resistor	2 Resistor, 1 capacitor	± 12 V	Grounded	No
Kim et al. [9]	2 Opamps, 1 multiplier, 10 transistors	1 Resistor	1 Resistor, 1 capacitor	± 5 V	Floating	No
Petrovic et al. [10]	1 VDTA, 1 multiplier (Total: 32 MOS transistors)	–	2 Resistors, 1 capacitor	± 0.9 V	Floating	Yes
Babacan and Kaçar [18]	1 OTA, 2 MOS transistors (Total: 16 MOS transistors)	–	1 Capacitor	± 1 V	Floating	No
Sánchez-López et al. [11]	4 CCII s (AD844), 1 multiplier (AD633)	2 Resistors	3 Resistors, 1 capacitor	± 10 V	Floating	No
Sánchez-López et al. [12]	2 CCII s (AD844), 1 multiplier (AD633)	1 Resistor	1 Resistor, 1 capacitor	± 10 V	Grounded	No
Ranjan et al. [14]	1 CCTA	1 Resistor	2 Resistor, 1 capacitor	± 1.5 V	Grounded	No
Sánchez-López et al. [15]	2 CCII s (AD844), 1 multiplier (AD633)	1 Resistor	1 Capacitor	± 10 V	Grounded	No
Cam and Sedef [13]	4 CCII + s, 1 multiplier	2 Resistors	2 Resistors, 1 capacitor	± 10 V	Floating	Yes
Yunus et al. [16]	1 MO-OTA, 1 multiplier	–	1 Resistor, 1 capacitor	± 1.25 V/ ± 5 V	Grounded	Yes
Sozen and Cam [17]	3 OTAs, 4 CCIIs	3 Resistors	3 Resistors, 1 capacitor	± 15 V	Floating	Yes
Proposed memristor emulator	2 VDTAs, 1 multiplier (total: 42 MOS transistors)	–	2 Resistors, 1 capacitor	± 0.9 V	Grounded	Yes

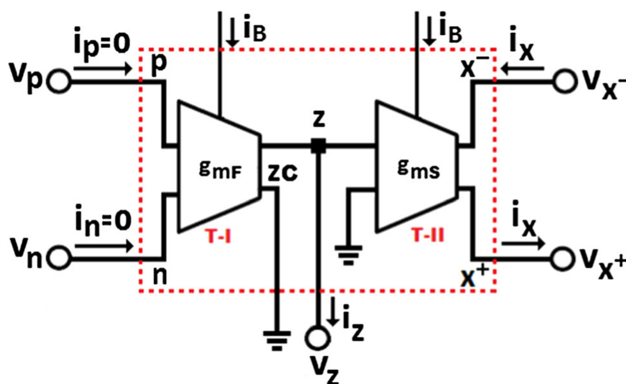

Fig. 1 Internal block diagram of the VDTA

The transconductances can be adjusted electronically by the external *DC* bias current i_B and are approximated as,

$$g_{mf} = \frac{g_{mp1}g_{mp2}}{g_{mp1} + g_{mp2}} + \frac{g_{mn1}g_{mn2}}{g_{mn1} + g_{mn2}}, \tag{4}$$

and

$$g_{ms} = \frac{g_{mp3}g_{mp4}}{g_{mp3} + g_{mp4}} + \frac{g_{mn3}g_{mn4}}{g_{mn3} + g_{mn4}}, \tag{5}$$

where g_{mni} and g_{mpi} are the transconductances of the *i*th NMOS and PMOS transistors respectively and is equal to,

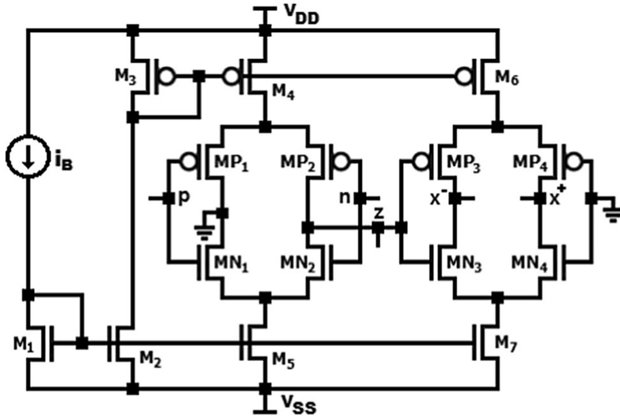

Fig. 2 Transistor-level representation of VDTA

$$g_{mni} = \sqrt{i_B \mu_N C_{ox}\left(\frac{W_{mni}}{L_{mni}}\right)}, \tag{6}$$

and

$$g_{mpi} = \sqrt{i_B \mu_P C_{ox}\left(\frac{W_{mpi}}{L_{mpi}}\right)}, \tag{7}$$

where i_B denotes the bias current; $\mu_{N,P}$ is the mobility of the carrier for transistors (N = NMOS, P = PMOS), C_{ox} is the gate-oxide capacitance per unit area and (*W*/*L*) is the aspect ratio for the MOS transistors. The value of *i* varies from 1, 2…, 4.

3 The proposed memristor emulator circuit

The proposed emulator circuit emulates the change in the resistance of the memristor with the change in the applied input signal. This circuit consists of a two VDTAs, two grounded resistors, one grounded capacitor, a four-quadrant analog multiplier. The block-level representation and transistor-level representation of the proposed emulator circuit are shown in Figs. 3 and 4 respectively. The proposed emulator is simple, fully integrated and utilizes only on-chip elements. Nevertheless, most of the reported emulator designs use an off-chip multiplier circuit which increases the cost, power, area and the structural complexity for the integration of the entire circuit. The proposed design uses a MOS-based four quadrant analog multiplier circuit which is based on Gilbert cell architecture [23].

The multiplier circuit based on Gilbert cell architecture is composed of three NMOS differential pairs, two NMOS active loads and one active biasing resistor. The CMOS circuit diagram of the four-quadrant analog multiplier is illustrated in Fig. 5. Transistor M_1, M_2 acts as active biasing resistor and draws current i_B from V_{DD}. Transistors M_3, M_4 form a current mirror and behave like a tail current source. Transistors M_5, M_6, M_7, M_8, M_9 and M_{10} form the three differential pairs for the applied differential inputs and transistors M_{11}, M_{12} behave as active loads.

As depicted in the schematic (Fig. 5), the symmetrical configuration of the circuit allows for large output voltage swings. Voltage signals (‘v_x’ and ‘v_y’) to be multiplied are applied to input terminals ‘x_p’, ‘x_n’ and ‘y_p’, ‘y_n’ respectively. The inputs ‘x_n’ and ‘y_n’ are complementary to ‘x_p’, ‘y_p’, respectively. Assuming that transistors M_5–M_{12} have identical value of β (i.e. $\beta = \mu_N \cdot C_{ox} \cdot W/L$), the output voltage of the multiplier can be expressed as,

$$v_{OUT} = \sqrt{2} \cdot \beta \cdot v_x \cdot v_y = \eta \cdot v_x \cdot v_y \tag{8}$$

where η is a constant for a definite value of β.

The operation of the proposed emulator can be explained mathematically by using the characteristic Eqs. (3) to (5). As shown in Figs. 3 and 4, $VDTA_1$ consists of ‘p_1’, ‘n_1’, ‘z_1’, ‘zc_1’, ‘x_1^+’, ‘x_1^-’ terminals and ‘g_{mf1}’, ‘g_{ms1}’ as the two transconductances. Similarly, $VDTA_2$ consists of ‘p_2’, ‘n_2’, ‘z_2’, ‘zc_2’, ‘x_2^+’, ‘x_2^-’ terminals and ‘g_{mf2}’, ‘g_{ms2}’ as the two transconductances. For $VDTA_1$, the current at the ‘x_1^-’ terminal (i_{x1}) is given by,

$$i_{x1} = g_{ms1} v_{z1} = g_{ms1} v_{fb}. \tag{9}$$

where v_{fb} is the feedback voltage from the analog multiplier.

For $VDTA_2$, Fig. 3 reveals the following at terminal ‘p_2’,

$$v_{in} = (i_{in} - i_{x1}) \cdot R_s = (i_{in} - g_{ms1} \cdot v_{fb}) \cdot R_s. \tag{10}$$

From (10), the input current (i_{in}) is related to the input voltage as,

$$i_{in} = \left(\frac{v_{in}}{R_S} + g_{ms1} \cdot v_{fb}\right). \tag{11}$$

Further analysis of $VDTA_2$ using (3)–(5), we obtain the voltage at ‘p_2’ terminal (v_{p2}, v_{n2} = 0) and the current at ‘z_2’ terminal (i_{z2}), v_{p2}, and i_{z2} are given respectively as,

$$v_{p2} = v_{in}, \tag{12}$$

and,

$$i_{z2} = g_{mf2} \cdot (v_{p2} - v_{n2}) = g_{mf2} \cdot v_{p2} = g_{mf2} \cdot v_{in}. \tag{13}$$

From (13), the voltage at the ‘z_2’ terminal (v_{z2}) can be obtained as,

$$v_{z2} = \frac{1}{C} \cdot \int i_{z2} \cdot dt = \frac{g_{mf2}}{C} \cdot \int v_{in} \cdot dt. \tag{14}$$

Thereby, from (3) and (14), the currents at the ‘x_2^+’ and ‘x_2^-’ terminals of $VDTA_2$ is given as,

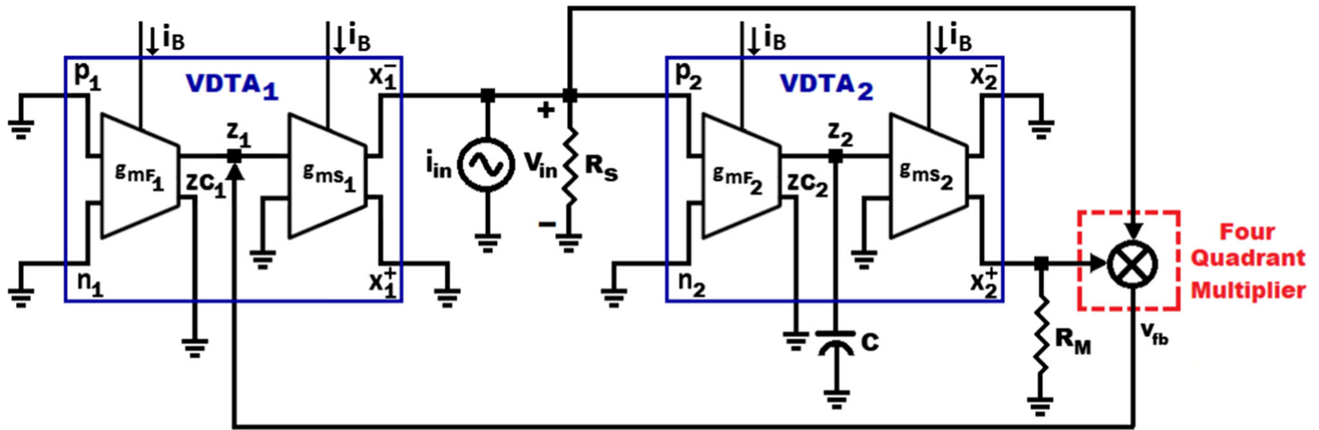

Fig. 3 Block level representation of proposed memristor emulator

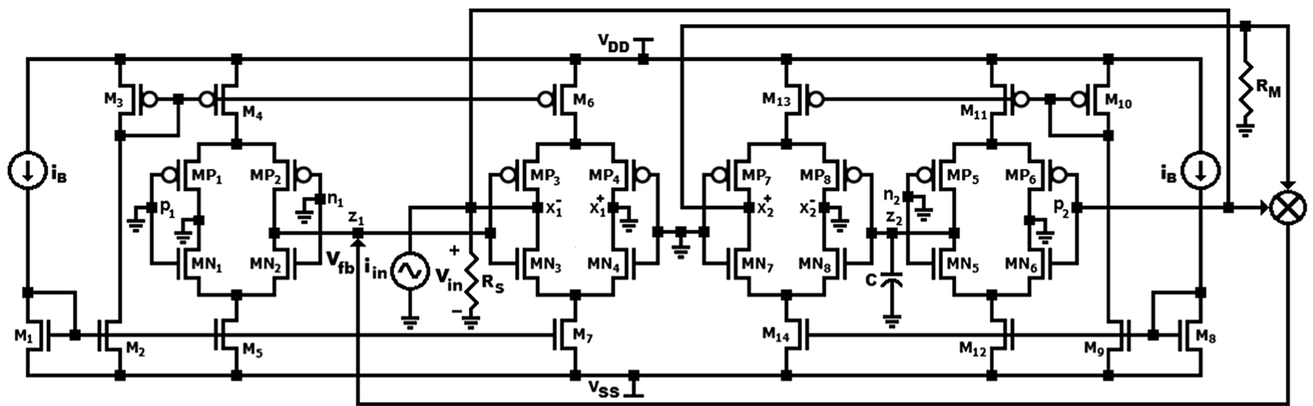

Fig. 4 Transistor level representation of proposed memristor emulator

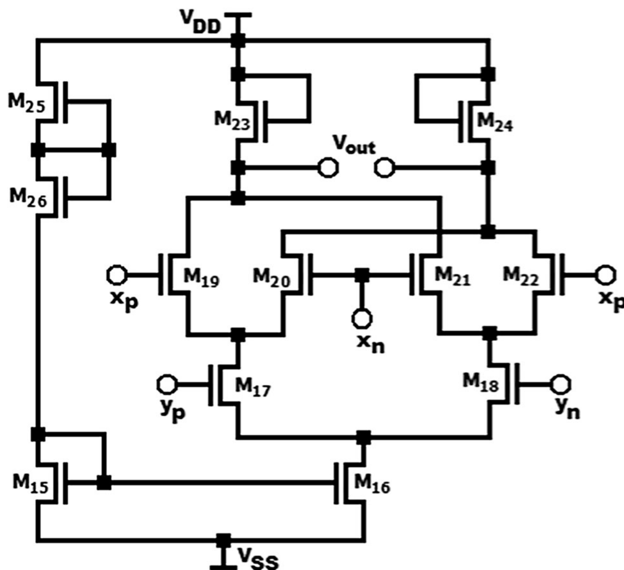

Fig. 5 Four quadrant analog multiplier incorporated in the proposed memristor design

$$i_{x2} = g_{ms2} \cdot v_{z2} = \frac{g_{ms2} \cdot g_{mf2}}{C} \cdot \int v_{in} \cdot dt. \tag{15}$$

Hence, from (15), the voltage at 'x_2^+' terminal (v_{x2+}) is as follows,

$$v_{x2^+} = i_{x2} \cdot R_M = \frac{g_{ms2} \cdot g_{mf2} \cdot R_M}{C} \cdot \int v_{in} \cdot dt. \tag{16}$$

The voltages drop v_{x2+} and v_{p2} are applied at the input of the four-quadrant analog multiplier to obtain the voltage (v_{fb}) at the output of the multiplier. The feedback voltage (v_{fb}), is obtained from (8), (12) and (16) and is given by,

$$v_{fb} = \eta \cdot v_{p2} \cdot v_{x2^+} = \frac{\eta \cdot g_{ms2} \cdot g_{mf2} \cdot R_M}{C} \cdot v_{in} \cdot \int v_{in} \cdot dt. \tag{17}$$

Substituting (17) in (11), the characteristic equation of the voltage-controlled memristor equation is revealed as,

$$i_{in} = v_{in} \cdot \left[\frac{1}{R_S} + \frac{\eta \cdot g_{ms1} \cdot g_{ms2} \cdot g_{mf2} \cdot R_M}{C} \cdot \int v_{in} \cdot dt \right]. \tag{18}$$

From (18), the memductance (G_M) of the proposed emulator circuit is given as,

$$G_M = {}^{i_{in}}/_{v_{in}}, \tag{19}$$

and,

$$G_M = \frac{1}{R_S} + \frac{\eta \cdot g_{ms1} \cdot g_{ms2} \cdot g_{mf2} \cdot R_M}{C} \cdot \int v_{in} \cdot dt. \tag{20}$$

For a particular case where the transconductances of both $VDTA_1$ and $VDTA_2$ are equal i.e. $g_{mf1} = g_{mf2} = g_{mf}$, and $g_{ms1} = g_{ms2} = g_{ms}$, the value of G_M from (20) is given by,

$$G_M = \frac{1}{R_S} + \frac{\eta \cdot g_{ms}^2 \cdot g_{mf} \cdot R_M}{C} \cdot \int v_{in} \cdot dt. \tag{21}$$

The dependence of G_M of the proposed memristor emulator on the bias current i_B is observed from Eqs. (4)–(7). The aforementioned equations govern the change in G_M for any change in i_B. Equations (20) or (21) suggest that, i_B can be utilized to modulate the memductance, thereby imparting electronically tunable nature to the proposed emulator.

4 Analysis and results

This Section presents the results obtained from our investigations.

4.1 Frequency behavior analysis

As established in the previous section, in Eq. (21), the proposed memristor emulator circuit depicts a tunable memductance whose value largely depends on the input voltage, 'v_{in}'. From Faraday's Law, we know that $\phi(t) = \int v(\tau) \cdot d\tau$. Therefore, Eq. (20) can be interpreted as,

$$i_{in}(t) = v_{in}(t) \cdot \left[\frac{1}{R_S} + \frac{\eta \cdot g_{ms1} \cdot g_{ms2} \cdot g_{mf2} \cdot R_M}{C} \cdot \int_{t_o}^{t} v_{in}(\tau) \cdot d\tau\right]. \tag{22}$$

Further, from Faraday's law, we obtain,

$$\phi_{in}(t) = \int_{t_0}^{t} v_{in}(\tau) \cdot d\tau, \tag{23}$$

and,

$$i_{in}(t) = v_{in}(t) \cdot \left[\frac{1}{R_S} + \frac{\eta \cdot g_{ms1} \cdot g_{ms2} \cdot g_{mf2} \cdot R_M}{C} \cdot \phi_{in}(t)\right]. \tag{24}$$

Thus, from (24), the memductance of the proposed flux-controlled memristor circuit can be presented as,

$$W(\phi_{in}(t)) = \frac{1}{R_S} + \frac{\eta \cdot g_{ms1} \cdot g_{ms2} \cdot g_{mf2} \cdot R_M}{C} \cdot \phi_{in}(t). \tag{25}$$

where $W(\phi_{in}(t))$ expresses the memductance function of the proposed memristor, which suggests that the memductance can be controlled by applying an input voltage. Further, Eq. (25) reveals that, ${}^{1}/_{R_S}$ is the time-invariant portion of the memductance $W(\phi_{in}(t))$.

The behavioral model of the proposed memristor derived in (25) can be used to gain an understanding of the frequency behavior of the circuit. In order to proceed with the study of frequency behavior of the emulator, let us assume that the proposed circuit is subjected to periodic sinusoidal excitations resulting in,$v_{in} = A_m \cdot \sin(\omega t)$; where, the amplitude is 'A_m', and the frequency of excitation is 'f' (which is given as,$\omega = 2 \cdot \pi f$). Therefore, we obtain,$\phi_{in} = -(A_m/\omega) \cdot \cos(\omega t)$. Substituting the expressions corresponding to the assumed excitation in (25), we obtain,

$$W(\phi_{in}(t)) = \frac{1}{R_S} - \frac{\eta \cdot g_{ms1} \cdot g_{ms2} \cdot g_{mf2} \cdot R_M \cdot A_m}{2\pi f \cdot C} \cdot \cos(\omega t). \tag{26}$$

Equation (26) reveals that, as the frequency of excitation ('f' or 'ω') gradually increases and approaches infinity, the time-varying portion of the memductance decreases and gradually approaches zero, thereby explaining the pinching effect of the characteristic hysteresis loop of the memristor emulator at very high frequencies. At high frequencies, the hysteresis loop pinches, areas enclosed by the hysteresis lobes decrease, and approaches the shape of a straight line. This behavior may be explained by (26), where the time-varying portion of $W(\phi_{in}(t))$ has a reduced overall contribution due to its inversely proportional relationship with 'f' (i.e.$(\eta \cdot g_{ms1} \cdot g_{ms2} \cdot g_{mf2} \cdot R_M \cdot A_m / 2\pi f \cdot C) \approx 0$, at very high frequencies of excitation). Hence, at high frequencies, $W(\phi_{in}(t))$ approaches the value of the time-invariant memductance, i.e.$W(\phi_{in}(t)) \approx 1/R_S$; this explains the pinching of the hysteresis loop to that of a straight line, suggesting the behavior of emulator as a linear time-invariant resistor. The relationship between the time-invariant and time-varying portions of $W(\phi_{in}(t))$, can be obtained from (26) as follows,

$$K = \eta \frac{g_{ms1} \cdot g_{ms2} \cdot g_{mf2} \cdot R_M \cdot R_S \cdot A_m}{\omega \cdot C} = \frac{1}{\tau \cdot f}, \tag{27}$$

where 'τ', is the time constant of the emulator circuit, and 'f' is the frequency of excitation. Further, from (27) the time constant of the proposed emulator circuit is given as,

$$\tau = \frac{2\pi C}{\eta \cdot g_{ms1} \cdot g_{ms2} \cdot g_{mf2} \cdot R_M \cdot R_S \cdot A_m}. \quad (28)$$

The frequency behavior of the proposed memristor emulator are governed by (27) and (28). The frequency analysis reveals three conditions relating K [in (27)] and the pinched hysteresis loop of $W(\phi_{in}(t))$. These conditions are delineated as follows:

i. $K \to 0$, when $f \to \infty$, the behavior of the memristor emulator is dominated by the influence of the linear time-invariant portion of memductance.
ii. $K \to 1$, when $f \to 1/\tau$, the emulator achieves the maximum pinched hysteresis loop.
iii. $K \geq 1$, when $f \leq 1/\tau$, the period of the excitation $(1/f)$ is greater than the time constant 'τ' of the proposed emulator circuit. This results in the loss of the hysteresis loop.

To ensure the behavior of the frequency-dependent pinched hysteresis loop, it can be concluded that, the value of K must lie in the range from 0 to 1, i.e.$0 \leq K \leq 1$. Further, the dependence of 'τ' on g_m shows that the time constant can also be varied by modulating the bias current i_B, thus tuning the characteristic hysteresis loop of the emulator circuit.

4.2 Analysis of simulation results

The proposed memristor emulator is simulated in Virtuoso Analog design Environment of Cadence at CMOS 45-nm *CMOS* process node. The supply voltage is taken as $V_{DD} = -V_{SS} = 0.9$ V. The transistor dimensions for the proposed memristor emulator are provided in Table 2. While conducting simulation analyses, all the VDTAs of the emulator have been identically biased with $i_B = 50$ µA. Thus, we have $g_{mf1} = g_{mf2} = g_{mf}$, and $g_{ms1} = g_{ms2} = g_{ms}$ and from (21), (26), (27) and (28) we obtain the following expressions,

$$W(\phi_{in}(t)) = \frac{1}{R_S} - \frac{\eta \cdot g_{ms}^2 \cdot g_{mf} \cdot R_M \cdot A_m}{2\pi f \cdot C} \cdot \cos(\omega t), \quad (29)$$

$$K = \eta \frac{g_{ms}^2 \cdot g_{mf} \cdot R_M \cdot R_S \cdot A_m}{\omega \cdot C} = \frac{1}{\tau \cdot f}, \quad (30)$$

$$\tau = \frac{2\pi C}{\eta \cdot g_{ms}^2 \cdot g_{mf} \cdot R_M \cdot R_S \cdot A_m}. \quad (31)$$

The emulator was subjected to a sinusoidal excitation of 1 kHz with an amplitude of 30 µA in order to examine the operation of the circuit. The input voltage and current, 'v_{in}', 'i_{in}' respectively, corresponding to the excitation are shown in Fig. 6. The transient responses of the proposed emulator are observed to be stable.

Further, Fig. 7 shows the frequency dependent pinched hysteresis loop for the same excitation, suggesting the stable operation of the circuit, where $0 \leq K \leq 1$ is satisfied and the memductance, $W(\phi_{in}(t))$ has a dominant time-varying nature. To obtain the frequency range of operation of the memristor emulator, the frequency 'f', was varied from 800 Hz to 10 kHz. The hysteresis loop exhibited a decrease in the lobe areas as 'f' increased and approached a straight line at 10 kHz. Such observations are illustrated in Fig. 8, which suggest the frequency range of operation to be from 800 Hz (f_{min}) to 10 kHz (f_{max}).

As emphasized in Sect. 4.1, the operation range $(0 \leq K \leq 1)$ of the memristor emulator circuit depends on the values of the different circuit elements [as in (29) and (31)]. Therefore, changing the values of the different circuital elements of the emulator can change the frequency range of operation. Table 3 enumerates the findings of such simulations by providing the different frequency ranges of operation for different values of i_B and C, while keeping the values of the resistances R_M, R_S, (1 KΩ each) and amplitude of excitation A_m constant.

Table 3 asserts the tunable nature of the proposed memristor emulator, where, by varying the i_B the operating frequency range of the circuit may be varied. Figure 9 illustrates the time varying nature of the memductance for sinusoidal excitation of, $A_m = 30$ µA, and $f = 50$ kHz. The

Table 2 Transistor dimensions

Transistor	Transistor type	Channel width (W) (µm)	Channel length (L) (µm)	Used in
M1/2/3/5/7/8/9/12/14	NMOS	3	0.18	Figure 4
M3/4/6/10/11/13	PMOS	3	0.18	Figure 4
MN1/2/3/4/5/6/7/8	NMOS	2	0.25	Figure 4
MP1/2/3/4/5/6/7/8	PMOS	2	0.25	Figure 4
M15/16	NMOS	5	0.25	Figure 5
M17/18	NMOS	10	0.18	Figure 5
MN19/20/21/22	NMOS	10	0.18	Figure 5
M23/24	NMOS	10	0.18	Figure 5
M25/26	NMOS	5	0.25	Figure 5

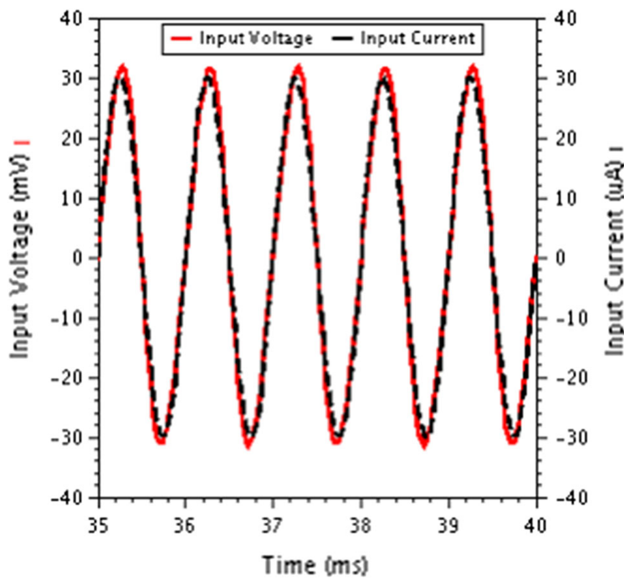

Fig. 6 The transient response of the proposed emulator to a sinusoidal excitation having amplitude of 30 μA and frequency of 1 kHz

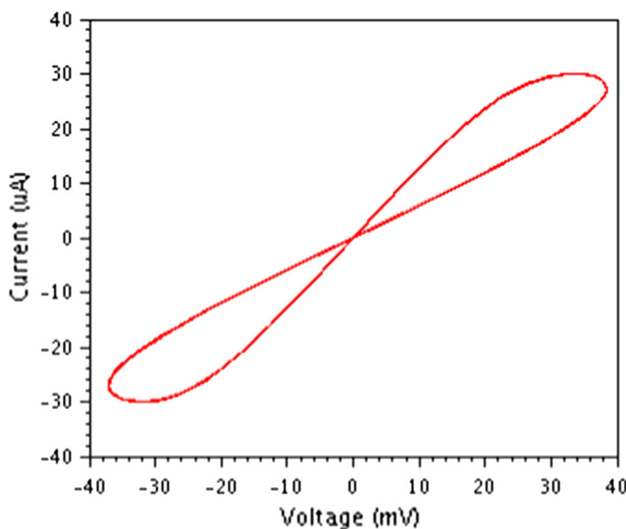

Fig. 7 Pinched hysteresis loop for the same excitation at a frequency of 1 kHz as in Fig. 5

power dissipation of the memristor emulator when subjected to such excitations, has been found to be 3.956 mW. Furthermore, the variation of memductance by varying i_{bias} is depicted in Fig. 10 for different frequencies of operation. Thus, the G_M and the frequency range of operation of the proposed memristor emulator can be tuned by the bias current.

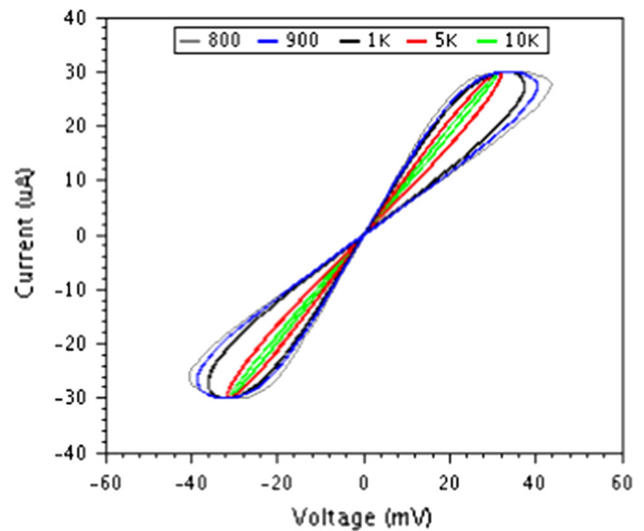

Fig. 8 Frequency depended hysteresis loop for excitations having an amplitude of 30 μA and frequency varying from 800 Hz to 10 kHz

Table 3 Tunable nature of the proposed memristor emulator

i_B (A)	C (F)	f_{min} (Hz)	f_{max} (Hz)
50 μ	10 n	800	10 K
50 μ	2.5 n	4.5 K	14 K
50 μ	1 n	13.4 K	20.3 K
55 μ	750 p	22.7 K	31 K
55 μ	250 p	36 K	42 K
60 μ	25 p	48 K	53 K

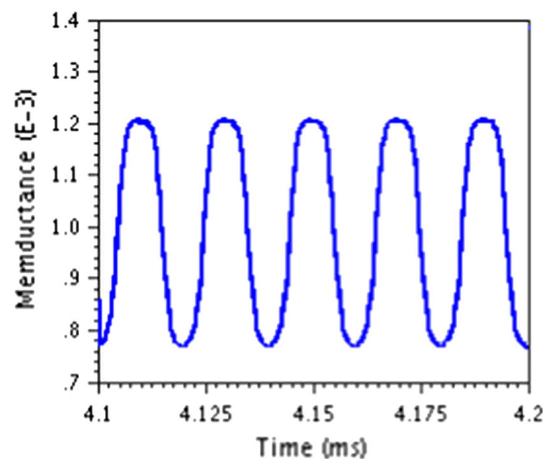

Fig. 9 Transient response of the memductance offered by proposed emulator for excitation of amplitude 30 μA and frequency 50 kHz

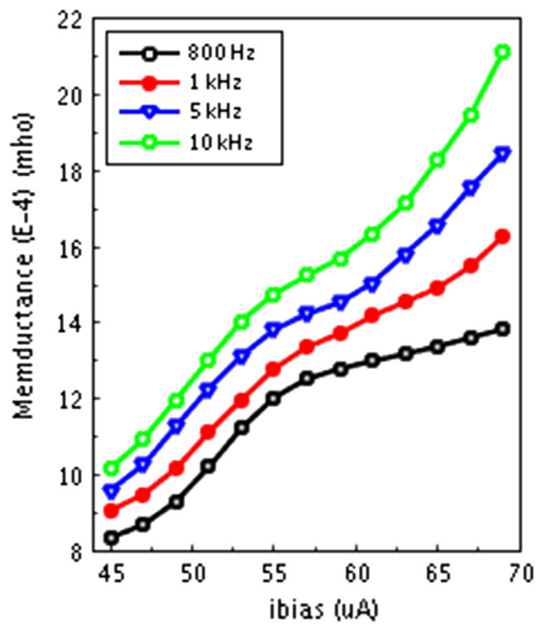

Fig. 10 The tunable nature of memductance offered by the proposed emulator circuit at $f = 800$ Hz, 1 kHz, 5 kHz, 10 kHz

4.3 Experimental results of proposed memristor emulator

This section presents the observations obtained from the experimental realization of the proposed memristor emulator circuit. The proposed VDTA based memristor emulator as in Fig. 3 has been implemented on breadboard using two commercially available LM13700 ICs, an analog multiplier AD633 IC, one capacitor (C) of 100 nF, two resistors of values 500 Ω (R_s), 5 kΩ (R_M), along with a DC supply source of ± 10 V and bias current of 1.35 mA. A single LM13700 IC is composed of two current controlled transconductance amplifiers. Therefore a single VDTA building block can be easily realized by utilizing one LM13700 IC [24, 25].

The two LM13700 ICs are used as there are two VDTA elements in the proposed circuit (Fig. 3) and they are connected via the analog multiplier, which is implemented by AD633 IC. The experimental setup is shown in Fig. 11, which illustrates the characteristic hysteresis loop obtained from the realized emulator circuit. Figure 12 illustrates typical pinched hysteresis loop and Fig. 13 shows the transient input voltage and current characteristics for an input waveform of amplitude 500 mV at a frequency of 1.46 kHz.

The voltage-current curves gradually become narrower as the operating frequency is increased. For this reason, the behavior of the proposed emulator is analyzed at 2 kHz, 3.6 kHz, 4.3 kHz and 5.5 kHz frequency regions, as depicted in Fig. 14. The governing expression (25) can objectively explain this phenomenon; with increasing operating frequency, the linear time-variant portion of (25) decreases, thus the memristor emulator approaches linear characteristics at higher frequency regions. The experimental results presented here, suggests the memrisitve characteristics of the proposed VDTA based emulator

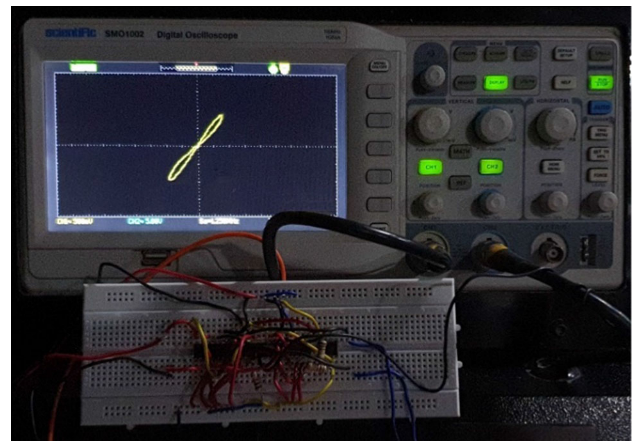

Fig. 11 Experimental setup consisting of the circuital realization of the proposed emulator on a breadboard, depicting the characteristic pinched hysteresis loop of a memristor obtained on a CRO

Fig. 12 Pinched Hysteresis loop of experimentally realized proposed memristor emulator circuit observed on CRO

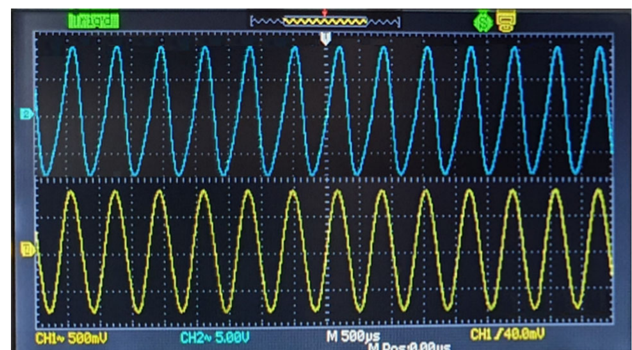

Fig. 13 Transient input voltage and current wave forms of experimentally realized proposed memristor emulator circuit observed on CRO

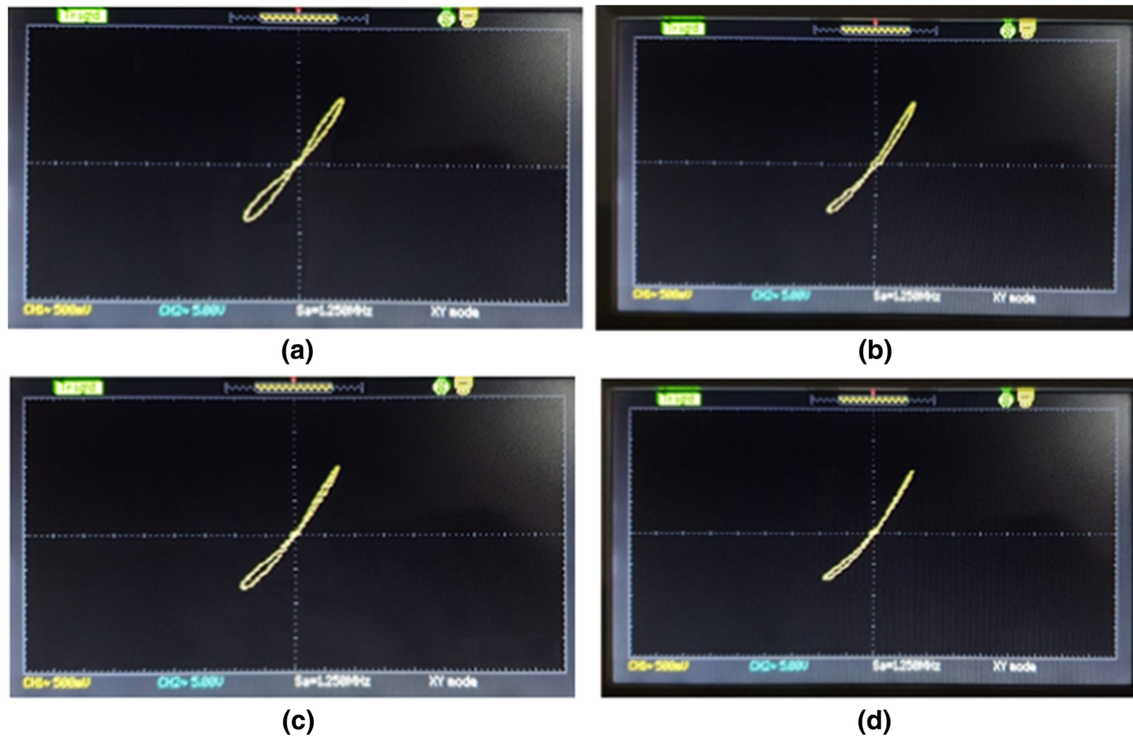

Fig. 14 Voltage-current hysteresis relationships for operating frequency of **a** 2 kHz, **b** 3.6 kHz, **c** 4.3 kHz and **d** 5.5 kHz

circuit with variation in operating frequency. The simulation and exhaustive theoretical analyses along with the observations made in the experimental analyses reveals the feasibility of memristive behavior of the proposed emulator circuit in a packaged integrated MOS realization.

4.4 Reliability of proposed memristor emulator

Memristors exhibit unique nonvolatile memory characteristics, however they are profoundly impacted by variability, especially at highly scaled technology nodes [26, 27]. This has a profound impact on their operation especially at highly scaled technology nodes. With the current trends in aggressive scaling in order to keep up with the projections of Moore's Law, it is important for memristive systems to retain their functionality even when subjected to extreme variations in device parameters. Keeping in view the importance to mitigate the impact of device variability, a study has been conducted to analyze the robustness of the proposed VDTA-based memristor emulator design.

The robustness of the proposed emulator has been assessed by subjecting the design to process variability. Due to the continued miniaturization of the MOS devices, process variation has a significant impact on performance of the circuit. Random variations in the wafer fabrication process, which include both intra-die and inter-die factors [28]; are responsible for variability in VLSI devices. Thus, the variation of any parameter x is,

$$\sigma_x = \sigma^2_{x,intra-die} + \sigma^2_{x,inter-die}. \tag{32}$$

Process sensitive MOS device parameters like the doping concentration N_{CH}, channel length L, gate oxide thickness t_{ox}, channel width W, and etc. are major contributors to process variability. Further, at highly scaled deep-submicron technology nodes, oxide thickness variations (*OTV*), metal-gate work-function fluctuation (*WKF*), random dopant fluctuation (*RDF*), line-edge and line-width roughness (*LER*, *LWR*) are sources of intrinsic variability [29]. To model such fluctuations the device parameters like L, W, t_{ox} are considered to have independent Gaussian distributions with 3σ variations of ± 10% as projected by the guidelines of the International Technology Roadmap for Semiconductor Industry (*ITRS*) [30]. The influence of the aforementioned device parameters has a correlated impact on the threshold voltage V_t of the *MOS* device, hence due to the statistical interdependence of the fluctuating components the total variation in V_t can be estimated by [29],

$$(\sigma V_{t,total})^2 \approx (\sigma V_{t,RDF})^2 + (\sigma V_{t,WKF})^2 + (\sigma V_{t,PV})^2, \tag{33}$$

where $\sigma V_{t,total}$ is the total fluctuation in V_t, $\sigma V_{t,RDF}$ is the fluctuation due to *RDF*, $\sigma V_{t,PV}$ and $\sigma V_{t,WKF}$ are the fluctuation components due to process variation- induced fluctuation in V_t and work-function respectively.

Hence, the overall impact of process variations resulting in device parameter fluctuations can be approximated by

applying Gaussian distribution with 3σ variations of $\pm$ 10% only on the device threshold voltage V_t [31].

Monte Carlo simulation of 5000 iterations was carried out by applying Gaussian distribution to V_t and the memductance (G_M) of the proposed memristor emulator was estimated. The overall impact of such variations can be estimated by Pelgrom's Law [32] related to the current factor (β),

$$\frac{\sigma^2(\beta)}{\beta} = \frac{\sigma^2(L)}{L} + \frac{\sigma^2(W)}{W} + \frac{\sigma^2(C_{ox})}{C_{ox}} + \frac{\sigma^2(\mu_n)}{\mu_n}. \quad (34)$$

At deep-submicron CMOS technologies, the carrier mobility (μ_n) saturates above the critical electric field (E_c) and very miniscule impact on the variation of β. Further, according to Pelgrom's Law [32], the variance in any parameter P (ΔP) can be determined as,

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 \cdot D_x^2, \quad (35)$$

where D_x is the separation between the matched devices and the area and spacing proportionality constants for P are represented as A_P and S_P respectively. From (35), the generalized expressions for variation in G_M may be modeled as,

$$\sigma^2(G_M) = \sum_i \left(\frac{\partial G_M}{\partial x_i}\right) \cdot \sigma_{x_i}^2, \quad (36)$$

where σ_{x_i} is standard deviation of the device parameter x for the ith device.

The yield distribution for the meductance G_M has been illustrated in Fig. 15. It is observed from Fig. 15 that there is a standard deviation (σ) of 97.079 μ℧ around the mean (μ) 1.11624 m℧, resulting in variability (σ/μ) of 0.08697.

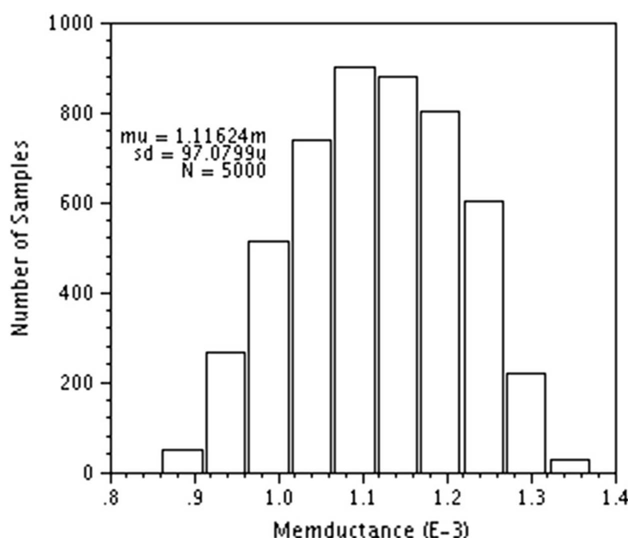

Fig. 15 Yield distribution for the memductance of the proposed emulator circuit for a Monte Carlo simulation of 5000 iterations

A limited spread in memductance value of the emulator circuit translates into a narrow spread in other design metrics of the memristor emulator, thereby validating the proposed design to be variation aware.

5 Conclusion

A novel memristor emulator circuit utilizing VDTA as active building elements is presented. The proposed emulator circuit consists of one grounded capacitor, two grounded resistors, one four quadrant analog multiplier, and two VDTAs. The circuit presented offers a simple circuit-topology, with fully integrated configuration, low power consumption, and tunable capability by which the characteristics of the emulated memristor can be varied electronically. The mathematical model for the proposed memristor emulator has been established in order to explain the characteristics and novel features of the circuit. Thorough analyses have been performed at CMOS 45 nm technology node using Virtuoso Analog Design Environment of Cadence, whose findings reported in this paper, reveal that the proposed emulator circuit is robust and variation-resilient to fluctuations in process parameters at deep-submicron technology nodes.

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