



Applying design equations in particle swarm optimization for auto-sizing of multi-stage opamps: an experimental study

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Abstract

This paper presents an experimental study on using analytical design equations in the particle swarm optimization (PSO) for the automatic sizing of multi-stage operational amplifiers (opamps). Differing from the existing research, this work incorporates design equations in the PSO search process in attempt to reduce the search space dimensionality and the number of PSO iterations without sacrificing the quality of search results. Design equations are approximate characterization of the opamp performance metrics in analytical form, which are widely used in manual design process. However, the opamp device sizes cannot be uniquely solved from a set of design equations. Heuristic search can serve as a local optimizer in a reduced-dimensional search space to further refine optimization. Extensive simulation-based experimental PSO search results are presented to demonstrate the effectiveness of the proposed auto-sizing tactic. An alternative genetic algorithm based search method is implemented as well and tested for comparison.

Keywords Auto-sizing · Design equation · Genetic algorithm (GA) · Multi-stage opamp · Operational amplifier (opamp) · Particle swarm optimization (PSO) · Relaxation iteration (RI)

1 Introduction

With continuous down-scaling of the advanced semiconductor process technology, the gain achievable by single or two-stage operational amplifiers (opamps) becomes inadequate. In the past two decades we have witnessed an increasing number of publications on the design of multi-stage opamps, mainly three-stage amplifiers, see for example [1–4] and the references therein.

Amplifier design starts from selecting a proper circuit topology to meet design requirements. Having selected a circuit topology, the designer would spend quite an amount of time on circuit sizing.

For multi-stage circuits, compensation is another important part of design. Compensation design is closely

related to design equations, which can be derived manually by analyzing a stage-form macromodel. Several research papers have outlined analytical design procedures for CMOS amplifier sizing [5, 6]. Some other authors have introduced graphical design procedures for analyzing compensation strategies [7, 8]. No matter by an analytical approach or a graphical approach, design equations always play important roles in the process of design reasoning.

While design equations can help reasoning during the design of a compensation network, they are also useful in determining device sizing. Based on a systematic calculation procedure, rough device sizes can be determined although they are not necessarily the final device size values [5, 6]. Nevertheless, design equations can play the role of constraints that can effectively reduce the blandness in optimizing the circuit sizing.

Several reference sizing procedures have been proposed in the literature, such as analytical design equation based calculation procedure [5, 6] or *gm/ID* based sizing strategy [9]. However, all these sizing strategies cannot determine the device sizes of an amplifier in one shot. Several iterations or tradeoff steps are necessary, which require a great

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deal of design expertise, which could become a major obstacle to the beginners.

Another idea proposed recently by Guo [10] is a local search method, which is also a method based on design equations. Discrepancies found between the performance metrics predicted by equations and validated by simulation are utilized by a set of relaxed equations to correct the current sizing. Guo [10] reported convergence by the relaxation iteration provided that an initial sizing calculated by design equations is sufficiently close to a local optimum. Repeatedly SPICE simulation is needed in the relaxation-based iterations.

However, all the previously mentioned sizing processes do not guarantee that the obtained sizing result be optimal in any sense because a sizing process will be terminated as long as a set of performance requirements have been satisfied. When conflict occurs, it is up to the designer to resolve the conflict, which is quite time-consuming sometimes. When designing multi-stage opamps (say, three stages), designers would have to work with more number of design equations, which could complicate hand calculation for device sizing.

Auto-sizing of opamps has been a constantly visited research subject in the literature. In the early days, auto-sizing was approached by simulation-based optimization, such as the works published at the end of 1980's [11–13]. However, those early works did not address the use of design equations. Also, multi-stage amplifier design was not yet a major research interest then.

Other optimization techniques applied to the automatic sizing of opamps include a combination of genetic algorithm (GA) and simulated annealing (SA) [14], a combination of GA with neural networks [15], a combination of GA with particle swarm optimization (PSO) [16], other variants of PSO [17, 18], and genetic programming (GP) [19], among others.

The novelty of this work is to incorporate design equations in a PSO-based search process for sizing two-stage and three-stage opamps. Currently, we use the design equations published in the research articles on specific multi-stage opamps. In future, it is also possible to automatically generate design equations for multi-stage opamps by a symbolic computation method [20]. Hence, it is a worthwhile effort to make a preliminary study on whether analytical design equations can enhance the efficiency of evolutionary search for the task of multi-stage opamp sizing.

The main contribution of this paper includes the following. Firstly, it develops a PSO method whose initial set is generated by using a set of design equations. In a sense PSO is used as a local optimizer that refines a set of feasible device sizes satisfying a set of design equations. Secondly, it develops a GA in the same setting, i.e., letting

GA begin with an initial population generated by the same set of design equations. Thirdly, we also investigate whether the integration of relaxation iteration [10] in PSO can benefit the convergence speed or even the suboptimal solution quality.

The rest of the paper is organized as follows. The equation-based auto-sizing procedure by PSO is described in Sect. 2. Then in Sect. 3 we outline design equations for several sample circuits on which we make experimental study in this paper. The experimental setting is then expanded on in Sect. 4 followed by reports on experimental results. Finally, Sect. 5 concludes the paper. A brief description of the design of GA used in this work is presented in “Appendix”.

2 Formulation of equation-based auto-sizing by PSO

2.1 Performance targets considered in this work

Opamp design begins with a set of performance targets. In this paper we mainly consider the set of $\{DC \text{ gain}, GBW, PM, CMRR, PSRR\}$, where GBW stands for *gain-bandwidth product*, PM for *phase margin*, CMRR for *common-mode rejection ratio*, and PSRR for *power-supply rejection ratio*.

When a set of design targets are given, the designer would have to choose a circuit topology first based on his/her design knowledge; the topology includes circuit elements that serve as compensation.

In order to appreciate the basic performance properties of a multi-stage amplifier, the designer would typically derive the open-loop transfer function (TF) from a stage-form macromodel, see for example the papers [5, 21–23]. After properly condensing the analytical expressions, a set of design equations can be derived as the characterization of the circuit ac performance. Mainly, the design equations can be associated with the properties such as dc gain, dominant poles-zeros, and phase margin, etc. Other special equations may be related to slew rate (SR), noise, and biasing currents, etc. Depending on the sizing strategy chosen, different design equations will be made use of with different priority.

The sizing steps can be described as follows. Given a CMOS transistor-level circuit and a set of performance targets, find the aspect ratios W/L (width over length) of all MOS devices, bias currents, and other design variables so that after SPICE simulation with a technology library the opmap performance meets the preset specifications.

2.2 PSO formulation

PSO is a nature-inspired collaborative optimization method [24, 25]. It works with a swarm of particles with position and velocity. Optimization is achieved by iteratively moving the swarm toward better solutions in reference to a given quality measure.

PSO is a population-based iterative optimization procedure, hence it requires an initial set of solution vectors in a given search space. Each particle consists of a vector of design variables of the opamp, which include the MOSFET dimensions (W/L) and other circuit variables like biasing currents and some lumped element values used in frequency compensation.

Suppose a particle swarm has the population size N . Each particle is composed of D design variables, represented by $x_i = [x_{i1}, x_{i2}, \dots, x_{iD}]$.

The D design variables with each particle are sufficient to define a SPICE netlist, which can be generated and passed to a SPICE simulator for simulation. Suppose we consider M performance measures for each circuit candidate. Let $T_k^{(d)}$ be the k th performance measure whose value is desired and let $T_k^{(sim)}(x_i)$ be the corresponding performance measure whose value is simulated for the circuit instance x_i . Then the relative performance error for the circuit instance (or particle) x_i is defined by

$$E_{rel}(x_i) := \sqrt{\sum_{k=1}^M \left(\frac{T_k^{(d)} - T_k^{(sim)}(x_i)}{T_k^{(d)}} \right)^2}. \tag{1}$$

We denote by $U[0, 1]$ the uniform distribution of real random numbers in the interval $[0, 1]$. $\rho \in U[0, 1]$ means that ρ is a random number with the uniform distribution.

PSO requires the definition of the velocity of each particle to update the particle position during iteration. It is a self-updated random vector defined by

$$v_{i,d}^{k+1} = v_{i,d}^k + c_1 \cdot \rho_1 \cdot (p_best_{i,d}^k - x_{i,d}^k) + c_2 \cdot \rho_2 \cdot (g_best_d^k - x_{i,d}^k) \tag{2}$$

where $\rho_1, \rho_2 \in U[0, 1]$. The index i ranges in $\{1, \dots, N\}$, the index d ranges in $\{1, \dots, D\}$, and k is the iteration index. $p_best_i^k$ is the best circuit instance once achieved by the i th particle in all iterations up to the k th step. g_best^k is the circuit instance of the best performance achieved by the whole swarm in all iterations up to the k th step. c_1 and c_2 are the acceleration coefficients, specifying the relative attraction nearby $p_best_i^k$ and g_best^k , respectively.

An alternative velocity vector is defined by the next equation

$$v_{i,d}^{k+1} = w^k * v_{i,d}^k + c_1 \cdot \rho_1 \cdot (p_best_{i,d}^k - x_{i,d}^k) + c_2 \cdot \rho_2 \cdot (g_best_d^k - x_{i,d}^k) \tag{3}$$

where an inertia factor w^k is introduced to adjust the weight of the previous velocity. Initially, w^0 is chosen $0 < w^0 < 1$ and is reduced linearly with each iteration. Equation (3) is what we used in our PSO implementation for velocity update.

The entries of the i th particle are updated by the following equation

$$x_{i,d}^{k+1} := x_{i,d}^k + v_{i,d}^{k+1}. \tag{4}$$

In order to accelerate the convergence of PSO iteration, reducing the search space dimensionality is an effective tactic. One option would be to use design equations, which restrict the search space where the circuit variables can vary. Since the adjustment of velocity in PSO is quite autonomous, we decide to apply design equations in the generation of the initial swarm to restrict the PSO search space in the region defined by the design equations. In this sense the subsequent PSO search serves as a local optimizer.

3 Design equations of sample circuits

Design equations are consequence of certain circuit structure and their connection to the performance requirements. Since the compensation network in a multi-stage opamp directly controls the pole-zero structure in the frequency domain, the details of a circuit topology can significantly alter the expression of design equations. Hence, design equation belongs to the topology-pertinent property of an amplifier. In other words, for each specific configuration of an amplifier, its associated design equations should be derived specifically by hand or generated by a computer program such as [20].

We shall use design equations in the generation of the initial circuit instances in PSO and in the embedded relaxation iterations. In this section we present one set of design equations for the standard two-stage opamp with simple Miller compensation (SMC) and refer to the literature for the design equations of other circuits. Our main focus in this work is on the two-stage or three-stage amplifier circuits.

3.1 Design equations of the CMOS two-stage SMC opamp

Shown in Fig. 1 is a standard two-stage CMOS opamp containing a simple Miller compensation capacitor C_C .

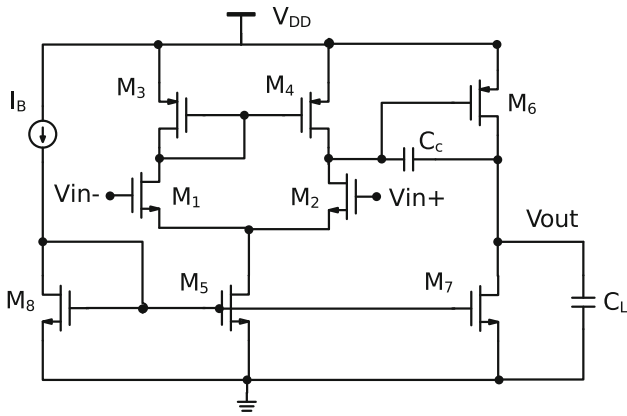


Fig. 1 CMOS two-stage SMC opamp

Thus this opamp is referred to as the SMC opamp. We shall present design equations pertinent to the noise, GBW, PM, and SR metrics, etc.

Palmisano et al. [5] presented a manual design procedure for the SMC opamp and its extensions. This procedure starts from the noise requirement. Neglecting flicker noise at low frequencies, we may write the input noise voltage spectral density of the two-stage opamp as

$$S_n(f) = 2 * 4kT \frac{2}{3g_{m1,2}} \left\{ 1 + \frac{g_{m3,4}}{g_{m1,2}} \right\} \quad (5)$$

where k is the Boltzmann constant and T is the absolute temperature.

Assuming $g_{m3,4} \ll g_{m1,2}$, we may calculate the transconductance of transistors M1,2 approximately from (5)

$$g_{m1,2} \approx \frac{16kT}{3S_n(f)}. \quad (6)$$

After $g_{m1,2}$ is known, the GBW requirement gives rise to the estimation of the compensation capacitor given by

$$C_C = \frac{g_{m1,2}}{2\pi f_{GBW}}. \quad (7)$$

Next, by the (internal and external) SR equations relating the quiescent currents $I_{D1,2}$ and I_{D7} to the lumped capacitor values

$$SR_{int} = \frac{2I_{D1,2}}{C_C} \quad (8)$$

$$SR_{ext} = \frac{I_{D7} - 2I_{D1,2}}{C_L} \quad (9)$$

where C_C is the compensation capacitor and C_L is the load capacitor, the biasing currents can be estimated by

$$I_{D1,2} = \frac{SR}{2} C_C \quad (10)$$

$$I_{D7} = SR(C_C + C_L) = 2 \left(1 + \frac{C_L}{C_C} \right) I_{D1,2} \quad (11)$$

where $SR_{int} = SR_{ext} = SR$ is assumed.

By $g_m = 2\sqrt{K_{n,p} \frac{W}{L} I_D}$ where $K_{n,p} = \mu_{n,p} C_{OX}/2$, the aspect ratio of transistors M1,2 can be derived from (11) as

$$\left(\frac{W}{L} \right)_{1,2} = \frac{g_{m1,2}^2}{4K_n I_{D1,2}}. \quad (12)$$

On the other hand, a pole-zero analysis gives rise to the phase margin expression

$$M_\phi = 90^\circ - \arctan \frac{f_{GBW}}{f_2} \quad (13)$$

where f_2 denotes the second dominant pole

$$f_2 = \frac{g_{m6}}{2\pi C_L}. \quad (14)$$

From the above two equations we may derive the transconductance gain of M6

$$g_{m6} = 2\pi f_{GBW} C_L \tan(M_\phi). \quad (15)$$

The aspect ratio of M6 is then given by

$$\left(\frac{W}{L} \right)_6 = \frac{g_{m6}^2}{4K_p I_{D6}} \quad (16)$$

because $I_{D6} = I_{D7}$.

As suggested by [5], the separation factor, κ , between the second pole (at frequency f_2) and the GBW frequency, i.e.,

$$\kappa = \frac{f_2}{f_{GBW}} \quad (17)$$

is a helpful parameter to facilitate decision-making in design.

Combining (7), (14), and (17), we obtain an estimate of the compensation capacitor by

$$C_C = \kappa \frac{g_{m1,2}}{g_{m6}} C_L \quad (18)$$

where κ can be determined by the phase margin requirement, i.e., $\kappa = \tan(PM) > 1$.

By the fact that $V_{GS3} = V_{DS4} = V_{GS6}$, the aspect ratios of M3,4 are related by

$$\left(\frac{W}{L} \right)_{3,4} = \frac{I_{D3,4}}{I_{D6}} \left(\frac{W}{L} \right)_6. \quad (19)$$

Furthermore, by $I_{D5} = 2I_{D1,2}$, the aspect ratios of M5 and M7 satisfy

$$\left(\frac{W}{L}\right)_5 = \frac{I_{D5}}{V_{DSAT5}^2 K_n}, \tag{20}$$

$$\left(\frac{W}{L}\right)_7 = \frac{I_{D7}}{V_{DSAT7}^2 K_n}. \tag{21}$$

If we set $V_{DSAT8} = V_{DSAT5,7}$, the biasing current I_B can be calculated by

$$I_B = \frac{\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_5} I_{D5}. \tag{22}$$

Remark 1 Note that in the above deduction all design targets are regarded as equalities. Since most design targets are specified as the reference numbers not necessarily being achieved exactly, these equalities should be considered as the reference targets for optimization. Because we use the design equations to generate an initial swarm for PSO search, the search result would usually produce the best possible approximation to the targets as long as the specified targets are feasible. If we would like to achieve better performance targets for certain metrics, we may choose higher target values for these metrics.

3.2 Design equations of three kinds of two-stage opamps with modified compensations

The simple Miller compensation in the opamp of Fig. 1 results in a zero in the right-half plane (RHP). In order to eliminate the RHP zero and improve phase margin, one may choose an alternative compensation in place of the Miller capacitor C_C . Three commonly adopted strategies are: nulling resistor (NR) in series with C_C , voltage buffer (VB) in series with C_C , and current buffer (CB) in series with C_C , see Fig. 2. Palmisano and Palumbo studied the optimization of these alternative compensations with NR and VB in [21] and CB in [22]. The reader may find the related design equations in these works.

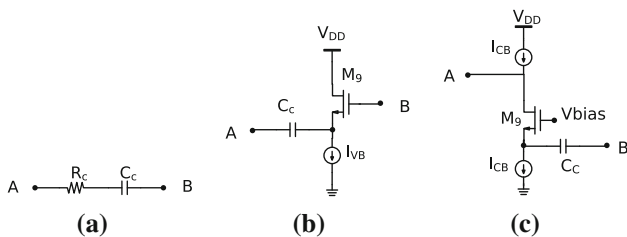


Fig. 2 Three alternative compensations for the two-stage opamp: **a** nulling resistor (NR) with C_C . **b** Voltage buffer (VB) with C_C . **c** Current buffer (CB) with C_C

3.3 Design equations of a CMOS three-stage opamp

A three-stage opamp with reversed nested Miller compensation added with feedforward and nulling resistor (RNMCFNRR) was proposed by Grasso et al. [23]. The transistor circuit schematic is shown in Fig. 3. The cascade of three stages enables a dc gain above 100 dB even with a low supply voltage. The specific compensation design was aimed at GBW enhancement. The detailed design equations can be found in [23].

3.4 Design equation based relaxation iteration

Guo [10] proposed a relaxation iteration (RI) procedure, which iteratively corrects the discrepancy found by comparing the performance metrics predicted by design equations and by simulation. Since the design equations might involve multiple performance measures in the same equation, relaxation can convert the equations into an iterative computation procedure. If the circuit sizing gradually reaches a local optimal operating point, then the high order terms neglected in design equations become truly minor. As a result, the circuit performance predicted by the approximate design equations agree better with the SPICE simulation results. So roughly one may anticipate that the relaxation iteration tends to converge.

According to Guo [10], relaxation-based iteration introduces parameter update equations by modifying the existing design equations into delta-correction; that is, adding a Δp term to a relaxation equation arising from its associated design equation.

For example, for the two-stage SMC opamp, we may perform one iteration on the GBW frequency as follows

$$f_{GBW} = \frac{g_{m1,2}}{2\pi C_C} + \Delta f_{GBW} \tag{23}$$

where Δf_{GBW} is a discrepancy between the predicted and the simulated. Upon convergence, $\Delta f_{GBW} = 0$ and the

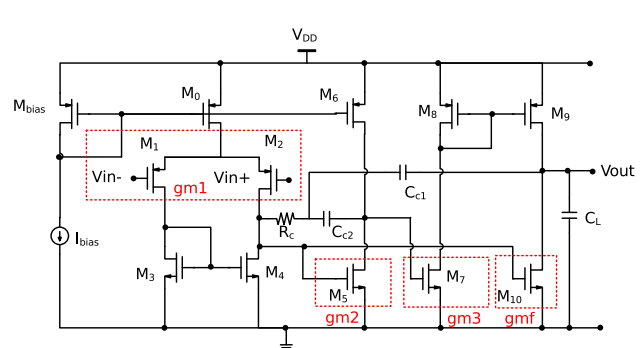


Fig. 3 Schematic of the three-stage RNMCFNRR opamp [23]

predicted f_{GBW} would be equal to the simulated. Similarly, one may make a correction on the phase margin as:

$$\phi = \frac{\pi}{2} - \tan^{-1} \frac{f_{GBW}}{f_2} + \Delta\phi. \quad (24)$$

The error terms Δf_{GBW} and $\Delta\phi$ above are calculated as follows

$$\Delta f_{GBW} = f_{GBW}^{(sim)} - \frac{g_{m1,2}^{(sim)}}{2\pi C_C}, \quad (25)$$

$$\Delta\phi = \phi^{(sim)} - \frac{\pi}{2} + \tan^{-1} \frac{f_{GBW}}{f_2^{(sim)}}, \quad (26)$$

where $g_{m1,2}^{(sim)}$, $f_2^{(sim)}$, $f_{GBW}^{(sim)}$, and $\phi^{(sim)}$ are the simulated transconductance of M1,2, the second dominant pole frequency, GBW, and PM, respectively, of the circuit at the last iteration step.

Other key design parameters can be updated as follows.

$$g_{m1,2} = g_{m1,2}^{(sim)} + 2\pi(f_{GBW} - f_{GBW}^{(sim)})C_C, \quad (27)$$

$$\frac{f_{GBW}}{f_2} = \tan\left(\tan^{-1} \frac{f_{GBW}}{f_2^{(sim)}} + (\phi^{(sim)} - \phi)\right). \quad (28)$$

By Eqs. (14) and (28), we can update g_{m6} by

$$g_{m6} = \frac{2\pi C_L f_{GBW}}{\tan\left(\tan^{-1} \frac{f_{GBW}}{f_2^{(sim)}} + (\phi^{(sim)} - \phi)\right)}. \quad (29)$$

The rest performance metrics and the related design parameters can be handled analogously. The slew rate can be corrected by

$$SR = \frac{2I_{D1,2}}{C_C} + \Delta SR = \frac{I_{D7}}{C_C + C_L} + \Delta SR. \quad (30)$$

Then update the bias currents by

$$I_{D1,2} = I_{D1,2}^{(sim)} + \frac{SR - SR^{(sim)}}{2} C_C, \quad (31)$$

$$I_{D7} = I_{D7}^{(sim)} + (SR - SR^{(sim)})(C_C + C_L). \quad (32)$$

Based on the above equations, the device sizes can be corrected accordingly.

In relaxation iteration, a scaling factor $\alpha \in (0, 1)$ can be introduced in the updating formulas to improve convergence [10].

Since the convergence of relaxation iteration is highly sensitive to the vicinity of the beginning circuit operating point (OP) to a local optimum, the performance of RI in local correction is not guaranteed in general. In our PSO experiment, we would intend to apply RI as a PSO enhancement. We shall investigate in our experiment that by embedding RI in the course of PSO iterations whether

the convergence of PSO can be accelerated. The details will be described in the next section.

4 Experimental results of PSO and comparison to GA

4.1 Experimental setup

We used the open source circuit simulator NGSPICE [26] in our experiment. The device model used in simulation was BSIM3 180 nm CMOS process. The PSO and GA (used as a comparison) programs were written in the C programming language and compiled by the GCC compiler. The runtime environment was an Intel core i7 3.6 GHz processor with 3.8 GB RAM running the Ubuntu Linux operating system.

When running PSO for auto-sizing of multi-stage opamps, we used the relative error function (1) to select $p_best_i^k$ of the i th particle and g_best^k at the k th iteration. The swarm size of PSO was set to 30. The inertia weight w^k varied from 0.9 to 0.4 linearly with iterations. Both of the acceleration coefficients c_1 and c_2 were set to 1.48. The position and velocity of each particle were updated by the iteration formula (4) and (3) (the one with an inertia factor), respectively. Note that the choice of the algorithm parameters was empirical, subject to experience-based adjustment for a specific circuit and performance targets in practice.

4.2 Results on the two-stage SMC opamp

Referring to Fig. 1, the design variables of the two-stage opamp are the aspect ratios (W/L) of eight transistors M1–M8, the bias current I_B , and compensation capacitor C_C . The sizing parameter finally obtained at the end of PSO are listed in Table 1. Table 2 lists the performance results of

Table 1 Sizing parameters of the two-stage SMC opamp. All aspect ratios are in units $\mu\text{m}/\mu\text{m}$

Parameters (by PSO)	Value	Value (by GA)
$(W/L)_{1,2}$	2.77/1	1.02/1
$(W/L)_{3,4}$	6.54/1	7.86/1
$(W/L)_5$	17.18/1	20.82/1
$(W/L)_6$	82.01/1	78.46/1
$(W/L)_7$	99.94/1	95.38/1
$(W/L)_8$	38.70/1	41.35/1
C_C	2.0 pF	1.18 pF
I_B	57.37 μA	53.30 μA

Table 2 Performance of the two-stage SMC opamp

Spec.	Desired	Simulated (by PSO)	Simulated (by GA)
Dc-gain	80 dB	78.74 dB	77.20 dB
GBW	10 MHz	10.00 MHz	10.01 MHz
PM	60°	60.32°	57.91°
CMRR	80 dB	76.60 dB	77.10 dB
PSRR	80 dB	82.62 dB	83.13 dB
SR+	–	12.70 V/μs	22.32 V/μs
SR–	–	11.41 V/μs	17.89 V/μs
Error	–	0.054484	0.072705

the optimized opamp and the desired values. The load capacitor C_L was fixed at 5 pF.

Figure 4 shows the evolution of the relative error of the two-stage opamp. The relative error curve stops descending after 180 PSO steps, indicating that a suboptimal solution has been reached by PSO.

Figures 5, 6 and 7 show the NGSPICE simulation results of the two-stage opamp for frequency response, CMRR, PSRR, and transient response to a period square wave, respectively, for the SMC opamp.

4.2.1 Comparison to GA

In order to make comparison, we also implemented a GA-based sizing program. The algorithm design is presented in “Appendix”. When running GA, we chose a population size of 40 individuals and set the number of iterations to 200. From Fig. 8, we find the fact that GA reached convergence after 189 iterations. The sizing parameters and the performance of the final suboptimal solution are listed

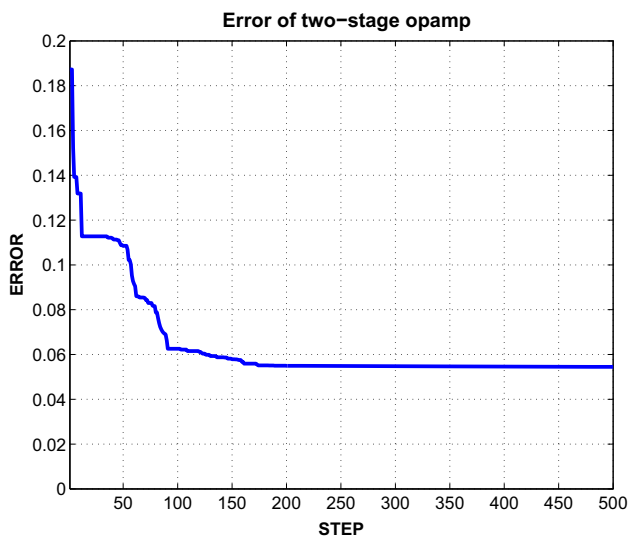


Fig. 4 Evolution of the relative error of the two-stage SMC opamp

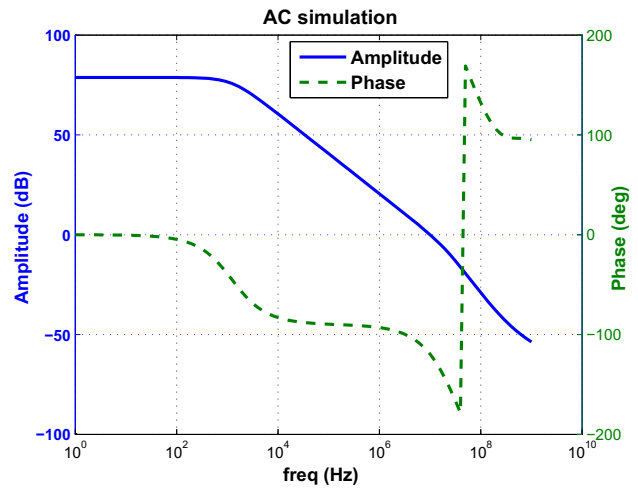


Fig. 5 Frequency response of the two-stage SMC opamp

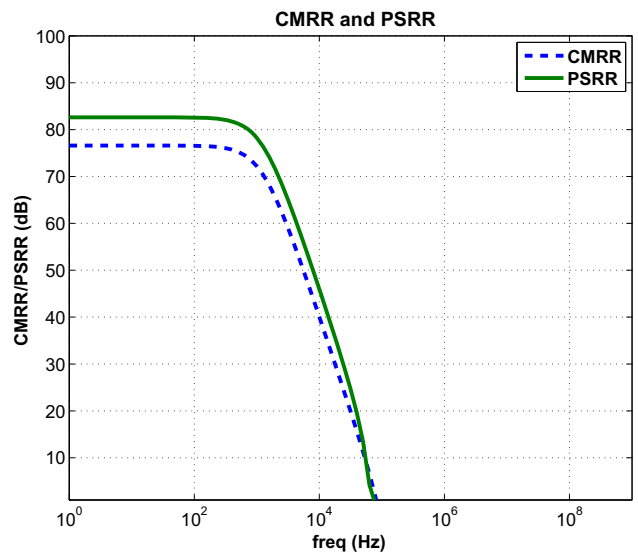


Fig. 6 CMRR and PSRR of the two-stage SMC opamp

in Tables 1 and 2, respectively, as well. The SPICE simulation results have been suppressed except for a comparison of the PSO evolution curves regarding the relative errors, which is shown in Fig. 8.

The next experiment further testifies that PSO search outperformed GA when optimizing the two-stage SMC opamp with a set of raised performance target values. This experiment also answers a question regarding the performance frontier; whether better performance than the specified can be achieved given a circuit topology. As we know, if the circuit topology does not change, the design equations remain the same. Hence, a search algorithm with a better capability of exploring the design space should be able to produce a better optimized design. Table 3 shows that PSO performed better than GA when the performance values are raised.

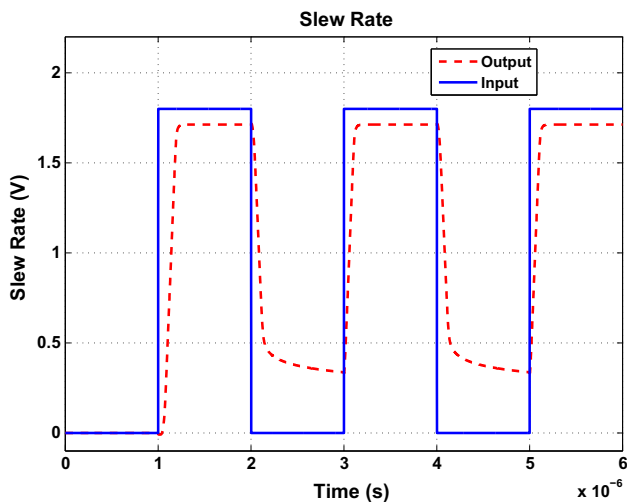


Fig. 7 Transient response of the two-stage SMC opamp

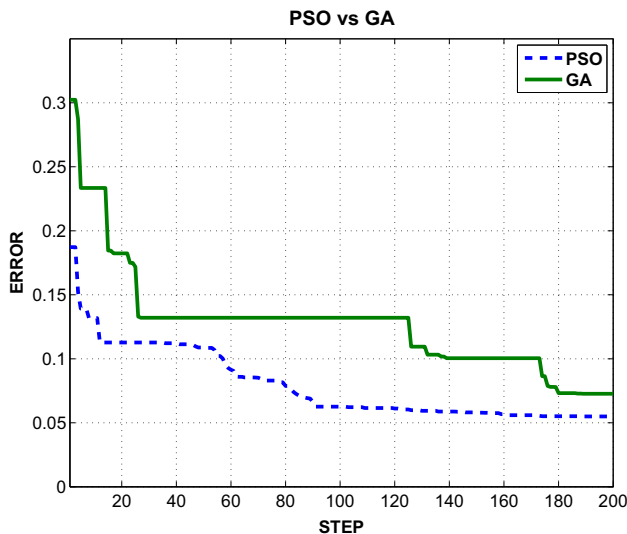


Fig. 8 Comparison of PSO and GA relative error evolution curves for the two-stage SMC opamp

Table 3 Comparison of the PSO and GA searching results for the two-stage SMC opamp with lifted targets

Spec.	Desired	Simulated (by PSO)	Simulated (by GA)
DC-gain	85 dB	83.30 dB	74.15 dB
GBW	13 MHz	12.95 MHz	12.26 MHz
PM	63°	62.88°	59.27°
CMRR	85 dB	84.52 dB	82.92 dB
PSRR	90 dB	90.54 dB	88.96 dB
Error	–	0.022047	0.154101

In conclusion, using PSO as a local optimizer in auto-sizing of multi-stage opamps outperforms GA relatively. We may attribute the reason to the fact that PSO is suited better to locally searching a continuous variable space while GA is relatively weaker due to that the crossover and

mutation operators have limited searching power in a continuous high-dimensional space. Because the performance of PSO is more promising in the scenario of circuit sizing, we decide to use PSO as the key optimizer in the following experiments.

4.3 Results on the two-stage opamps with three modified compensations

The simple Miller compensation (with the Miller capacitor C_C only) of the two-stage opamp shown in Fig. 1 can be modified by inserting extra circuit components into the Miller capacitor C_C branch. We mainly consider the following three alternative compensation structures: C_C in series with a nulling resistor (NR), with a voltage buffer (VB), or with a current buffer (CB); the corresponding circuit blocks are shown in Fig. 2. The resulting opamps are referred to as the MCNR opamp, MCVB opamp, and MCCB opamp, respectively.

The MCNR opamp has the following PSO design variables: the aspect ratios of eight transistors M1–M8, bias current I_B , compensation capacitor C_C , and the nulling resistor R_C .

The MCVB opamp has the following PSO design variables: the aspect ratios of nine transistors M1–M9 (one appearing in the VB block), bias current I_B , I_{VB} and compensation capacitor C_C .

The MCCB opamp has the following PSO design variables: the aspect ratios of nine transistors M1–M9 (one appearing in the CB block), bias current I_B , I_{CB} and compensation capacitor C_C .

The PSO results on these three kinds of two-stage variants are summarized in Table 4 and the comparisons of the optimized performances are listed in Table 5. For all cases the output load C_L was fixed at 5 pF.

Shown in Figs. 9, 10, 11 are the relative error evolution curves during the execution of PSO for the MCNR, MCVB, and MCCB opamps, respectively. To save space we do not show the simulated performance plots for these examples.

4.4 Results on the three-stage RNMCFNR opamp

Referring to Fig. 3, the design variables of the three-stage RNMCFNR opamp are: W/L of 11 transistors M0–M10, W/L of the bias transistor M_{bias} , bias current I_{bias} , compensation elements C_{C1} , C_{C2} and R_C . The load capacitor C_L was fixed at 500 pF.

The sizing parameters after the PSO run are listed in Table 6. The simulated circuit performance numbers are listed in Table 7. Figure 12 shows the relative error evolution of the three-stage RNMCFNR opamp; it stops

Table 4 Sizing parameters of the three two-stage opamp variants. All aspect ratios are in units $\mu\text{m}/\mu\text{m}$

Parameters	MCNR	MCVB	MCCB
$(W/L)_{1,2}$	5.63/1	4.48/1	6.78/1
$(W/L)_{3,4}$	2.15/1	10.12/1	10.77/1
$(W/L)_5$	4.43/1	30.07/1	28.30/1
$(W/L)_6$	100.00/1	58.50/1	58.67/1
$(W/L)_7$	100.00/1	80.01/1	74.60/1
$(W/L)_8$	17.38/1	28.17/1	36.24/1
$(W/L)_9$	–	1.06/1	37.77/1
R_C	2.52 k Ω	–	–
C_C	1.48 pF	1.28 pF	1.24 pF
I_B	99.98 μA	23.86 μA	32.61 μA
I_{VB}	–	23.86 μA	–
I_{CB}	–	–	32.61 μA

descending after about 250 steps, which indicates that the best suboptimal solution has been found by PSO.

Figures 13, 14 and 15 show the SPICE simulation results of the three-stage RNMCFNR opamp for the AC response, CMRR, PSRR, and transient response, respectively.

For the RNMCFNR opamp, we also made a test to see whether using design equations could significantly improve the quality of suboptimal solution in PSO search. This is indeed true. Figure 16 shows a comparison of the evolution curves of the relative errors. We see that the PSO search without using design equations in producing the particles of the initial swarm (particles generated at random) had a curve with much larger relative errors comparing to the one using design equations for the initial swarm. The comparison is a clear indication that design equations can contribute significantly to producing a better quality initial swarm and enhancing the quality of the final PSO search result.

Table 5 Performance measures of the three two-stage opamp variants optimized by PSO

Spec.	MCRZ		MCVB		MCCB	
	Desired	Simulated	Desired	Simulated	Desired	Simulated
DC gain	81.5 dB	78.16 dB	81.5 dB	80.39 dB	79 dB	79.78 dB
GBW	17 MHz	16.75 MHz	21 MHz	21.10 MHz	24 MHz	23.81 MHz
PM	65°	63.25°	60°	60.93°	70°	69.16°
CMRR	80 dB	77.83 dB	80 dB	77.99 dB	80 dB	76.83 dB
PSRR	80 dB	83.85 dB	80 dB	84.01 dB	80 dB	82.84 dB
SR+	–	15.95 V/ μs	–	25.04 V/ μs	–	21.32 V/ μs
SR–	–	14.38 V/ μs	–	13.27 V/ μs	–	10.71 V/ μs
Error	–	0.075306	–	0.058201	–	0.055942

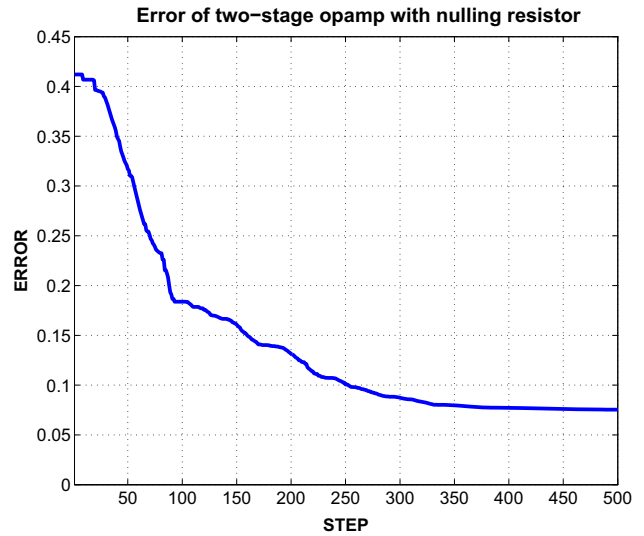


Fig. 9 Evolution of the PSO relative error for the two-stage MCNR opamp

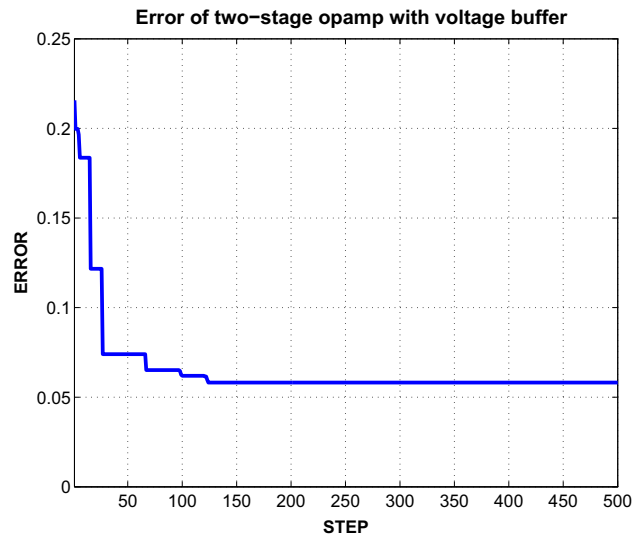


Fig. 10 Evolution of the PSO relative error for the two-stage MCVB opamp

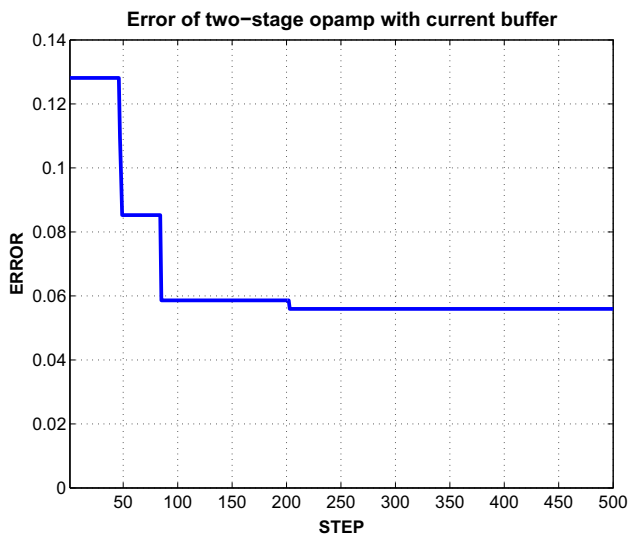


Fig. 11 Evolution of the PSO relative error for the two-stage MCCB opamp

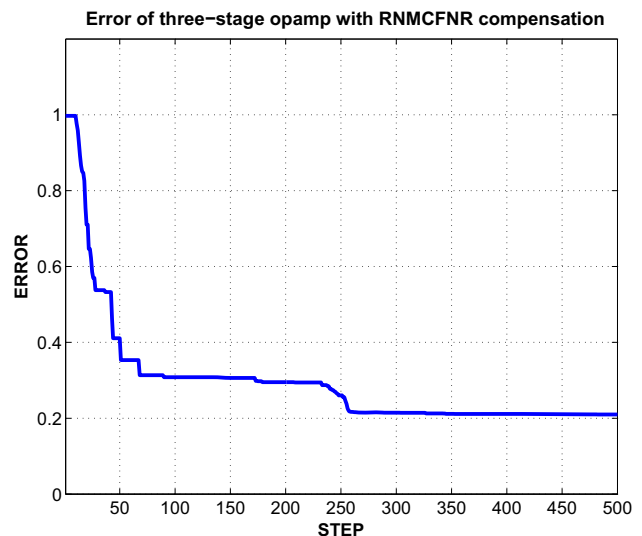


Fig. 12 Evolution of the PSO relative error for the three-stage RNMCFNR opamp

Table 6 Sizing parameters of the three-stage RNMCFNR opamp. All aspect ratios are in units $\mu\text{m}/\mu\text{m}$

Parameters	Value
$(W/L)_{0,6,8,9}$	22.87/0.5
$(W/L)_{1,2}$	6.93/0.5
$(W/L)_{3,4}$	10.06/0.5
$(W/L)_{5,7,10}$	25.15/0.5
$(W/L)_{bias}$	2.07/0.5
R_C	2.62 k Ω
C_{C1}	8.61 pF
C_{C2}	1.00 pF
I_{bias}	5.81 μA

Table 7 Performance of the three-stage RNMCFNR opamp

Spec.	Desired	Simulated
DC-gain	112 dB	99.69 dB
GBW	3 MHz	3.02 MHz
PM	63°	62.99°
CMRR	80 dB	85.26 dB
PSRR	80 dB	91.32 dB
SR+	–	2.71 V/ μs
SR–	–	6.23 V/ μs
Error	–	0.209975

4.5 Test on relaxation iteration embedding

The previous PSO tests have demonstrated that, starting from an initial instance set generated by design equations, PSO can effectively search a suboptimal solution. But the convergence takes quite a number of iterations.

Thus we were motivated to further test whether embedding the relaxation iteration can accelerate the PSO

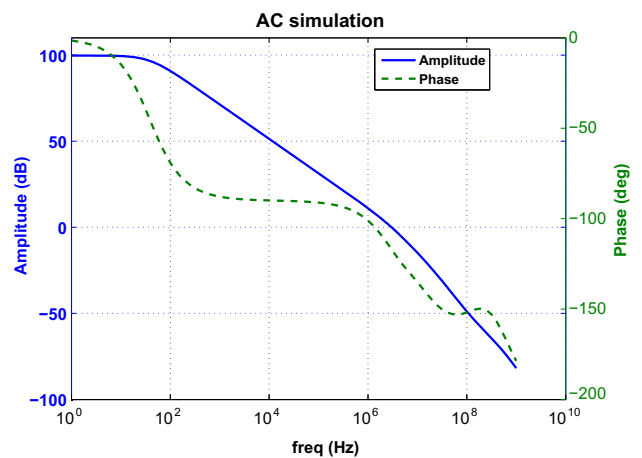


Fig. 13 Frequency response of the three-stage RNMCFNR opamp

convergence without sacrificing the suboptimal solution quality. Since RI is equation-based iteration, it fits in the scenario of equation-based PSO. Our test was focused on two circuits: the two-stage SMC opamp and the three-stage RNMCFNR. While running RI, the compensation capacitor C_C remains unchanged.

Knowing that relaxation iterations could be effective if the fitness of instance is sufficiently small, we initiate RI after a period of PSO iterations. We made the insertion of RI adjustable so that the convergence enhancement became more effective.

We chose to preset a relative error level of PSO iterations to invoke RI and set a control number (K) for RI iteration. After K relaxation iterations, PSO continues until the end.

Figure 17 shows a comparison of PSO error evolution with and without RI embedding for the two-stage SMC

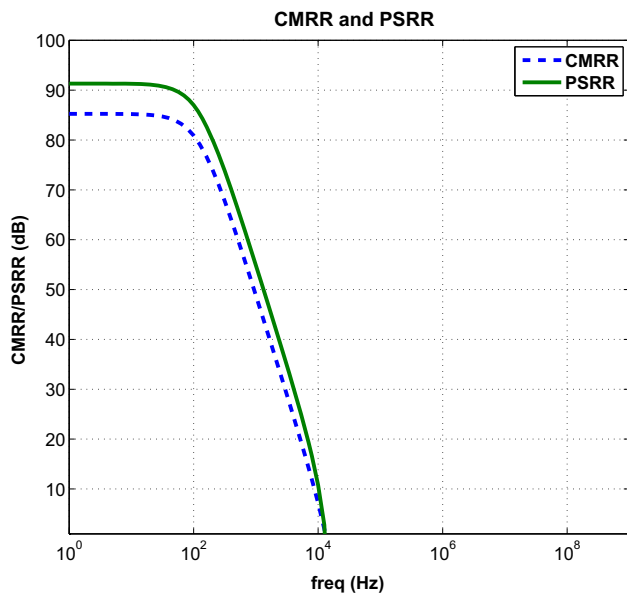


Fig. 14 CMRR and PSRR curves of the three-stage RNMCFNR opamp

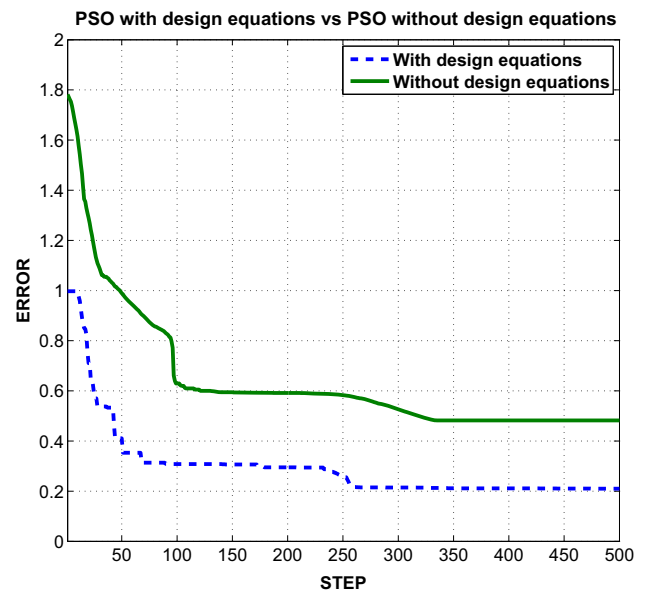


Fig. 16 Comparison of the PSO relative error evolution curves for the three-stage RNMCFNR opamp with and without using design equations in PSO search

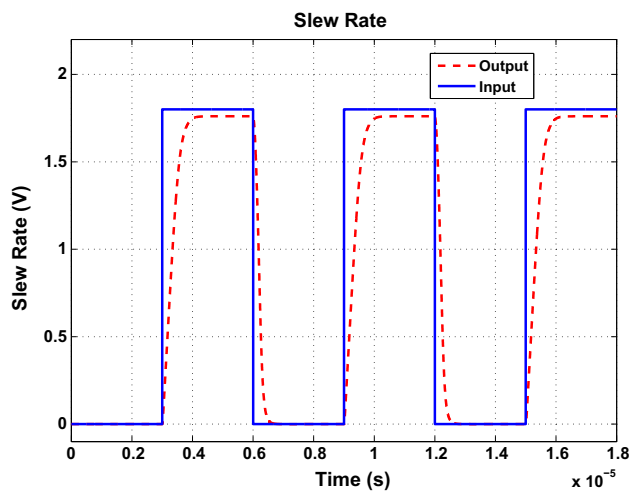


Fig. 15 Transient response of the three-stage RNMCFNR opamp

opamp. In this test RI was inserted at the relative error level of 20%; that is, RI was invoked when the initial PSO search had dropped the relative error by 20%, which was about 7 PSO iterations. After 2 relaxation iterations, PSO continued to the end. We observe that with only two steps of RI a significant amount of relative error was decremented.

We also tested the same RI embedding strategy for the three-stage RNMCFNR opamp with the error evolution curves of shown in Fig. 18. For this case RI was activated when the relative error level dropped by 70% by the initial PSO iteration. The reason we select a large percentage was because the initial error of the three-stage RNMCFNR opamp was large. Again the number of relaxation iterations was 2. For both curves the initial part of PSO iterations

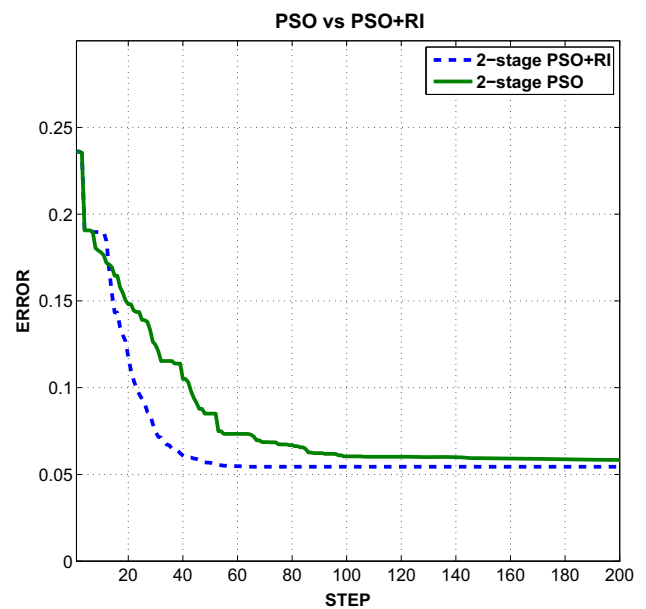


Fig. 17 Comparison of PSO convergence with and without RI for the two-stage SMC opamp

were made identical to exhibit the effect of RI activation, which did explicitly accelerated convergence.

Finally, we mention the CPU time in the executions of PSO, POS+RI, and GA on the examples we have tested. For the two-stage SMC opamp the CPU time was about 28 min by PSO only and 42 min by GA. After embedding RI, the CPU time spent on the two-stage SMC opamp by PSO was reduced to about 13 min. While testing the other three two-stage opamps with modified compensations, we

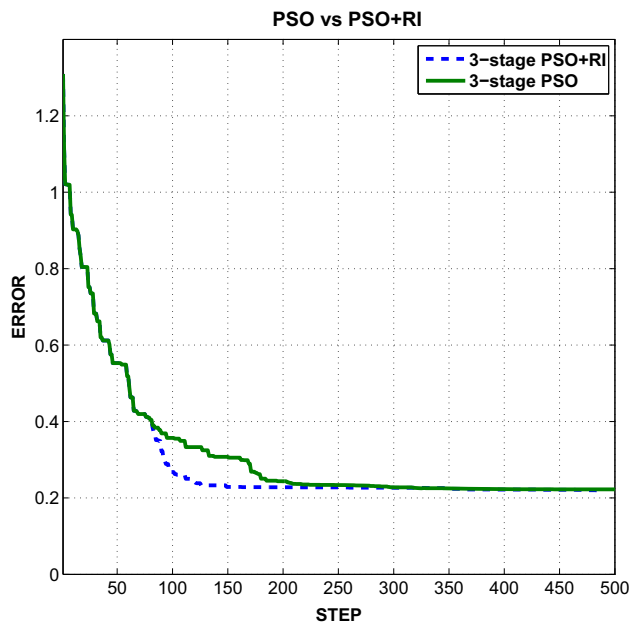


Fig. 18 Comparisons of PSO convergence with and without RI for the three-stage RNMCFNR opamp

measured the following CPU time costs by equation-based PSO search: MCNR 48 min, MCVB 20 min, and MCCB 35 min. Last, for the three-stage RNMCFNR opamp, the PSO search without using design equations took 72 CPU min, whereas by using design equations the CPU time was reduced to 54 min. By PSO with RI embedding, the CPU time spent on the three-stage RNMCFNR opamp was reduced to 30 min.

5 Conclusion

The main purpose of this paper is to make an experimental study on the role that design equations may play when they are combined with a heuristic search algorithm like PSO or GA. Although PSO performs relatively better than GA in the investigated scenario of local search, whether such a discrepancy is affirmative would require further investigation. A more interesting observation is that, by incorporating an auto-generation engine of design equations, the equation-based auto-sizing tool would become more powerful. This approach is believed to be more promising than other fully heuristic search routines without considering the use of design equations. Recent research has shed light on the auto-generation of design equations for a class of multi-stage opamps with the help of symbolic computation [20, 27–30]. Future research will be directed toward integrating an equation generation engine with heuristic search methods like PSO to completely get rid of the need of manually deriving design equations in an auto-sizing tool.

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Appendix: Design of GA for comparison

GA is a well-known nature-inspired evolutionary algorithm that can be applied to heuristic search problems [31]. As a comparison to PSO, we develop in this section a GA for equation-based automatic circuit sizing. Similar to PSO, GA also searches a suboptimal solution by iterating a population. Hence, there exist issues of initial selection of population, fitness evaluation, and the design of genetic operators such as mutation, crossover, and elite selection.

In the same spirit of this work, we generate the initial population by design equations when using GA as the search engine. The vector formed by the design variables become an individual in the GA population. We assume that all MOS devices has the fixed channel length L . Hence, the channel width W_i of each MOS device becomes one of the optimization variables. Each W_i is a real number and an array of them forms the individual coding (i.e., the chromosome) in the GA. The fitness of each individual is evaluated by the inverse of the relative error function, i.e.,

$$\text{fitness}(x_i) = \frac{1}{E_{rel}(x_i)} \quad (33)$$

where $E_{rel}(x_i)$ was defined in (1).

We use the roulette wheel selection in generating a new population, which means that the probability of selecting an individual to serve as a parent is proportional to its fitness.

The operator of crossover is defined as follows.

$$a_{k,j} := \gamma a_{l,j} + (1 - \gamma) a_{k,j} \quad (34)$$

$$a_{l,j} := \gamma a_{k,j} + (1 - \gamma) a_{l,j} \quad (35)$$

where $a_{k,j}$ is the j th gene (i.e., W_j) of the k th chromosome (i.e., individual) and $a_{l,j}$ is the j th gene of the l th chromosome. $\gamma \in U[0, 1]$ controls the randomness of combining two chromosomes.

Mutation of the j th gene of the i th chromosome is defined below.

$$a_{i,j} := a_{i,j} + (a_{max} - a_{i,j})\phi(g), \quad \text{with probability } 50\% \quad (36)$$

$$a_{i,j} := a_{i,j} + (a_{min} - a_{i,j})\phi(g), \quad \text{with probability } 50\% \quad (37)$$

where, $\phi(g) := \rho(1 - g/G_{max})^2$, g is the current generation index, and G_{max} is the maximum number of GA generations. $\rho \in U[0, 1]$. a_{max} and a_{min} are the maximum and minimum values of the gene a_{ij} , respectively. For example,

the maximum and minimum channel widths of all W_j are set to 100 and 1, respectively, throughout the GA iterations. Namely, $a_{max} = 100$ and $a_{min} = 1$.

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