Analog Integrated Circuits and Signal Processing (2020) 102:225–235
https://doi.org/10.1007/s10470-019-01550-7

A test point selection approach for DC analog circuits with large number of predefined faults

Masoumeh Khanlari[1] · Mehdi Ehsanian[1]

Received: 25 June 2019 / Revised: 25 June 2019 / Accepted: 3 October 2019 / Published online: 2 November 2019

Abstract

Test point selection is an important stage in analog circuits fault diagnosis. In this paper, a test point selection method is proposed that is suitable for large numbers of predefined faults in DC analog circuits using the technique of constructing a fault dictionary for each component. Main idea is selecting a test point set with minimum amount of overlap between fault and no-fault regions for each component. A combined exclusive-inclusive algorithm is applied on each fault dictionary and using the achieved information, a grade is given to each test point. Then the test points with grades lower than a threshold value are eliminated and a decision guide is provided for tester to select final test point set. Applying this method on a benchmark circuit is eliminating 22% of test points and the accuracy metrics of proposed approach is comparable with using all of the test points. The results show that by eliminating 56% of the test points, the accuracy metrics just drops about 4%.

Keywords Fault diagnosis · Test point selection · Classification · Support vector data decomposition

1 Introduction

Methods for fault diagnosis of analog circuits fall in two categories called simulation before test (SBT) and simulation after test (SAT) [1]. SBT methods require minimum computation during the test and most of the computational effort are performed off-line. Fault dictionary is an important method of SBT approach, especially in diagnosing catastrophic faults [1]. A fault dictionary is a set of measurements of the circuit under test (CUT) simulated under potentially faulty conditions (including no-fault case) and constructed before the test. There are three important phases in the fault dictionary approach. At first, the circuit is simulated for each of the predefined faults and the resulting responses are stored. Next phase is selection of test points. The last phase is designing classifier to isolate the predefined faults. During the test, the faulty circuit is excited by the same stimuli that were used in simulations, and measurements are made at the preselected nodes. Finally, they are classified using the designed classifier to diagnose the fault.

Test points may be nodes at which the measurements are performed. In practice, it may not be possible to make measurements at every point of the circuit. Test point selection is process of selecting optimum set of points with maximum degrees of fault isolation.

Generally, test point selection methods fall in two categories: inclusive and exclusive approaches [2]. In inclusive approaches, the desired optimum set of test points is initialized to be null, then a new test point is added to it if needed. For the exclusive approaches, the desired optimum set is initialized to include all available test points. Then a test point will be deleted if its exclusion does not degrade the degree of fault diagnosis. Various criterions were used in contributions to include or exclude a test point. Ambiguity set (AS) and integer-coded table were used in [2] to define the criterion. Entropy index (EI) of test points is the criterion used in [3]. The work in [4] uses a fault-pair Boolean table technique instead of integer-coded table to increase its accuracy. The method in [5] used the line's slope of voltage equation between two nodes to select

✉ Mehdi Ehsanian
ehsanian@kntu.ac.ir

Masoumeh Khanlari
khanlari@kntu.ac.ir

[1] Electrical Engineering Department, K. N. Toosi University of Technology, Tehran, Iran

optimum test point set in linear time-invariant circuits. Probability density of node voltages is another approach used to define the criterion [6, 7]. The work in [6] introduced a fault-pair isolation table constructed by calculating the area of non-overlapping part of the distribution curves, and the work in [7] used fault-pair similarity coefficients calculated by Cauchy–Schwarz inequality. Combined inclusion–exclusion approach was also proposed in some contributions [8–10]. To take into consideration the component tolerances, a new integer-coded fault dictionary called extended fault dictionary (EFD) was used in [11]. A novel entropy measure was used as the criterion in this work. Some works have been done which cannot be classified into inclusion or exclusion group, such as graph based algorithm [12, 13], greedy randomized adaptive search procedure (GRASP) [14], genetic algorithm [15], multidimensional fitness function discrete particle swarm optimization (MDFDPSO) [16], Quantum-inspired evolutionary algorithm [17], binary bat algorithm (BBA) [18], and depth first search (DFS) algorithm [19].

In all of these works, whole fault classes are investigated during search for optimum test points. The works are based on exhaustive or local search which select optimum set for isolating predefined faults. It was pointed out in [3, 15] that exhaustive search is NP-hard. Also, time complexity of local search approaches is in direct proportion to the number of predefined faults. Therefore, these approaches are not applicable when the number of predefined faults is enlarged.

To deal with the problem of large numbers of predefined faults, the idea of designing a classifier for each of the circuit components rather than one classifier for the whole circuit was proposed in [20]. However, the method suffers from randomness effect of the used classifiers. Two overcome this problem, there is a new idea in designing approach of classifiers. In this way, classifiers are designed in two stages. At first, Support Vector Data Description (SVDD) technique is used to detect the fault regions in data space of each component. Afterward, classification among various classes included in fault regions are performed based on a clustering approach by using Improved Kernel Fuzzy C-Means (IKFCM) algorithm. The main idea of this paper is to find a test point set for each component by which the fault regions have minimum overlap with no-fault region. This leads to best isolation of fault and no-fault states. Since there are a few specified number of fault types that a component may be encountered with, this process has low complexity even if the number of circuit faults is large. Details about this approach are given in following sections.

This paper has been organized in five sections. Section 2 describes the fault diagnosis method. The new test point selection method is described in Sect. 3. Experimental results are discussed in Sect. 4 and finally, Sect. 5 concludes the paper.

2 Fault diagnosis method for large numbers of predefined faults

The proposed test point selection method is comprised of two phases: off-line process which is done before starting the test, and on-line process during the test process. These processes are described in following.

2.1 Off-line process

Figure 1 shows the diagram of off-line process. First, the predefined fault list is provided for the CUT, which usually includes all of single hard/soft faults, or all of double hard/soft faults. Here, hard fault means short-circuit and open-circuit, and soft fault means deviation from the specified tolerance ranges. Single fault means one component is faulty, and double fault means two components are faulty simultaneously. Single and double faults are most probable faults in analog circuits [1]. The circuit is

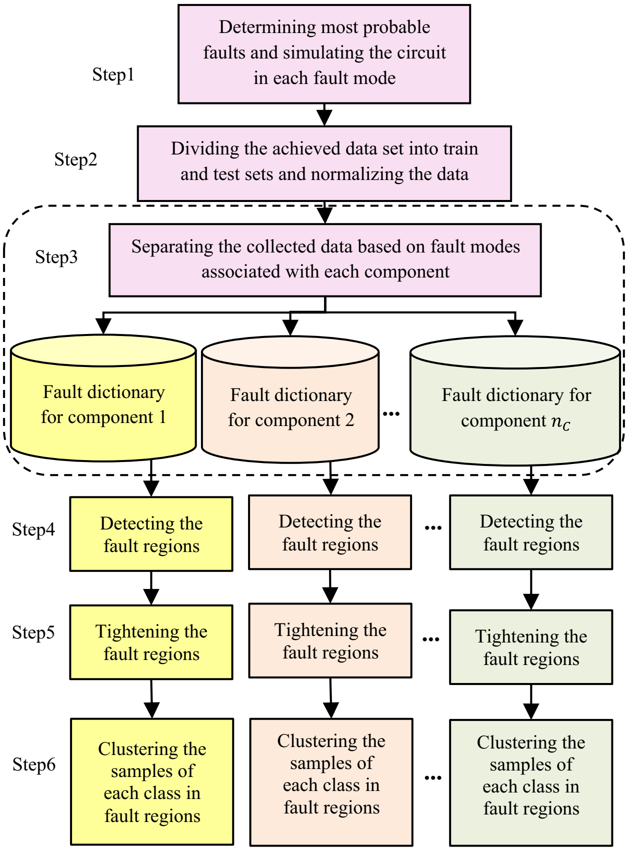
Step1
Determining most probable faults and simulating the circuit in each fault mode
Step2
Dividing the achieved data set into train and test sets and normalizing the data
Step3
Separating the collected data based on fault modes associated with each component
Fault dictionary for component 1
Fault dictionary for component 2
...
Fault dictionary for component n_c
Step4
Detecting the fault regions
Step5
Tightening the fault regions
Step6
Clustering the samples of each class in fault regions

Fig. 1 Diagram of constructing the fault dictionary with off-line process

Table 1 Predefined fault list in a supposed circuit

Predefined faults				Fault classes for the components		
#	R1	R2	R3	R1	R2	R3
1	O	–	–	O	–	–
2	S	–	–	S	–	–
3	–	O	–	–	O	–
4	–	S	–	–	S	–
5	–	–	O	–	–	O
6	–	–	S	–	–	S
7	–	–	–	–	–	–

simulated in each fault mode and no-fault mode to store measured responses in the fault dictionary.

The collected data of fault list are divided into the train and test sets and normalization is done by the Z-Score method with respect to the mean and standard deviation of the train set part. The normalized data are classified based on various fault types of each component. Table 1 shows the predefined single hard fault list for a typical circuit with three resistors, R1 to R3, and the fault types of each component. In this table, O, S, and "–" mean open-circuit, short-circuit and no-fault respectively. This categorization forms the required fault dictionary for each component.

Then, the fault regions in data space of each fault dictionary are recognized by the SVDD algorithm. The SVDD is a popular kernel-based technique to construct a flexible description of the input data [21]. This process has been shown for a typical component in Fig. 2 with two detected fault regions in which no-fault area are separated from fault regions.

For each component, the accurate diagnosing fault states are more importance than no-fault state, so the fault regions are tightened by t% when finding the samples of no-fault class that is located in the fault regions. Therefore, some of no-fault samples located in the fault regions are disregarded and the overlap between fault and no-fault samples is decreased with the penalty of misclassifying the disregarded no-fault samples. The value of t should be selected so that misclassification rate of no-fault class does not increase too much. This process is shown in Fig. 3. The left is a fault region containing the fault and no-fault samples. In the right, some of the no-fault samples that are located in the fault region disregarded with tightening the fault region.

The detected fault regions include the data from various fault classes and a part of no-fault class. The data of various classes in fault regions are clustered using IKFCM algorithm [20]. Thereby, some cluster centers are achieved which are used for classifying new data during the test (in on-line process).

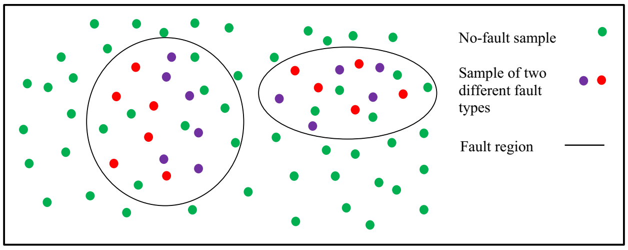

Fig. 2 Detecting the fault regions for a typical component by the SVDD algorithm

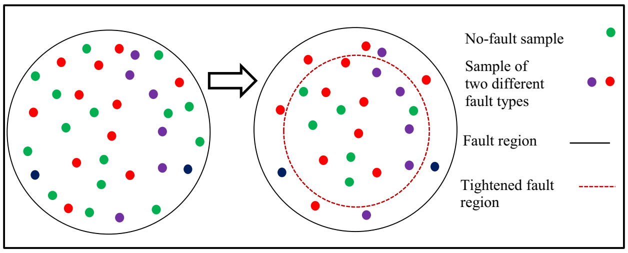

Fig. 3 Tightening fault region for no-fault samples; (left) fault region including fault and no-fault samples, (right) the tightened fault region

2.2 On-line process

The on-line process is performed during the test to classify a new measured data. Figure 4 shows the on-line process for a typical component. If data is located in fault regions, then the sample belongs to the no-fault class and so the component is non-faulty. Otherwise, classification is made in the fault region which includes this sample. For this purpose, distance of the sample to each cluster center included in this fault region is found. The data belongs to the cluster with minimum distance, and the class of samples in this cluster determines the fault type of the related component.

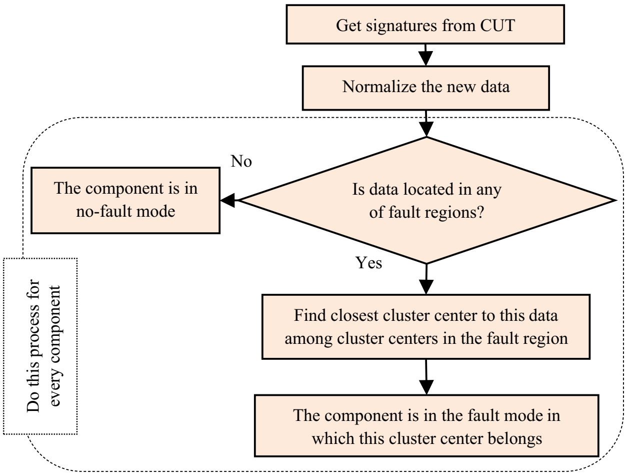
Get signatures from CUT
Normalize the new data
Is data located in any of fault regions?
No
The component is in no-fault mode
Yes
Find closest cluster center to this data among cluster centers in the fault region
The component is in the fault mode in which this cluster center belongs
Do this process for every component

Fig. 4 The on-line process of classifying a new data

3 A novel approach for test point selection

The more no-fault samples in fault regions leads to the more probability of misdiagnosing faulty components which is more destructive than misdiagnosing non-faulty components.

Main idea used in this paper is finding a test point set by which there are minimum amount of overlap between faults and no-fault classes. A solution to this problem is exhaustive search among test points using evolutionary algorithms. The fitness function may be the number of no-fault samples that are located in fault regions. Therefore, all of no-fault samples in each fault dictionary should be examined to find those located in fault regions.

In a circuit with n_c components and n_f fault modes for each component, the number of m-fold faults (N_F) is achieved by Eq. 1. No-fault class, in which all of components are non-faulty, should be added to N_F. Among these $N_F + 1$ classes, N_{fault} classes fall in each fault class and $N_{no-fault}$ classes fall in no-fault class for every component (Eqs. 2–3).

$$N_F = \frac{n_c!}{m!(n_c - m)} n_f^m \tag{1}$$

$$N_{fault} = \frac{(n_c - 1)!}{(m-1)!(n_c - m)!} \times (n_f)^{m-1} \tag{2}$$

$$N_{no-fault} = (N_F + 1) - n_f\left(\frac{(n_c - 1)!}{(m-1)!(n_c - m)!} \times (n_f)^{m-1}\right) \tag{3}$$

For example, in a typical circuits with 10 components, the number of double hard faults is N_F = 180 (m = 2 and n_f = 2, including short-circuit and open-circuit). These fault classes, as well as the no-fault class are divided into three classes for each component including short-circuit (n_{fault} = 18 classes), open-circuit (N_{fault} = 18 classes), and no-fault ($N_{no-fault}$ = 145 classes). By performing Monte Carlo analysis with 50 iterations in each simulation, there would be 900 samples in short-circuit (18 × 50 = 900), 900 samples in open-circuit class and 145 × 50 = 7250 samples in no-fault class. Based on our experiments, dealing with this large number of no-fault samples to calculate fitness function in exhaustive search for each component, may take several days to be performed. Although this process is performed before starting real test, but the long time vesting may affect marketing parameters like time-to-market.

Alternative method has been shown in Fig. 5. This is a combined exclusive-inclusive method. The percentage of no-fault samples located in fault regions is the criterion ($C(\%)$) to be minimized (Eq. 4).

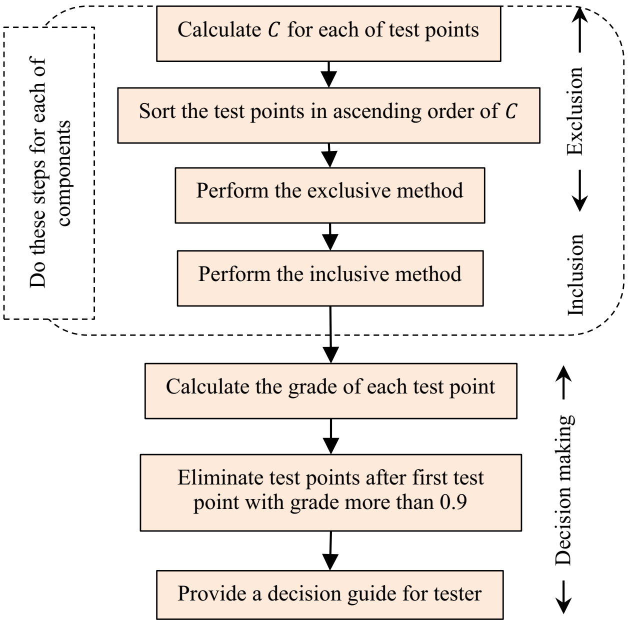
Calculate C for each of test points
Sort the test points in ascending order of C
Perform the exclusive method
Perform the inclusive method
Do these steps for each of components
Exclusion
Inclusion
Calculate the grade of each test point
Eliminate test points after first test point with grade more than 0.9
Provide a decision guide for tester
Decision making

Fig. 5 Test point selection process

$$C = \frac{Ns_{nfr}}{Ns_{nf}} \times 100 \tag{4}$$

where Ns_{nfr} is the number of no-fault samples located in the fault regions, and Ns_{nf} is the number of total no-fault samples. Steps of this algorithm are as follows.

3.1 Exclusion

After constructing the fault dictionaries by the measured DC node voltages at all of the accessible test points, the value of C is calculated for each test points in single-dimensional space. The test points are sorted with respect to the values of C in ascending order. Then, redundant test points are eliminated by exclusive method. In this way, the test point set is initialized to include all accessible test points and starting from last one (maximum to minimum value of C), a test point is eliminated in each iteration if two following conditions are met.

First, its elimination should not increase the value of C more than 1%. By this manner, the test points which do not create significant improvement in the value of C are eliminated.

The second condition is related to tighten the fault regions for no-fault samples (Sect. 3.1). No-fault samples located outside the tightened fault regions do not affect diagnosing accuracy of fault samples. However, those located inside the tightened regions may cause misclassifications in fault samples.

Typically, let's consider the two fault regions in Fig. 6. The samples of the fault regions are achieved from different test points. The right-sided fault region contains

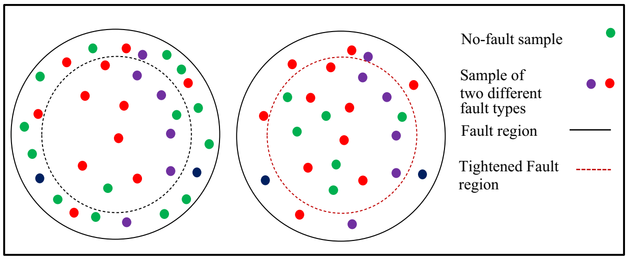

Fig. 6 Two fault regions in two different two-dimensional spaces

fewer no-fault samples than the left-sided fault region, but it contains more no-fault samples located in tightened fault region. Since the no-fault samples located out of the tightened regions are disregarded, the accuracy of diagnosing fault samples in the left-sided fault region is higher than the left fault region. To consider this effect, percentage of no-fault samples located in tightened fault regions ($C_t(\%)$) is calculated (Eq. 5).

$$C_t = \frac{Ns_{nft}}{Ns_{nf}} \times 100 \tag{5}$$

In which, Ns_{nft} is the number of no-fault samples located in the tightened fault regions. The second condition is that by excluding test point, the C_t should not increase more than 1%.

3.2 Inclusion

The effectiveness of selected test points is verified by inclusive method. In this way, the test point set is initialized to be null. Starting from the first test point in the selected set at the previous step, a test point is selected in each iteration if two conditions are met. First, including that test point should decrease the value of C more than 1%. The second condition is that including the test point should not increase the C_t.

Performing exclusive method before inclusive method speeds up the test point selection process. The reason is that inclusive algorithm is started with one node and may include most of test points to gradually improve C and C_t. However, exclusive algorithm is started with all nodes, that probably have better value of C and C_t than one node in inclusive algorithm. Therefore, it is more probable that redundant test points are eliminated in next iterations, and performing the inclusive algorithm with this reduced test point set take less time.

3.3 Decision making

Previous processes are performed for every component to find effective test point set for each of them. Thereafter, a grade is given to each test point that is equal to the number of components whose selected test point set include that test point.

The grades are sorted in descending order and cumulative sum of them are calculated by partially summing the grades. Let $\{g_1, \ldots, g_N\}$ be the cumulative sum of grades, where N is the number of test points and g_N is sum of all grades. Then they are manipulated as follows:

$$\{g_1^*, \ldots, g_N^*\} = \frac{\{g_1, \ldots, g_N\}}{g_N} \tag{6}$$

Values of g_i^* ($i = 1, \ldots, N$) are in interval [0,1]. Let g_t^* be first grade equal to or greater than 0.9. This means that test points related to grades g_1^* to g_t^* are adequate to diagnose at least 90% of components. Therefore, other ones are omitted and selected test points make the optimum test point set (S_{opt}).

Finally, it is useful to provide a decision guide for testing. For this purpose, starting from the first test point in S_{opt} and adding next test points in each iteration, parameters C and C_t are calculated for each component. Then, the parameters are averaged over components. The tester can decide which set is appropriate for the circuit. According to our previous experiences, a good choice is a set using which averaged C and averaged C_t is as follows:

$$C_{av} \approx 20\% \tag{7}$$

$$C_{tav} \leq \frac{\frac{Ns_f}{2}}{Ns_{nf}} \times 100\% \tag{8}$$

where C_{av} and C_{tav} are averaged C and averaged C_t over components respectively. By this choice, according to Eq. 7, on average, at most 20% of no-fault samples are located in fault regions. Therefore, average accuracy of 80% in diagnosing no-fault samples is guaranteed. Also, according to Eq. 8, the average number of no-fault samples located in tightened fault regions is half the number of fault samples which is reasonable choice to dominate the fault samples in fault regions. The test point selection method is more described in the next section using a benchmark circuit.

4 Experimental results

4.1 DC transistor circuit

Figure 7 shows an analog DC transistor circuit. In [22] only 6 predefined faults were considered for this circuit but here all the double hard faults are selected as predefined faults. There are two possible hard faults for resistors (short-circuit and open-circuit) and six hard faults for each transistor (three short-circuits in junctions and three open-circuits in leads). By considering all the related faults in a

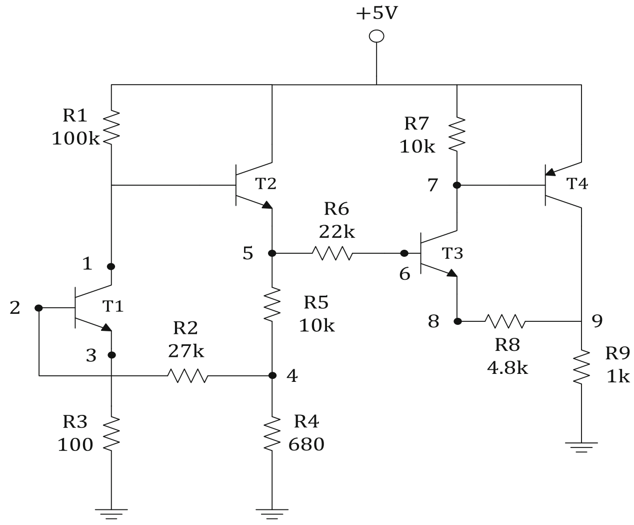

Fig. 7 Benchmark circuit used in this paper

transistor, each transistor can be assumed as 6 components as base–emitter, base–collector, collector–emitter junctions (with no-fault and short-circuit fault), and base, collector, emitter leads (with no-fault and open-circuit fault). Therefore, there are 33 components in Fig. 7, including 9 resistors and 24 transistor components.

According to above discussion for Fig. 7, we don't have same number of faults for each component and Eq. 1 is not applicable for fault calculation. If we want to use Eq. 1 for number of faults in Fig. 7, we should imaginary consider same number of faults for each component. To do this, we add open-circuit fault to each junction and short-circuit fault to each lead to reach $n_f = 2$ for all components. Now, using Eq. 1 we get 2112 faults for this circuit that 1259 of them are not real. Therefore, the number of double hard faults in Fig. 7 is 853, and adding no-fault mode to this list, the number of predefined faults and no-fault mode is 854.

According to other works, we consider 5% tolerance for the resistors. Open- and short-circuit faults were modeled by connecting a 100 MΩ resistor in series and paralleling a 0.01 Ω resistor, respectively.

Circuit simulations are done by HSPICE and classifiers are implemented with MATLAB. The Monte-Carlo analysis with 50 iterations is done for each of 854 predefined faults to measure DC voltage at all nodes. The fault dictionary for each component is constructed by the achieved data from simulations according to the discussion in Sect. 2.

Table 2 shows the sorted values of C for each component. In this table, B, C, E, BE, CE, and CB stand for Base, Collector, Emitter, Base–Emitter, Collector–Emitter and Collector–Base respectively.

In the next step, exclusive and inclusive algorithms should be performed for every component. Tables 3 and 4 show these processes for BE1. In these tables, acc_{nf} is rate of truly classified samples of no-fault class, and acc_f is rate of non-misclassified samples of fault classes in no-fault class that are defined as follows:

$$acc_f = 100 - \frac{Ni_{fnf}}{Ns_f} \times 100 \tag{9}$$

$$acc_{nf} = \frac{Nc_{nf}}{Ns_{nf}} \times 100 \tag{10}$$

where Ni_{fnf} is the number of fault samples incorrectly classified in no-fault class, Ns_f is total number of fault samples, Nc_{nf} is the number of correctly classified no-fault samples, and Ns_{nf} is the total number of no-fault samples.

Typically, by excluding node 7 in the first row of Table 3, the value of C is unchanged and increment of C_t less than 1%, so it could be discarded from the test point list. Continuing this exclusion process, finally just nodes 2, 9, and 4 are remained for inclusion process. According to Table 4, by inclusive process, the effectiveness of the selected nodes is verified. Because of significant improvement in C and C_t values by adding nodes 9 and 4, all of these nodes are selected for fault diagnosis of BE1 component.

Results of exclusion and inclusion processes for all of the components are shown in Table 5. According to this table, now node grading is done to determine the importance of each node in circuit fault diagnosis process (Table 6). According to the second row of Table 6, there are 23 components that require node 6, and 2 components which require node 5. The third row shows the cumulative sum of grades. Finally, the normalized grade of each node is determined in the last row. On the base of normalized grades of the nodes, node 3 is the first node with the grade of more than 0.9 and by adding nodes 4 and 5 there is not any significant improvement in the grade values. Consequently, nodes 4 and 5 can be discarded from the test point set. Therefore, nodes 6, 8, 2, 7, 9, 1, and 3 are most effective nodes for diagnosing almost all of components.

If access to all the selected test points is not possible, it is useful to recommend a decision guide for testing. This guide is shown in Table 7. The parameters in this table are averaged over the components. According to this table, we can see the fault diagnosis accuracy using the specified nodes. The average of C is decreased and so acc_{nf} is increased by including more nodes. The slow falling trend of acc_f in this table is because of rising trend of averaged C_t.

With reference to the criteria equations (Eqs. 7, 8), and regarding that $\frac{\frac{Ns_f}{2}}{Ns_{nf}} \times 100\% = 5\%$ in this circuit, the set $\{6, 8, 2, 7\}$ is appropriate test node set since the average C

Table 2 Sorted values of m and related test points

Component	Sorted test points									Sorted values of C (%)								
BE1	2	3	6	8	9	5	4	1	7	43.9	48.6	68.1	73	73.6	77.3	78	79.9	88
BE2	6	5	2	1	4	8	9	3	7	19.8	21.9	22.7	24.7	24.7	34.4	40.7	46	67.9
BE3	8	6	9	7	5	2	4	1	3	18.1	26.3	36.3	48.5	50.8	64	65.3	70.5	89.6
BE4	7	8	9	6	5	2	1	4	3	47.6	51.9	52.3	59.8	80	84.7	85.7	87.4	92.4
CE1	6	8	9	1	5	2	3	4	7	14.6	34.9	35	38.5	48.5	50.5	55.1	57.7	70.4
CE2	5	4	2	6	1	8	9	3	7	12.5	15.6	18.1	20.3	23.2	25.3	30.2	51.7	65.1
CE3	8	9	6	7	5	2	4	1	3	14.1	15.3	35.3	61.7	72.1	79.5	82	82.2	92.9
CE4	9	8	6	7	5	1	2	4	3	8.7	11.6	41.8	52.9	66.7	76.9	79.5	83.2	92.1
CB1	6	9	8	2	1	5	4	7	3	19.6	42.3	43.1	44.5	50.4	56.2	69.2	73.9	78
CB2	1	6	5	2	4	8	9	3	7	7.3	19.3	21.3	22.5	24.3	33.4	36.8	45.9	68.9
CB3	9	8	6	5	2	4	7	1	3	14.1	15.1	22.3	58.8	60.3	62.6	65.2	66.5	87.2
CB4	9	8	6	7	5	2	4	1	3	9.4	13.4	36.8	50.2	70.6	78.9	81.3	81.3	92.7
B1	3	6	2	8	9	5	1	4	7	42.5	69	69.5	72.1	73.4	78.5	79.6	80.9	87.2
B2	6	5	1	4	2	8	9	3	7	14.9	19.4	22.8	24.6	25.7	28.9	31	51.6	62.8
B3	8	6	9	7	5	1	2	4	3	32	37.5	37.9	55.1	71.7	74.8	82.1	85	91.5
B4	8	9	6	7	5	1	2	4	3	51.6	53.8	54.9	58.8	74.7	83.5	83.8	86.5	92.7
C1	6	8	9	2	1	5	4	3	7	66.8	72	73.1	74.3	75.2	76.3	78.6	81.7	86.5
C2	6	4	2	8	1	9	3	7	5	18.4	27.8	28.2	30.3	30.9	36.7	50.8	67.3	100
C3	8	9	6	7	5	1	2	4	3	38.9	40.4	41.5	51.5	67.6	76.3	81.5	85.3	90.9
C4	8	9	6	7	5	2	1	4	3	47	47.8	58.7	64.6	81.8	84.5	86.6	87	92.5
E1	3	2	6	8	9	5	4	1	7	35.8	67.9	70.2	73.8	74.7	78.9	79.1	80.4	87.9
E2	5	6	4	2	1	8	9	3	7	8.2	8.6	12.9	14.9	19.2	22.6	25.8	42.3	54.5
E3	8	9	6	7	5	1	2	4	3	29.9	34.8	38.8	49.2	77	79.2	82.2	85.4	91.5
E4	8	9	6	7	5	2	1	4	3	43.4	44.9	54.1	58.8	74.6	83.7	83.7	86.2	92.8
R1	1	6	5	2	4	8	9	3	7	10	17.2	17.7	21.8	22.8	30.6	35.7	43.9	66.2
R2	6	8	9	5	2	1	4	7	3	68.7	72.2	73.2	78.3	78.4	80.8	83.5	86.8	87.7
R3	3	6	8	9	2	5	1	4	7	38.5	71	75.1	76	76.6	81.8	83.3	87.3	89.1
R4	2	3	6	9	8	1	7	4	5	19.2	44.3	62.2	74.7	75.4	80	88.2	100	100
R5	5	6	4	2	1	8	9	3	7	6	12.6	19.7	23.6	26	35.4	46.2	47.9	71
R6	6	8	9	7	5	1	2	4	3	42.9	52.3	55.8	75.4	77.2	82.3	85.6	88.2	93
R7	9	8	7	6	5	2	1	4	3	55.8	59.1	61.7	70.8	83.6	85.1	87.4	88	92.4
R8	9	8	6	7	5	2	4	1	3	50.1	55.4	67.6	71.8	85.4	85.4	88	90.3	92.8
R9	9	8	7	6	5	2	4	1	3	23.6	34.7	55.8	55.9	83.7	84.4	87	88.3	92.9

Table 3 Exclusion process for BE1

Node set	Exclusion				
	C (%)	C_t (%)	acc_{nf} (%)	acc_f (%)	Endorsement
$\{2,3,6,8,9,5,4,1,7\}$	3.9	0.46	95.9	95.4	✔
$\{2,3,6,8,9,5,4,1\}$	3.9	0.47	96.1	95.2	✔
$\{2,3,6,8,9,5,4\}$	3.8	0.46	96.3	94.7	✔
$\{2,3,6,8,9,5\}$	5.1	0.47	94	96.3	×
$\{2,3,6,8,9,4\}$	3.7	0.55	96.1	95.4	✔
$\{2,3,6,8,4\}$	4.4	0	94	98	×
$\{2,3,6,9,4\}$	3.7	0.69	96.3	94.4	✔
$\{2,3,9,4\}$	3.7	0.08	95.7	97.5	✔
$\{2,9,4\}$	4.4	0	94.7	98.8	✔
$\{9,4\}$	46.5	2.82	48.2	90.7	×

Table 4 Inclusion process for BE1

Inclusion					
Node set	$C(\%)$	$C_t(\%)$	$acc_{nf}(\%)$	$acc_f(\%)$	Endorsement
$\{2\}$	41.4	0.86	57.9	100	✔
$\{2,9\}$	8.1	0.55	92.5	99.1	✔
$\{2,9,4\}$	5.7	0	94.7	98.8	✔

of this set is almost equal to 20% and average C_t is less than 5%.

If all of the nine test points are used, then average acc_{nf} and average acc_f are 85.2% and 92.9% respectively. Therefore, using $\{6,8,2,9\}$ test point set, there are about 56% reduction in the number of test points with just 3.9% reduction in acc_{nf} and 3.1% increment in acc_f. If the set in the last row of Table 7 is selected, the accuracy parameters

Table 5 Selected nodes by exclusive and inclusive algorithms

Component	Selected nodes by exclusive algorithm									Final selected nodes by inclusive algorithm								
BE1	2	9	4	–	–	–	–	–	–	2	9	4	–	–	–	–	–	–
BE2	6	1	–	–	–	–	–	–	–	6	1	–	–	–	–	–	–	–
BE3	8	6	–	–	–	–	–	–	–	8	6	–	–	–	–	–	–	–
BE4	7	8	6	2	–	–	–	–	–	7	8	6	2	–	–	–	–	–
CE1	6	2	3	–	–	–	–	–	–	6	2	3	–	–	–	–	–	–
CE2	6	1	–	–	–	–	–	–	–	6	1	–	–	–	–	–	–	–
CE3	8	6	–	–	–	–	–	–	–	8	6	–	–	–	–	–	–	–
CE4	9	7	–	–	–	–	–	–	–	9	7	–	–	–	–	–	–	–
CB1	9	2	–	–	–	–	–	–	–	9	2	–	–	–	–	–	–	–
CB2	1	6	–	–	–	–	–	–	–	1	6	–	–	–	–	–	–	–
CB3	8	6	–	–	–	–	–	–	–	8	6	–	–	–	–	–	–	–
CB4	9	7	–	–	–	–	–	–	–	9	7	–	–	–	–	–	–	–
B1	3	6	2	8	9	7	–	–	–	3	–	–	–	–	–	–	–	–
B2	6	1	–	–	–	–	–	–	–	6	1	–	–	–	–	–	–	–
B3	8	6	2	–	–	–	–	–	–	8	6	2	–	–	–	–	–	–
B4	8	6	7	2	–	–	–	–	–	8	6	7	2	–	–	–	–	–
C1	6	8	9	2	1	3	7	–	–	6	8	9	2	1	3	7	–	–
C2	6	1	–	–	–	–	–	–	–	6	1	–	–	–	–	–	–	–
C3	8	9	6	7	2	–	–	–	–	8	9	6	7	2	–	–	–	–
C4	8	6	7	2	–	–	–	–	–	8	6	7	2	–	–	–	–	–
E1	3	2	6	8	9	7	–	–	–	3	–	–	–	–	–	–	–	–
E2	5	1	–	–	–	–	–	–	–	5	1	–	–	–	–	–	–	–
E3	8	9	6	2	–	–	–	–	–	8	9	6	2	–	–	–	–	–
E4	8	6	7	2	–	–	–	–	–	8	6	7	2	–	–	–	–	–
R1	1	6	–	–	–	–	–	–	–	1	6	–	–	–	–	–	–	–
R2	6	8	9	2	7	3	–	–	–	6	8	9	2	7	3	–	–	–
R3	3	6	8	9	2	1	7	–	–	3	–	–	–	–	–	–	–	–
R4	6	4	–	–	–	–	–	–	–	6	4	–	–	–	–	–	–	–
R5	5	4	–	–	–	–	–	–	–	5	4	–	–	–	–	–	–	–
R6	6	8	7	2	–	–	–	–	–	6	8	7	2	–	–	–	–	–
R7	9	8	7	6	2	–	–	–	–	9	8	7	6	2	–	–	–	–
R8	9	8	6	7	2	–	–	–	–	9	8	7	–	–	–	–	–	–
R9	9	8	6	2	–	–	–	–	–	9	8	–	–	–	–	–	–	–

Table 6 Grades of nodes

Nodes	6	8	2	7	9	1	3	4	5
Sorted grades	23	17	15	13	12	8	7	3	2
Cumulative sum of grades	23	40	55	68	80	88	95	98	100
Normalized grades	0.23	0.4	0.55	0.68	0.8	0.88	0.95	0.98	1

Table 7 Decision guide of the benchmark circuit

Nodes set	Average $C(\%)$	Average $C_t(\%)$	Average $acc_{nf}(\%)$	Average $acc_f(\%)$
{6}	42.6	0.07	57.2	99.6
{6,8}	30	0.04	69.9	99.1
{6,8,2}	22.7	1.23	79.2	96.1
{6,8,2,7}	20.3	1.15	81.3	96
{6,8,2,7,9}	18.8	1.47	83.4	93.6
{6,8,2,7,9,1}	17.8	1.21	84.3	93.2
{6,8,2,7,9,1,3}	16.9	1.23	85.3	92.9

Using all of the nodes: average acc_{nf} = 85.2%, and average acc_f = 92.9%

will be same as when using all of the nine nodes, with about 22% reduction in the number of test points.

To verify the effectiveness of the selected test point set, one can discard any of the selected node to see its importance. This process is shown in Table 8 and degradation of diagnosis capability is demonstrated in it. Although some sets have higher acc_f, but decreasing of acc_{nf} is much more than increasing of acc_f for them.

4.2 Comparison with other methods

The previous works in this field are on the base of searching the best node set so that maximum number of predefined faults can be isolated. The number of predefined faults in those works cannot be very large, since the accuracy of isolating may be too low. For instance, the test point selection method proposed in [6] is examined on a band-pass filter with 11 nodes, 16 components, and 32 potential single hard faults (short-circuit and open-circuit for each component) from which 23 faults were selected as predefined faults. Its simulation results, lead to selecting 5 nodes from 11 nodes by which only 14 faults could be classified (60.9% diagnostic accuracy).

Table 9 shows the comparison results of the proposed method with the references [6, 7, 22] which are works in DC domain. The proposed method can classify very large number of predefined faults with highest accuracy using only 4 nodes that shows the efficiency of the proposed method specifically when the number of predefined faults is very large.

The process time for our method is about 35 min that is very faster than using exhaustive search that needs multiple days for best test point selection.

5 Conclusion and future work

A test point selection method using combined exclusive-inclusive algorithm was introduced for analog circuits with large numbers of predefined faults. In this method it is supposed that a classifier is designed for each of circuit components, and most effective test points that make significant improvement in accuracy of every classifier are selected. Based on the experimental results 4 nodes from 9 circuit nodes were selected using which average acc_f and acc_{nf} of the components are 96% and 81.3% respectively.

Table 8 Verifying the effectiveness of selected test points (↓ and ↑ mean decreasing and increasing comparing with selected node set)

Nodes set	Average $C(\%)$	Average $C_t(\%)$	Average $acc_{nf}(\%)$	Average $acc_f(\%)$
{6,8,2,7} (Selected node set)	20.3	1.15	81.3	96
{8,2,7}	24	0.73	76.8 (↓ 4.5)	96.5 (↑ 0.5)
{6,2,7}	24.3	1.31	77.8 (↓ 3.5)	94.8 (↓ 1.2)
{6,8,7}	27.2	0.33	73 (↓ 8.3)	98 (↑ 2)
{6,8,2}	22.7	1.22	79.2 (↓ 2.1)	96.1 (↑ 0.1)

Table 9 Results of comparing the proposed method with other works

Method	No. of predefined faults	No. of selected nodes	Accuracy of fault diagnosis	
[7]	17	4 of 12	70.6%	
[6]	23	5 of 11	60.9%	
[22]	6	11 of 11	96.8	
Proposed method	854	4 of 9	83% (no-fault)	96% (fault)

These nodes are used for diagnosing 854 predefined faults (as well as no-fault mode) containing all of double hard faults.

Due to computational burden of calculating the criterions, exhaustive search was not used in this paper. Therefore, it is not claimed that the proposed method can find global optimum solution. However, the method aimed to find most effective test points that make significant improvement in circuit diagnosing. Test points that have little impact on the criterions are eliminated to reduce the number of required test points.

Finally, it is worth noting that although the proposed method was used for a DC analog circuit, it has the potential of being used for time or frequency domains. Steps of the algorithm may be applied on time samples or frequency points of circuit's frequency response to select the optimum set. This idea will be examined in future works.

References

1. Bandler, J. W., & Salama, A. E. (1985). Fault diagnosis of analog circuits. *Proceedings of the IEEE, 73,* 1279–1325.
2. Prasad, V. C., & Babu, N. S. C. (2000). Selection of test nodes for analog fault diagnosis in dictionary approach. *IEEE Transaction on Instrumentation and Measurement, 49,* 1289–1297.
3. Starzyk, J. A., Liu, D., Liu, Z.-H., Nelson, D. E., & Rutkowski, J. O. (2004). Entropy-based optimum test points selection for analog fault dictionary techniques. *IEEE Transaction on Instrumentation and Measurement, 53*(3), 754–761.
4. Yang, C., Tian, S., Long, B., & Chen, F. (2010). A novel test point selection method for analog fault dictionary techniques. *Journal of Electronic Testing, 26*(5), 523–534.
5. Yang, C., Tian, S., Long, B., & Chen, F. (2011). Methods of handling the tolerance and test-point selection problem for analog-circuit fault diagnosis. *IEEE Transaction on Instrumentation and Measurement, 60*(1), 176–185.
6. Zhao, D., & He, Y. (2015). A new test point selection method for analog circuit. *Journal of Electronic Testing, 31,* 53–66.
7. Ma, Q., He, Y., Zhou, F., & Song, P. (2018). Test point selection method for analog circuit fault diagnosis based on similarity coefficient. *Mathematical Problems in Engineering, 2018,* 1–11.
8. Yang, C., Tian, S., & Long, B. (2009). Test points selection for analog fault dictionary techniques. *Journal of Electronic Testing, 25,* 157–168.
9. Zhao, D., & He, Y. (2015). A new test points selection method for analog fault dictionary techniques. *Analog Integrated Circuits and Signal Processing, 82,* 435–448.
10. Saeedi, S., Pishgar, S. H., & Eslami, M. (2019). Optimum test point selection method for analog fault dictionary techniques. *Analog Integrated Circuits and Signal Processing, 100*(1), 167–179.
11. Cui, Y., Shi, J., & Wang, Z. (2016). Analog circuit test point selection incorporating discretization-based fuzzification and extended fault dictionary to handle component tolerances. *Journal of Electronic Testing, 32,* 661–679.
12. Huang, J. L., & Cheng, K. T. (1997). Analog fault diagnosis for unpowered circuit boards. In *International test conference, Washington*.
13. Huang, J. L., & Cheng, K. T. (2000). Test point selection for analog fault diagnosis of unpowered circuit boards. *IEEE Transaction on Circuits and Systems II, 47*(10), 977–987.
14. Lei, H., & Qin, K. (2014). Greedy randomized adaptive search procedure for analog test point selection. *Analog Integrated Circuits and Signal Processing, 79,* 371–383.
15. Golonek, T., & Rutkowski, J. (2007). Genetic-algorithm-based method for optimal analog test points selection. *IEEE Transaction on Circuits and Systems II, 54*(2), 117–121.
16. Jiang, R., Wang, H., Tian, S., & Long, B. (2010). Multidimensional fitness function DPSO algorithm for analog test point selection. *IEEE Transaction on Instrumentation and Measurement, 59*(6), 1634–1641.
17. Lei, H., & Qin, K. (2013). Quantum-inspired evolutionary algorithm for analog test point selection. *Analog Integrated Circuits and Signal Processing, 75,* 491–498.
18. Zhao, D., & He, Y. (2015). Chaotic binary bat algorithm for analog test point selection. *Analog Integrated Circuits and Sigal Processing, 84*(2), 201–214.
19. Luo, H., Lu, W., Wang, Y., & Wang, L. (2017). A new test point selection method for analog continuous parameter fault. *Journal of Electronic Testing, 33*(3), 339–352.
20. Khanlari, M., & Ehsanian, M. (2017). An improved KFCM clustering method used for multiple fault diagnosis of analog circuits. *Circuits Systems and Signal Processing, 36,* 3491–3513.
21. Tax, D., & Duin, R. (2004). Support vector data description. *Machine Learning, 54,* 45–66.
22. Tan, Y., He, Y., Cui, C., & Qiu, G. (2008). A novel method for analog fault diagnosis based on neural networks and genetic algorithms. *IEEE Transactions on Instrumentation and Measurement, 57*(11), 2631–2639.

Masoumeh Khanlari received the B.S. degree in electrical engineering from Babol Noshirvani University of Technology in 2005 and M.Sc. degree in electrical engineering from Tarbiat Modares University in 2008. She is currently pursuing her Ph.D. degree in electrical engineering from K.N. Toosi University of Technology. She is currently working as lecturer in electrical department at Islamic Azad University of Sari. Her current research includes analog circuits fault diagnosis.

Mehdi Ehsanian received the M.Sc. degree in electrical engineering from Sharif University of Technology in 1988, and Ph.D. degree in electrical engineering from University of Montreal in 1998. He was with INTEL until 2008 (10 years). He is currently working as assistant professor in Electrical Engineer department at K.N. Toosi University of Technology. His current research includes analog circuits, RF design, frequency synthesizers, clock and data recovery, and data converters.