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A 230 µW built-in on-chip auto-calibrating RF amplitude detector in 65 nm CMOS

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Abstract
In this paper, a built-in-self-calibration RF amplitude detector circuit in 65 nm CMOS is presented. The proposed architecture makes use of two detector replicas with a feedback control system to perform the self-calibration. The system is capable of detecting RF peak amplitudes range of 0–0.6 V_p with a conversion gain of − 3 V/V. The proposed system has a wide dynamic range that can auto-corrects the RF detector to less than 10% across process and temperature variations. This architecture is implemented in standard 65 nm 1P7 M CMOS process. Comprehensive silicon measurement results show that the self-calibration structure improves the detection error of the non-calibrated RF amplitude detector by a maximum of 71% at only 230 µW overall power consumption. The proposed system can be used to calibrate the variations in circuits within an RF transceiver such as LNA, Mixers, oscillators etc.

Keywords Amplitude detector · Built-in-self-test (BiST) · Detection error · RF detector and variability compensation

1 Introduction

The increasing need for CMOS miniaturization to achieve smaller and faster RF chips as well as process, temperature, and supply voltage variability, have been a challenge in reference to yield of first-time-right-silicon RF chips. In addition to test challenges, with finer geometries, the performance of RF circuits is susceptible to effects of process variation, noise coupling and temperature fluctuations. As such, the cost of testing RF chips has increased significantly which at some stage, the testing cost surpasses the fabrication cost of the chip itself [1]. Therefore, the push towards built-in-self-test/calibration (BIST), where testing and calibrating are realized on-chip, could largely reduce the cost of testing. One approach that has been largely followed is to use an RF amplitude detector to calibrate RF circuits thereby reduce the testing cost.

Converting peak amplitude, power or RMS amplitude to equivalent dc voltage has been implemented in board level [2, 3]. Moreover, several ways of implementing the RF amplitude detector have been reported in the literature [4, 5]. RMS detectors realized in CMOS [6] require complex signal processing implementation which limits the operating frequency. A dynamic range of 10 dB is reported in [7]. Rectification through a single diode-connected transistor principle is also utilized to implement detectors with a dynamic range of 20 dB [8, 9]. In order to obtain a higher dynamic range, amplification before converting to DC was proposed in [10, 11]. In case of large gain and wider dynamic range is required, this technique is not suitable because of the limited frequency bandwidth by the amplifier preceding the actual RF detector.

These works targeted the detection range and conversion gain improvement [12]. Most of the reported designs assumed the RF detector is immune to the variable PVT

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conditions [4] or calibrated off-chip. Moreover, no work has been done to consider the significant detection error inside the RF amplitude detector itself.

This paper is organized as follows. The operating principle of the RF detector is presented in Sect. 2. Section 3 describes the sources of detection error in the RF detector. The two-point calibration technique is described in Sect. 4. Moreover, the proposed self-calibrating architecture is presented in Sect. 5. The implemented silicon measurement results verify the performance of the proposed structure in Sect. 6. Section 7 demonstrates an example application of VGA gain calibration. Finally, Sect. 8 summarizes the performance and draws the conclusion.

2 RF amplitude detector

The RF amplitude detector shown in Fig. 1 [7] consists of the main core detector and LPF. The main core detector translates the high-frequency input to low frequency (dc) current, and the LPF averages out its value to a digital-friendly DC voltage. The varying levels of DC output are then used to generate the self-calibrating bias levels.

The input transistor M_n is biased to operate in the weak inversion region. This offers high transconductance (g_m) which is reflected in the high sensitivity V-I curve on top of the low power consumption. High sensitivity enables the detector to sense a wider range of inputs. The input is ac coupled to allow separate bias of M_n.

Understanding the relationship between the input amplitude and the DC output is essential. The derivation of the relationship was investigated in [5]. The drain current can be expressed as [5]:

$$I_n = I_{DO}\left(\frac{W}{L}\right)_n \exp\left(\frac{V_{GS}}{nV_T}\right) \tag{1}$$

where I_{DO} = is the process dependent current constant, $(W/L)_n$ is the aspect ratio of M_n, n is a constant related to depletion region characteristics, V_T is the thermal voltage

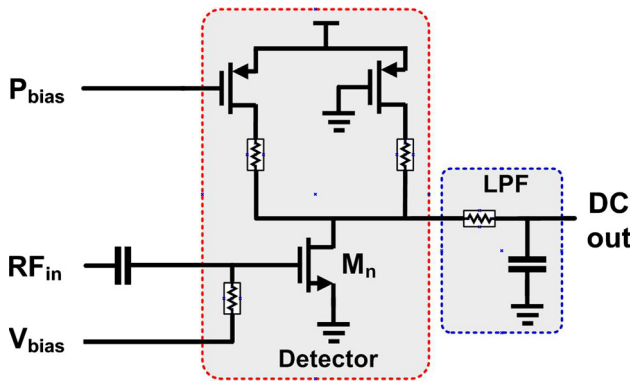

Fig. 1 RF amplitude detector

The high-frequency input which can be represented as $V_a\cos(\omega t)$ superimposed with the V_{bias} will constitute the V_{GS} component of (1). Replacing V_{GS} with $V_{bias} + V_a\cos(\omega t)$ will result in (2).

$$I_n = I_{DO}\left(\frac{W}{L}\right)_n \exp\left(\frac{V_{bias} + V_a\cos(\omega t)}{nV_T}\right) \tag{2}$$

$$I_n = I_{DO}\left(\frac{W}{L}\right)_n \exp\left(\frac{V_{bias}}{nV_T}\right)\exp\left(\frac{V_a\cos(\omega t)}{nV_T}\right)$$

$$I_n = I_{BO}\left[1 + \frac{V_a}{nV_T}\cos(\omega t) + \frac{1}{2}\left(\frac{V_a}{nV_T}\right)^2\cos^2(\omega t)\right]$$

$$I_n = I_{BO}\left[1 + \left(\frac{V_a}{2nV_T}\right)^2 + \frac{V_a}{nV_T}\cos(\omega t) + \left(\frac{V_a}{2nV_T}\right)^2\cos(2\omega t)\right]$$

where $I_{BO} = I_{DO}\left(\frac{W}{L}\right)_n \exp\left(\frac{V_{bias}}{nV_T}\right)$

I_{BO} is the dc bias current of the transistor. The increase in the amplitude of the high-frequency input (V_a) will result in an increment of the drain current I_n. The drain voltage is then pulled away from V_{DD} causing the output node, charged initially to V_{DD} to discharge, thus establishing a negative relation with respect to the RF signal amplitude. As the output is low pass filtered the effective component is the dc component of I_n. The ideal inverse relationship is depicted in Fig. 2(a). Detection range is the input voltage range of RF amplitude at which the detector response is linear. Similarly, the conversion gain (also called RF-to-dc conversion gain) is the slope of the characteristics. Proper sizing of the PMOS load and input devices enable a high conversion gain.

As the supply voltage is limited, increasing the conversion gain can only be achieved at a cost of the detection/dynamic range as shown in Fig. 2(b). A sub-range approach can easily be implemented to achieve both high conversion gain and wider dynamic range. Keeping M_n in the weak inversion region applying several V_{bias} values will result in linear regions for specific sub-range of RF

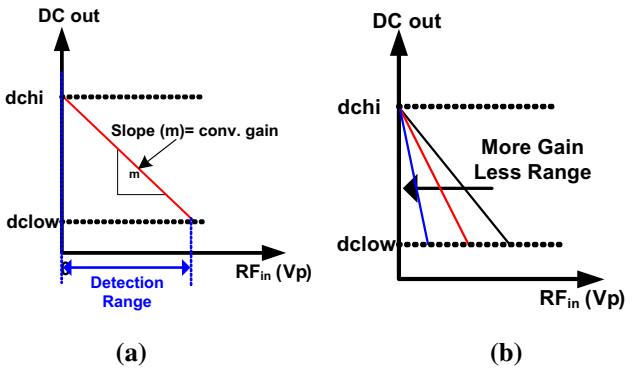

Fig. 2 **a** Ideal characteristics, **b** relationship between detection range and conversion gain

amplitudes as shown in Fig. 3. The aggregate result is extended detection range and high conversion gain.

The sub-range technique divides the whole dynamic range into sub-ranges where each sub-range section has a linear region with the highest possible conversion gain. Moreover, there is an overlap of dynamic range between adjacent sub-ranges. The sub-ranges are achieved by applying several V_{bias} to obtain linear region for a specific range. For example, by decreasing the gate bias, higher amplitude signals are needed to turn the input transistor on and vice versa thereby guarantee a region with high conversion gain and aggregated highest dynamic range possible. V_{bias} voltages from 350 up to 500 mV with an increment of 50 mV is selected to achieve 4 sub-ranges with an overlap of about 30 mV.

Wide dynamic range, higher RF to DC conversion gain are some of the key design specifications for RF detector design [7]. In typical self-calibration of complex RF systems, multiple RF amplitude detectors are required. The minimal power consumption of the detectors is, therefore, an essential parameter to consider. Since the main purpose of this detector is to be used as a sensing circuit in complex RF systems, to avoid loading the system, the high input impedance is also one of the main requirements of the detector design.

3 Detection error

The RF amplitude detector's characteristics deviate from its nominal under varying PVT conditions. To have clearer insight about the effect of PVT, the drain current versus drain voltage characteristics of a typical 120 nm/60 nm CMOS is simulated. The simulation was conducted in the 65 nm node. Several corner simulations at different temperature levels were conducted. Figure 4 shows the deviation of the characteristics from nominal values for

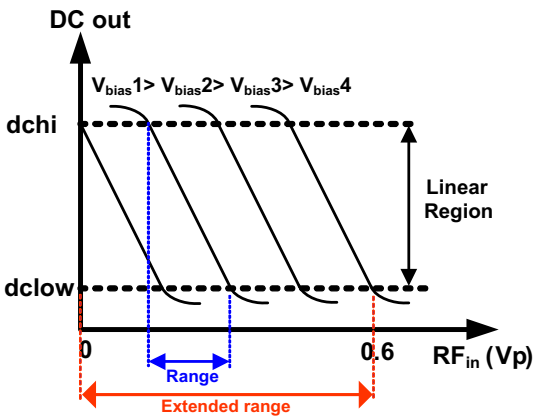

Fig. 3 Extended range RF amplitude detector characteristics

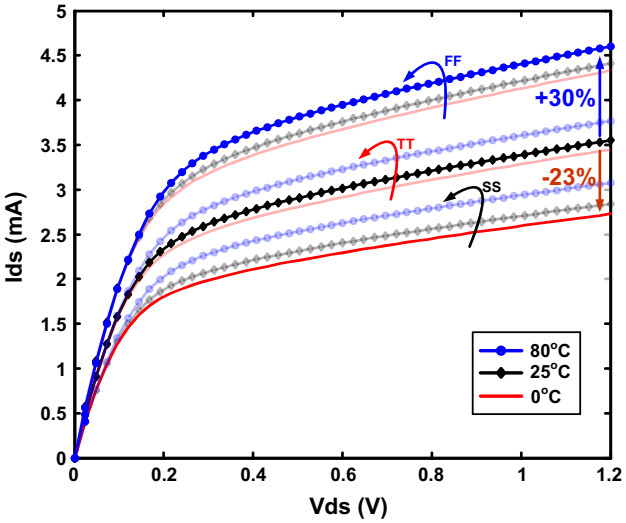

Fig. 4 Effect of PVT on IV characteristics of CMOS

different process and temperature conditions. A maximum deviation of + 30% was observed. The RF amplitude detector structure is composed of CMOS transistors and passive components. The deviation from the nominal characteristics of these components will produce an aggregate deviation of the RF detector characteristics.

To quantify and analyze the detection error within the RF detector, the detector response at various process and temperature corners are simulated. Detection error can be evaluated in two ways. For a constant RF input amplitude, the percentage dc output deviation from the nominal characteristics is one possible way of detection error. Four values of V_{bias} (500 mV down to 350 mV in steps of 50 mV) are selected to implement the sub-range approach discussed in Section II. The DC detection error (ε_{dc}) can be expressed as:

$$\varepsilon_{dc} = \frac{DC_{nom} - DC_{cor}}{DC_{nom}} \tag{3}$$

where DC_{nom} is the simulated nominal detector output at room temperature and TT process corner, DC_{cor} is the detector output at a varying corner and temperature conditions

Figure 5 shows SPICE simulation of the detector characteristics at 1 GHz RF input highlighting the maximum detection errors for four V_{bias} values. The nominal simulation was conducted at 25 °C TT process corner. The worst-case corner simulations were also performed. Using (3) the detection error was estimated for all sub-ranged simulations. A maximum detection error of 57% at 500 mV V_{bias} was observed.

The second way of looking at the detection error is; the different RF amplitude inputs that correspond to a fixed DC

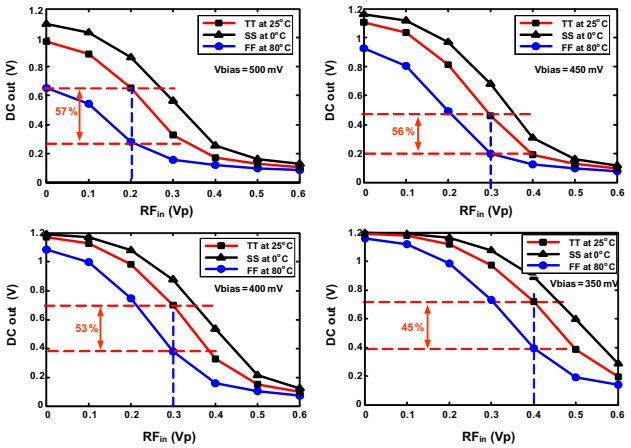

Fig. 5 Simulated RF amplitude detector dc detection error at different values of V_{bias}

output. We will refer to this error as input amplitude detection error (ε_{in}) and is expressed as:

$$\varepsilon_{in} = \frac{V_{anom} - V_{acor}}{V_{anom}} \tag{4}$$

where V_{anom} is the amplitude of RF input with the detector simulation conditions at room temperatures and TT process corner. V_{acor} is the amplitude the RF input with varying corner and temperature simulation conditions.

A maximum detection error as high as 81% is observed as shown in Fig. 6. These significant detection errors must be rectified before the RF detector can be used to calibrate complex systems.

A Monte-Carlo simulation for 1000 samples is also performed. The process, mismatch and temperature conditions are simulated under the Monte-Carlo setup. 1000 detection error samples for V_{bias} levels of 350–500 mV is simulated across several RF amplitude inputs. The detection error for all bias levels is presented in Fig. 7. A 75% detection error is measured at 450 mV V_{bias} and 0.4 V RF input.

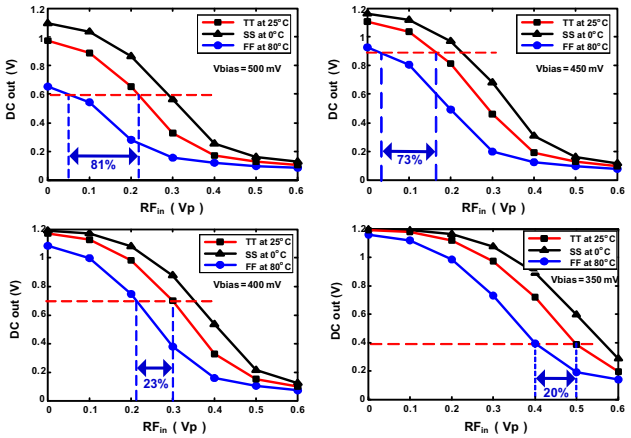

Fig. 6 Simulated RF amplitude detector input detection error at different values of V_{bias}

To investigate the detector response for a wideband RF input, the characteristics of the detector for 1 GHz, 10 GHz, and 30 GHz is simulated. Moreover, the four sub-ranged modes are simulated for these wideband RF inputs. An interesting observation can be made with respect to the input RF frequency. The conversion gain and the general behavior of the detector is consistent for the wideband RF input. The simulated results are depicted in Fig. 8.

4 Two point calibration

Few approaches which consider the effect of variation due to PVT conditions have been proposed in the literature. The attempt to mitigate this variation using a digitally assisted technique proposed in [13], which disconnects the detector input in the offset acquiring stage. This technique fails to provide a continuous calibration.

A two-point calibration shown in Fig. 9 [14] which is proposed in this paper provides a more suitable solution. The idea is to anchor the output of the RF detector at the extremes, to constant references. The detector response to zero amplitude RF input is anchored to a reference denoted as d*chi*. Similarly, the detector dc output when a maximum RF amplitude input is applied is anchored to a constant dc output denote by d*clow*. Therefore, the output of the detector is frozen to these two points even with the PVT variations. Thereby mitigating the detection error to its minimal possible values.

5 Proposed self-calibrating RF detector

The RF detector extracts parameters related to the auto-calibration of the RF component under test. This could be the gain information of an LNA, phase noise of an oscillator or mismatch of a mixer. As demonstrated in the previous sections, the detection error within the detector itself is significantly large to ignore. If the detector's error is not compensated, it could result in wrong extraction of parameters the detector is supposed to extract.

The two-point calibration technique described in the previous section (Fig. 9) is implemented to auto-calibrate the RF amplitude detector. Two replicas of the main detector which can generate bias voltages to achieve the two anchoring points are proposed.

5.1 Zero RF replica

Figure 10 shows one of the replicas denoted as Zero RF replica. Under the normal operating condition, when the

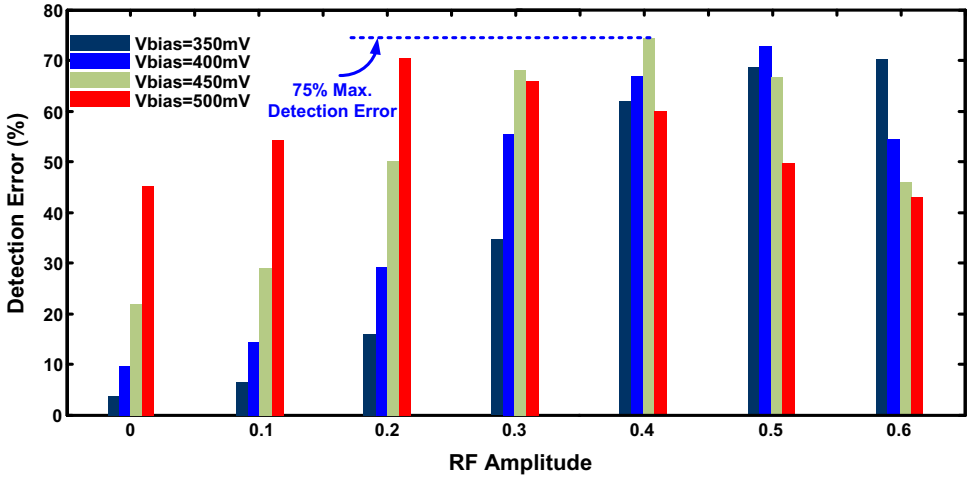

Fig. 7 Monte-Carlo (1000 samples) simulation for uncalibrated RF amplitude detector output

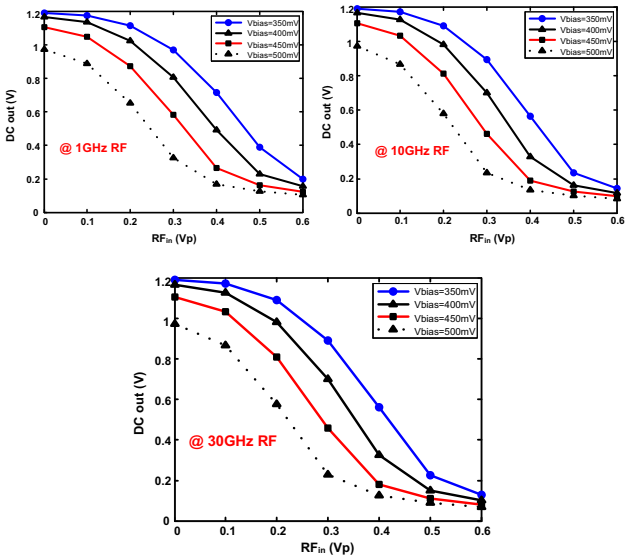

Fig. 8 Simulated RF amplitude detector response for 1, 10 and 30 GHz RF input

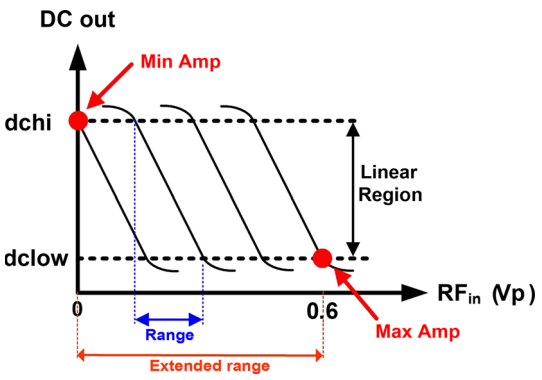

Fig. 9 Two-point calibration technique

RF input amplitude is 0 V the detector output is 1 V_{dc}. The main purpose of the Zero RF replica is to generate a gate bias voltage that forces the output to 1 V_{dc} irrespective of the PVT conditions.

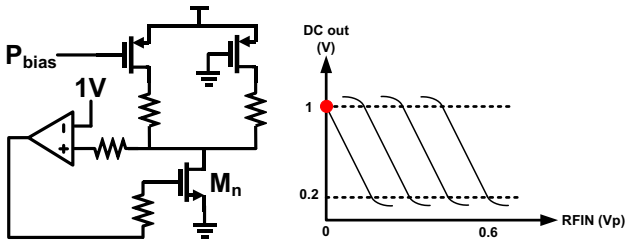

Fig. 10 Implemented Zero RF replica and its Minimum RF anchoring characteristics @ 1.2 V supply

The dc coupling capacitor can be ignored for this replica since there is 0 V amplitude RF input. The output of the replica is compared to a fixed 1 V_{dc} reference, which through feedback adjusts the replica's gate voltage to force the appropriate bias point to generated detector output of 1 V_{dc} at all times.

5.2 Max RF replica

The Max RF replica is presented in Fig. 11. Similarly, the purpose of this replica is to generate PVT variation independent P_{bias} for the main detector. To imitate the Max RF case, the replica is supplied with a 5 GHz rail to rail

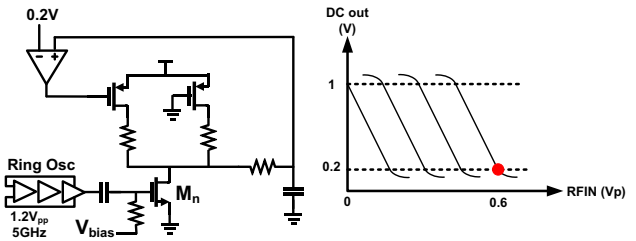

Fig. 11 Implemented Max RF replica and its Max RF anchoring characteristics

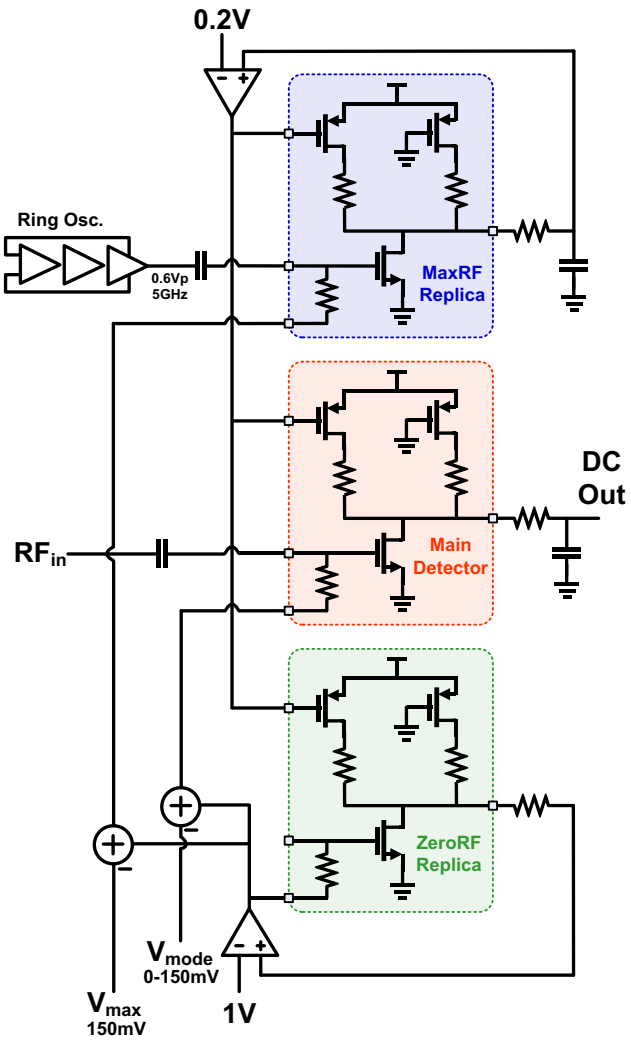

Fig. 12 Implemented self-calibrated RF amplitude detector

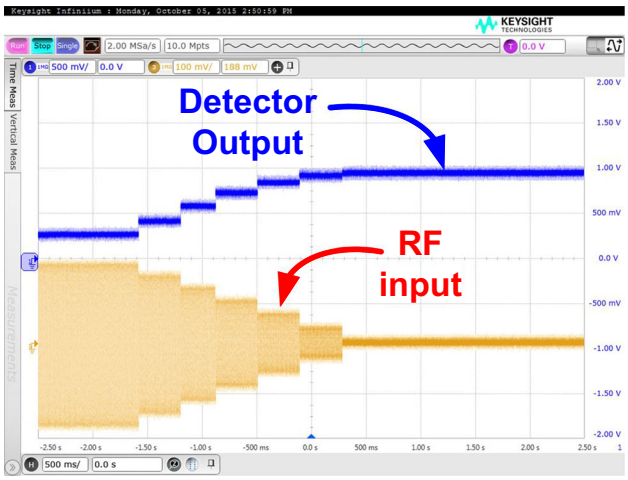

Fig. 13 Measured output of the self-adjusting structure

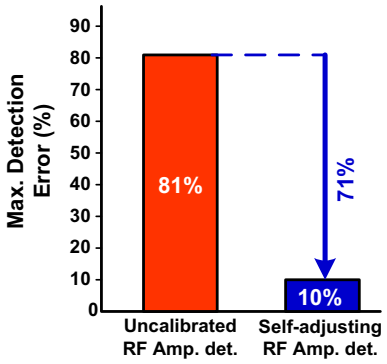

Fig. 14 Detection error mitigation summary

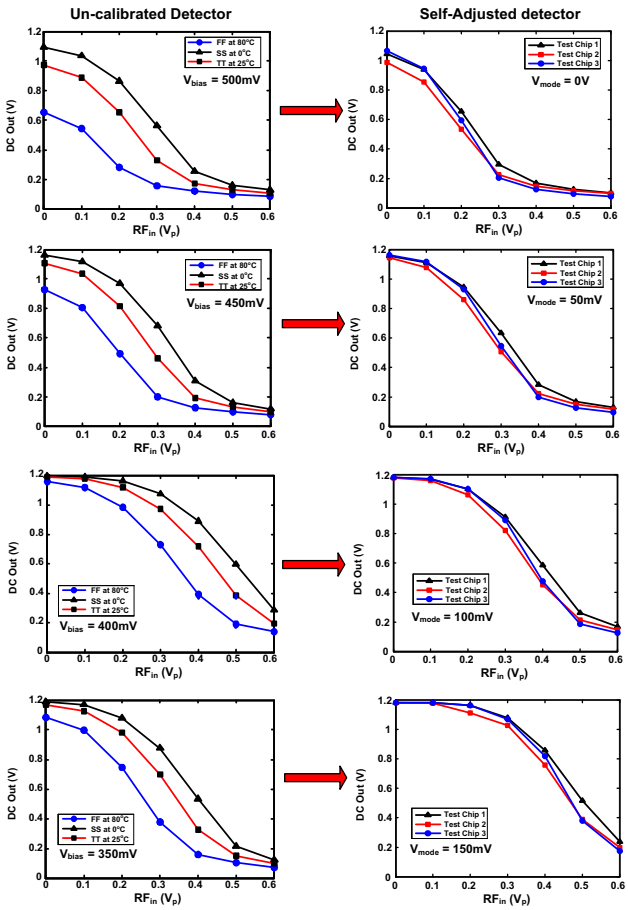

Fig. 15 Measurement results for self-adjusting structure compared to uncalibrated RF detector for all modes

(1.2 V_{pp}) input generated from a ring oscillator. The ring oscillator with a supply voltage of 1.2 V generates 5 GHz at 50% duty cycle output. An in-depth investigation is conducted to analyze the effect of the ring oscillator

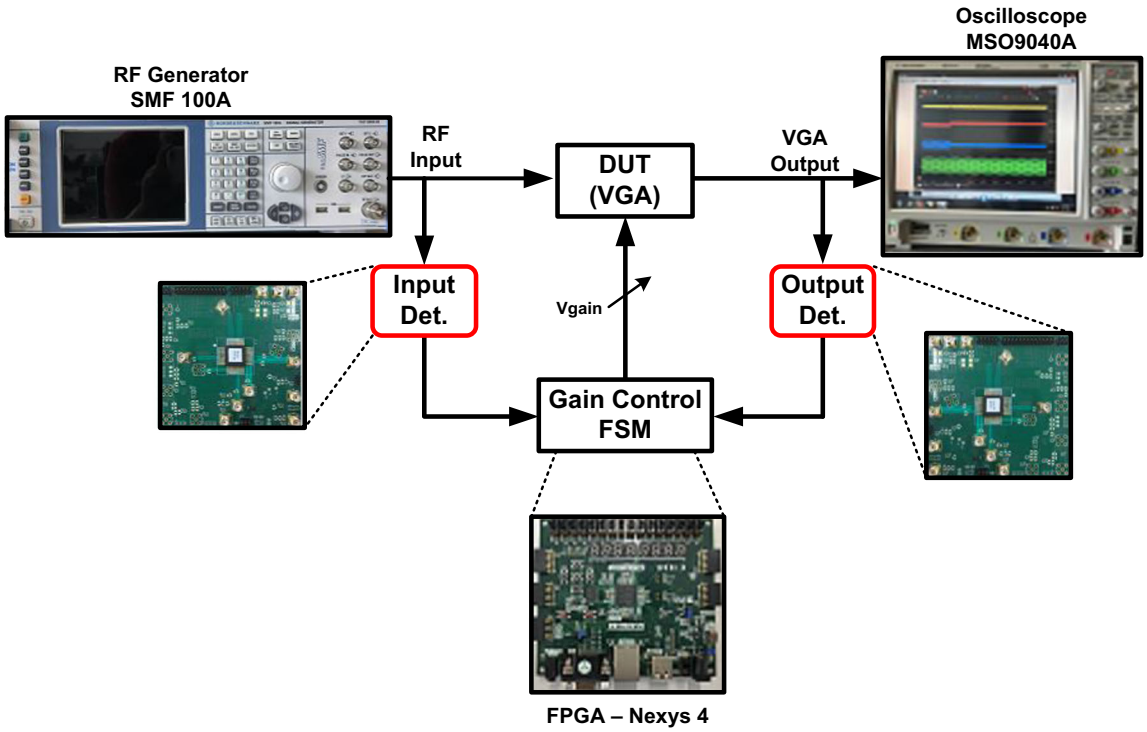

Fig. 16 Measurement setup

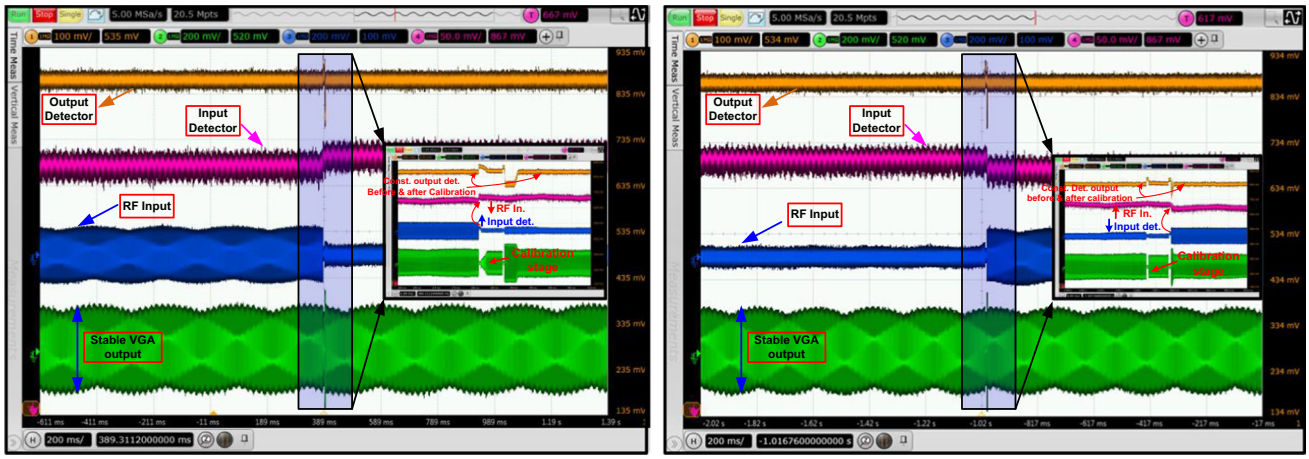

Fig. 17 Measured Variable gain calibration for (**a**) HIGH to LOW RF input transition and (**b**) LOW to HIGH RF input transition

frequency and duty cycle. The results show the replica is insensitive to the ring oscillator's frequency or duty cycle.

The nominal output of the detector at 0.6 V_p RF input amplitude is 0.2 V_{dc}. This output is compared to a fixed 0.2 V reference. The feedback loop forces the load such that the output is anchored at 0.2 V_{dc} regardless of the PVT conditions. Therefore, the two-point calibration can be achieved by means of the Zero RF and Max RF replicas. The complete self-calibrating structure is presented in the following section.

5.3 Complete self-calibrating structure

The proposed complete self-calibrating structure consists of the main detector, Zero RF replica and Max RF replicas as shown in Fig. 12. In the top-level layout, the replicas are placed in proximity to the main core to reduce variations. Moreover, all the cores' input devices are sized at much larger than minimum length to have better matching between all copies. Analog subtractor is inserted at the feedback to enable a programmable mode select.

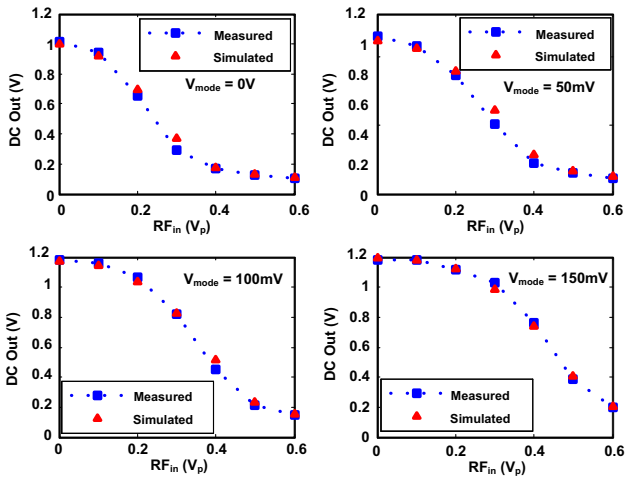

Fig. 18 Silicon measurement vs. SPICE simulation for Self-adjusting structure for the four modes of operation

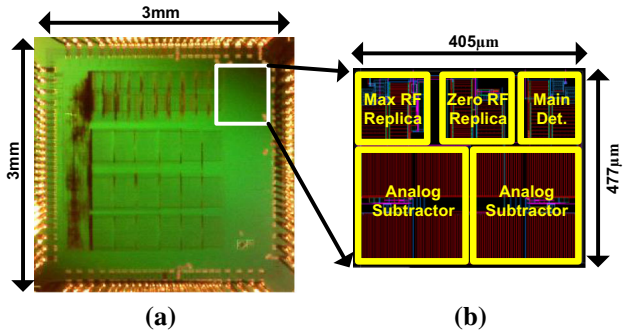

Fig. 19 **a** Chip die photo, **b** layout showing different parts of the system

There are four modes of operation to implement the extended dynamic range. V_{mode} is swept from 0 to 150 mV in steps of 50 mV. When V_{mode} is 0 mV which corresponds to the first mode, the bias voltage for the main detector is solely generated from the Zero RF replica. As described in section V, the zero RF replica will generate a bias voltage to anchor the main detector's output at 1 V_{dc}.

To stabilize the detector at the end of its characteristic curve, the Max RF replica is used as part of the self-calibration structure. At V_{mode} of 150 mV which corresponds to the fourth mode, the Max RF replica feedback loop forces the loads such that the output is anchored at 0.2 V_{dc}.

6 Measurement results

The proposed architecture is implemented in 65 nm 1P7 M CMOS process. Several samples were taken to verify the functionality of the structure. Figure 13 demonstrates the functionality of the self-adjusting structure. The staircase output represents the inverse relationship of the detector output to the RF input. Figure 14 summarizes the mitigation of detection error.

The comparison of the RF amplitude detector before and after the self-calibration technique is presented in Fig. 15. The measurement is performed at 1 GHz RF input for several chip samples. The characteristics are anchored at the extremes with measured detection error mitigated to a level of less than 10% for all modes of operation. The 10% detection error could possibly be from the mismatching between the replicas and the variation within the replicas itself.

7 Application demonstration

The RF amplitude detector can be used to extract specific parameters in complex RF systems. These parameters can be used for the self-calibration purpose. A variable gain amplifier auto-gain control with the help the proposed RF detector is demonstrated in this section. An off-chip AD8331 variable gain amplifier is used as the DUT. The gain of the AD8331 is controlled by an analog gain control pin denoted as V_{gain}.

The measurement setup for this case is shown in Fig. 16. The input detector continuously monitors the RF input amplitude level. Similarly, the output detector monitors the VGA output amplitude. The monitored input and output amplitude levels are analyzed in a digital processing unit (FPGA). Initially, the VGA output at a 50 mVp RF input is measured the stored. Then a continuous gain control FSM generates the required V_{gain} to adjust the VGA gain.

The measurement results for the VGA gain self-calibration are shown in Fig. 17. Figure 17(a) shows a calibration process for RF input transition of high to low. The RF input is dropped from 200 to 50 mV. The corresponding input detector's output is then increased. V_{gain} then alternates until the VGA output is set to a fixed value. This is demonstrated by the stable VGA output and constant output detector's DC output. Similarly, when RF input increases from 50 up to 200 mV, the corresponding input detector's output is then decreased. The calibration then sets the required V_{gain} to fix the VGA output to a stable predetermined output. The silicon measurement for four modes of operation is compared with the simulation results as shown in Fig. 18. The measurement fits well with simulation with minimal difference.

8 Conclusion

This paper demonstrated the proposed architecture self-calibrates to mitigate the detection error that arises due to PVT variations from within ordinary RF detector. A wide

range amplitude detector with − 3 V/V conversion gain is implemented. Two-point calibration technique is implemented to reduce the detection error within the detector itself. Two replicas with feedback control systems are implemented to generate the two-point calibration bias. The silicon measurement result shows that the detection error is mitigated to less than 10% from 81% for both dc detection error (ε_{dc}) and input detection error (ε_{in}). At a typical supply voltage of 1.2 V, the overall power consumption of the proposed architecture is 230 μW with only 0.2 mm^2 active area consumption as shown in Fig. 19.

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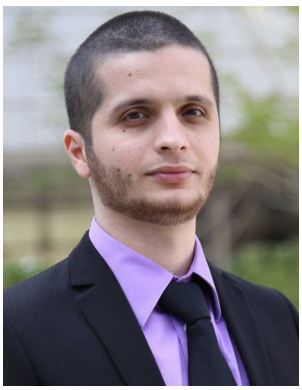

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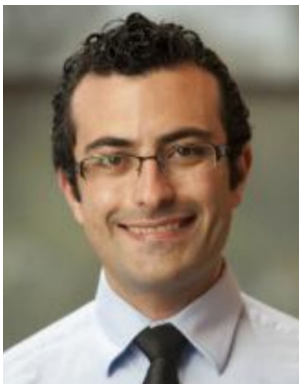

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Hani Saleh (M'12) is an assistant professor of electronic engineering at Khalifa University since 2012. He is an active member in KSRC (Khalifa University Research Center) where he leads a project for the development of wearable blood glucose monitor SOC and a mobile surveillance SOC. Hani has a total of 19 years of industrial experience in ASIC chip design, microprocessor design, DSP core design, graphics core design and embedded system design. His experience spans DSP core design, microprocessor peripherals design, microprocessors and graphics core deign. Prior to joining Khalifa University he worked as a Senior Chip Designer (Technical Lead) at Apple incorporation; where he worked on the design and implementation of Apple next generation graphics cores for its mobile products (iPad, iPhone, …etc.), prior to joining Apple, he worked for several leading semiconductor companies including Intel (ATOM mobile microprocessor design), AMD (Bobcat mobile microprocessor design), Qualcomm (QDSP DSP core design for mobile SOC's), Synopsys (a key member of Synopsys turnkey design group where he taped out many ASICs and designed the I2C DW IP included in Synopys DesignWare library), Fujitsu (SPARC compatible high performance microprocessor design) and Motorola Australia (M210 low power microprocessor synthesizable core design). Hani received a Bachelor of Science degree in Electrical Engineering from the University of Jordan, a Master of Science degree in Electrical Engineering from the University of Texas at San Antonio, and a Ph.D. degree in Computer Engineering from the University of Texas at Austin. Hani research interest includes DSP algorithms design, DSP hardware design, computer architecture, computer arithmetic, SOC design, ASIC chip design, FPGA design and automatic computer recognition. Hani has 3 issued US patents, 13 pending patent application, and over 60 articles published in peer review conferences and Journals in the areas of digital system design, computer architecture, DSP and computer arithmetic.

Baker Mohammad (SM'13) earned his Ph.D. from University of Texas at Austin in 2008, his M.S. degree from Arizona State University, Tempe, and BS degree from the University of New Mexico, Albuquerque, all in ECE. He is an associate professor of electronic engineering at Khalifa University, and a consultant for Qualcomm Incorporated. Prior to joining Khalifa University he was a Senior staff Engineer/Manager at Qualcomm, Austin, USA where he was engaged in designing high performance and low power DSP processor used for communication and multi-media application. Before joining Qualcomm he worked on a wide range of microprocessors design at Intel Corporation from high performance, server chips greater than 100Watt (IA-64), to mobile embedded processor low power sub 1 W (xscale). He has over 16 year's industrial experience in microprocessor design with emphasis on memory, low power circuit and physical design. His research interest includes power efficient computing, high yield embedded memory, emerging technology such as memristor, STTRAM, and computer architecture. In addition, he is engaged in micro-watt range computing platform for WSN focusing on energy harvesting and power management including efficient dc/dc, ac/dc convertors. Baker holds 12 issued US patents and have several pending patent applications. He authored one book titled "Embedded Memory Design for Multi-Core and SOC" and publishes several publications in the area of digital system design, memory design and testing, power management and power conversion, in addition to emerging memory technology (memristor) modeling and design.

Mohammed Ismail (F'97) is a prolific author and entrepreneur in the field of chip design and test, spent over 25 years in academia and industry in the US and Europe. He obtained his BS and MS from Cairo University, Egypt and His Ph.D. from the University of Manitoba, Canada in 1983, all in electrical engineering. He is the Founder of the Ohio State University's (OSU) Analog VLSI Lab, one of the foremost research entities in the field of analog, mixed signal and RF integrated circuits and served as its Director. He also served on the Faculty of OSU's ElectroScience Lab. He held a Research Chair at the Swedish Royal Institute of Technology (KTH) where he founded the RaMSiS (Radio and Mixed Signal Integrated Systems) Research Group there. He had visiting appointments in Finland (Aalto university), Norway (NTH and University of Oslo), the Netherlands (Twente University) and Japan (Tokyo Institute of Technology). He Joined Khalifa University, the UAE in 2011, where he held the ATIC (now Mubadala Technology) Professor Chair and is Founding Chair of the ECE Department. He is the Founding Director of the Khalifa Semiconductor Research Center (KSRC) and Co-Director of the ATIC-SRC Center of Excellence on Energy Efficient Electronic systems (ACE4S) targeting selfpowered chip sets for wireless sensing and monitoring, bio chips and power management solutions. He recently joined Wayne State University, Detroit,

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