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A CMOS temperature sensor based on duty-cycle modulation with calibration

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Abstract
In this paper, a digital CMOS temperature sensor based on duty-cycle modulation with digital calibration is presented. The temperature sensor generates a duty-cycle-modulated signal by applying a proportional to absolute temperature (PTAT) current and a complementary to absolute temperature (CTAT) current derived from substrate bipolar junction transistors (BJT) to an integrator followed by a window comparator. The duty-cycle-modulated signal is then converted to a digital representation of temperature with two counters. Calibration is performed in the digital domain with three calibration parameters. Dynamic element matching (DEM) and chopping techniques are also used to minimize the errors caused by the component mismatch. The prototype chip is fabricated in a 0.5 μm CMOS process. The chip area occupies 2.3 mm^2. Measurement results from 11 test chips show that an inaccuracy of −1.1−0.5 °C is achieved over the temperature range from −35 to 85 °C after calibration. The 2.5 V supply voltage is utilized and the total power consumption is 0.83 mW at a conversion rate of 0.5 kSa/s with a resolution of 0.0625 °C/LSB, leading to 6.48 − nJ°C^2 resolution figure of merit (FoM) and 2951.1 − nJ$\%^2$ accuracy FoM.

Keywords Calibration parameter · Chopping technique · CMOS temperature sensor · Digital temperature representation · Duty-cycle modulation · Dynamic element matching (DEM)

1 Introduction

Temperature sensors are ubiquitous in a very broad range of applications. Examples include consumer electronic products, portable devices, industries, internet of things (IoT) and so on [1]. Traditional temperature sensors are usually discrete devices such as thermistors, platinum resistors, Pt wire, which are bulky and consume high power [2]. Miniaturization, intelligence, and low power consumption have been a trend of almost all kinds of sensors, including temperature sensors likewise. In CMOS technology, the temperature sensing element can be bipolar junction transistors (BJT), MOSFETs, or resistors, etc. [3]. With temperature sensing circuits translating temperature information to voltage, frequency, delay time, etc., an analog-to-digital converter (ADC) or a time-to-digital Converter (TDC) is integrated into the thermal sensors for digital code conversion to compose the so-called smart temperature sensors [4].

Nevertheless, many of the existing temperature sensors output the indirect information of temperature, such as counts [1], voltage [5], frequency [6], delay time [7], etc. They need an extra processor to process the output signals (calculation, transformation and average, communication, etc.). For instance, in reference [3], an accurate BJT-based temperature sensor employs the substrate PNPs as sensing elements. The sensor outputs a duty-cycle-modulated signal. An ARM processor that works at a frequency of

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72 MHz was used to digitize the time intervals of the sensor output and calculate the average duty cycle. While in this work, an integrator substitutes the direct capacitor ($C \sim 150$ pF in the reference [3]) for charging and discharging. It is used to avoid the frequent variation of the voltage at the node of charging. In particular, it expands the range of the integral window, which is suitable for low-voltage design. Besides, the digital circuit for temperature calculating is implemented on the chip. A serial peripheral interface (SPI) is employed to output the binary temperature data to an external SPI master. It is suitable for the applications in which the user requires the temperature data directly.

The proposed temperature sensor incorporates proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) current sources with an integrator, a window comparator, and the digital logic module. The PTAT and the CTAT current are generated with substrate PNPs. The combination of PTAT and CTAT current is a classical method to measure temperature. An innovative duty-cycle modulation scheme is one of the features of this work. The duty-cycle modulation circuits convert temperature related signal from current domain to time domain. This scheme has advantages of low power consumption, flexibility and simplicity in operation. An external clock is utilized to be a timing sequential benchmark for circuits. To calibrate the chip effectively, a method of parameter calibration has been proposed to trim the error of temperature. Three parameters are used to calibrate the measured temperature. Actually, more parameters can be introduced as calibration parameters to achieve more accurate temperature measurement results.

The rest of the paper is organized in four sections. Section 2 introduces the architecture of the proposed temperature sensor, operating principle and circuit implementation detailedly. Section 3 presents the measurement results, and conclusions are drawn in the last section.

2 System design

The proposed temperature sensor chip includes an analog frontend, a controller & counter block, a temperature calculator and two SPI modules. The overall architecture of the proposed temperature sensor is illustrated in Fig. 1. In the analog frontend, the PTAT current and the CTAT current are generated and applied to the integrator which performs multiple integrations to average noise. A triangle signal resulted from the integration is digitized with the window comparator. Dynamic element matching (DEM) and chopper-stabilization are applied in the analog frontend to alleviate mismatch of devices and reduce low-frequency noise, with the control of the controller & counter block.

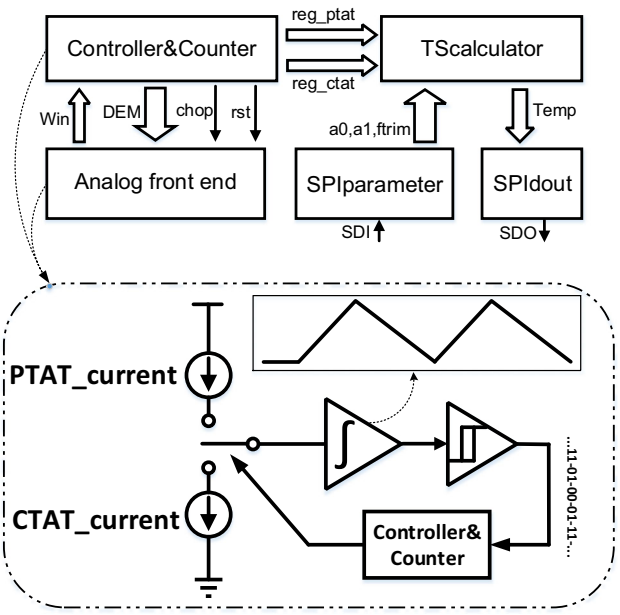

Fig. 1 The block diagram of the temperature sensor

Furthermore, the counter runs counting according to a system clock and digital signals (Win). The first SPI is proposed to achieve the programming on chip with calibration parameters. The parameters can be modified by programming with SPI if it is necessary to calibrate the chip. The calibration parameters and the results of the counter are loaded into temperature calculator to achieve calculating on chip in the next step. In this way, the binary temperature data is obtained. Finally, the second SPI converts the binary temperature data from parallel format to serial format and outputs to the master off chip.

2.1 Temperature sensing principle

For a BJT, there is [8]:

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T} \tag{1}$$

where V_{BE} is the base-emitter junction voltage, $V_T = kT/q$ is the voltage equivalent of temperature, k is the Boltzmann constant, T is the absolute temperature in K, q is the electron charge, respectively. $m \approx -3/2$, $E_g \approx 1.12$ eV is the bandgap energy of silicon. When $V_{BE} \approx 750$ mV, $T = 300$ K, $\partial V_{BE}/\partial T \approx -1.5$ mV/K. It can be observed that V_{BE} shows a complementary to absolute temperature characteristic [8].

By using two identical BJTs biased with a current density ratio of $1 : p$, a voltage difference between the two base-emitter junctions can be obtained, and it can be expressed as

$$\Delta V_{BE} = \frac{kT}{q} ln \frac{I_{C2}}{I_S} - \frac{kT}{q} ln \frac{I_{C1}}{I_S} = \frac{kT}{q} ln(p) \quad (2)$$

It can be observed in formula (2) that ΔV_{BE} is proportional to absolute temperature characteristic [8].

Along the line of consideration, the PTAT and CTAT voltages are applied on the resistors to generate PTAT and CTAT currents. The simplified circuit diagram is illustrated in Fig. 2 [3, 9, 10]. The DEM in this work is not shown in Fig. 2 but has been simplified. It is introduced in Fig. 7 in detail. Transistors M1 to M4 are utilized to bias the circuit. The ratio of W/L is 1:m between M5 and M6, M7 and M8 (m = 4). The ratio of the emitter area is n:1 between Q1 and Q2 (n = 3). The voltage difference of emitters between the bipolar Q1 and Q2 can be obtained on the resistor R1, while the R1 is the so-called PTAT resistor. So the current of R1 is $i_{ptat} = \Delta V_{BE}/R1$, and the $\Delta V_{BE} = V_T ln(mn)$. The current can be copied by the current mirrors composed by M11 to M14. They are current sources. The circuit composed by M9 and M10, Q3 and Q4, generate a CTAT voltage V_{BE}. The bipolar Q3 compensates the base junction current for bipolar Q4, to achieve the compensation of current gain β of Q4 (the current gain β of PNP BJT is approximately 6.5 in this work) [11]. The base-emitter junction voltage V_{BE} of Q4 is buffered by the amplifier amp2, and then applied on resistor R2, to generate a CTAT current $i_{ctat} = V_{BE}/R2$. This is a current sink. The resistor R2 is a so-called CTAT resistor. Usually, the current which is independent of temperature can be obtained as $i_{ref} = i_{ptat} + i_{ctat}$ by means of optimizing the resistor values of R1 and R2 [12]. However, compared to the i_{ref}, the PTAT or CTAT current just varies by about 30% over the desired temperature range: −45 °C to 130 °C. A larger range of change over the temperature is preferred to obtain a high dynamic range. For this reason, a combination has been presented as

$$I_{ptat} = 3i_{ptat} - 0.5i_{ctat} \quad (3)$$

$$I_{ctat} = i_{ctat} - i_{ptat} \quad (4)$$

$$I_{ref} = 2i_{ptat} + 0.5i_{ctat} \quad (5)$$

With this current combination [9], the PTAT or CTAT current varies about from 20 to 90% over the temperature range mentioned above. So the current variation can be detected more effective. Figure 3 shows the simulation results, I_{ref} is about 5.5 μA, I_{ptat} varies from about 1 μA to 5 μA over the temperature range mentioned above. This current combination can be obtained by controlling the switches S1 and S2 in the appropriate sequence in Fig. 2.

2.2 Duty-cycle modulation

PTAT and CTAT currents are direct-current (DC) signals, which can be transformed into ramps after integrator. The slope of ramp is dependent on the value of current. In view of this, Fig. 4 shows the structure of integrator. The PTAT current is integrated firstly, resulting in a decreasing ramp at the output of the integrator. Similarly, a rising ramp can be obtained by switching to CTAT current. In reference [3], the PTAT and CTAT currents charge and discharge the 150pF capacitor directly. So the drain voltage of current

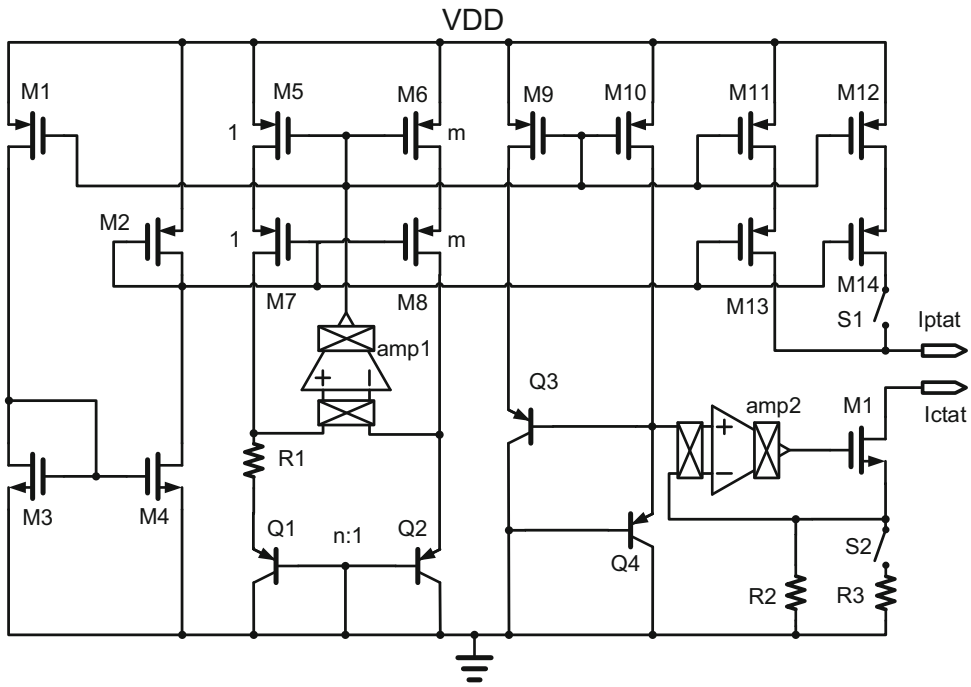

Fig. 2 Simplified circuit diagram of PTAT and CTAT currents generator

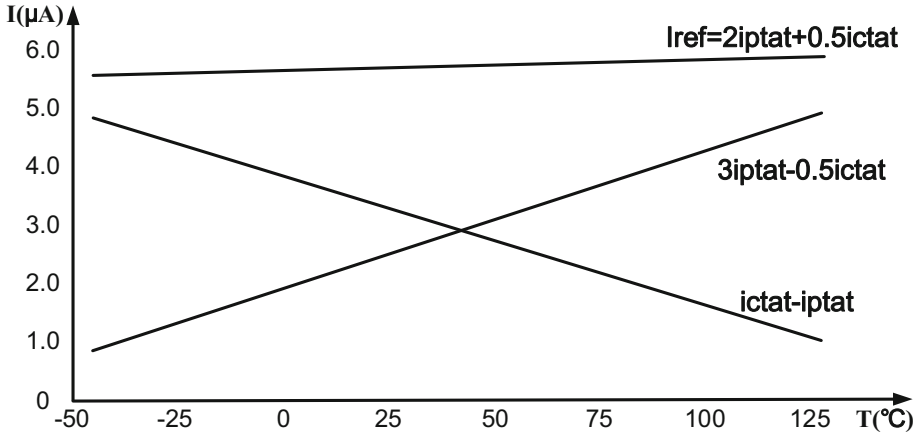

Fig. 3 Simulation results of the new combination of PTAT and CTAT currents from formula (3), (4) and (5)

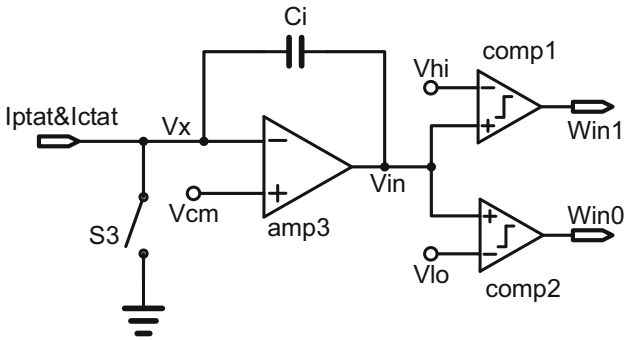

Fig. 4 The diagram of integrator and window comparator

mirrors changes from the input threshold V_{TH_N} to V_{TH_P} of Schmitt trigger, which introduces the channel length modulation effect. The integrator in Fig. 4 stabilizes the drain voltage of current mirrors in the conversion. Without stabilization, the current varies about:

$$\Delta i_{ptat} \approx \pm\frac{1}{8}\mu_p C_{ox}\frac{W}{L}V_{OV}^2\lambda(V_{TH\_P} - V_{TH\_N}) \tag{6}$$

Where λ is channel length modulation coefficient, V_{OV} is the overdrive voltage of PMOS M11 to M14. Last but not least, V_{TH_N} is not allowed to be smaller than V_{BE} considering the i_{ctat} generation. It is crucial for low-voltage design (In reference [3], the supply voltage is 2.7−5.5 V, this work's is 2.5 V). The integrator is a valid method to expand the range of comparing. With stabilization, the current is fixed, and the input swing of window comparator is more flexible. A window comparator is connected after integrator. The comparator is designed with the cross-coupling structure. So it has a fast response. Notwithstanding the delay of the comparator, it's influence can be regarded as negligible when comp1 and comp2 have an approximate equal delay. The basic logic of duty-cycle modulation is shown in Table 1, where $V_{hi} = 2.25$ V, $V_{lo} = 0.25$ V, $V_{cm} = 1.25$ V in this design, to structure a big enough rang for integration $[(2.25 - 0.25)/2.5 = 80\%]$, they are produced

Table 1 The basic logic of duty-cycle modulation

Condition	Results	State
$V_{in} < V_{lo}$	win1 = 0, win0 = 0	Judgement
$V_{lo} < V_{in} < V_{hi}$	win1 = 0, win0 = 1	Integration (count)
$V_{in} > V_{hi}$	win1 = 1, win0 = 1	Judgement

by resistor voltage dividers, win1 and win0 are the outputs of comparators. So the information of PTAT and CTAT currents can be transformed into digital signal by the integrator and window comparator. Actually, the input offset voltage of amplifier amp3 (Fig. 4) has no influence on the system considering that the input offset voltage of amp3 do not change the relative interval of comparing. And the accuracies of V_{hi}, V_{lo} and V_{cm} have no influence to the system as the same reason as offset of amp3. The inaccuracies of those reference voltages do not change the duty in formula (9). However, integrator consumes an additional power consumption about 130 μW.

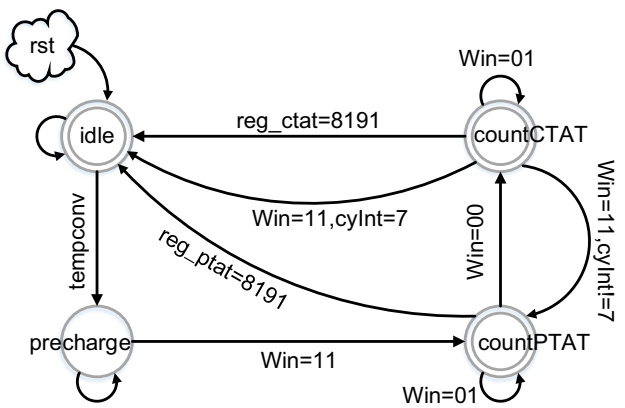

Fig. 5 The state machine of controller and counter

The state machine of controller and counter is shown in Fig. 5. It has four states: idle, precharge, countPTAT, countCTAT. The counter counts the number according to the system clock and the Win logic. It counts the clock numbers of PTAT and CTAT integral time. A large range of clock frequency is permitted from dozens of kHz to several MHz. The relationships of integral time, currents and counts are

$$t_{int} = \frac{2 \times C_i \times (V_{hi} - V_{lo})}{(I_{ptat} + I_{ctat})} \tag{7}$$

$$reg\_ptat + reg\_ctat = N \times f_{clk} \times t_{int} \tag{8}$$

where t_{int} is the integral time of one cycle, reg_ptat and reg_ctat are the count values, N is the number of cycles, f_{clk} is the frequency of system clock. Ci is the integral capacitance (Ci $\sim$ 68 pF in this paper). The counter overflows inevitably when the system clock frequency is too high. A recommended range of system clock is 500 kHz−8 MHz. It can also be designed with CMOS ring oscillator on chip. The variation in clock duty cycle has little impact on the counts. Because the counts are the statistic of clock numbers rather than the clock duty cycle. However, the counts of a single cycle of integration may have a terrible inaccuracy due to the error of counting. For this reason, multiple integrations are proposed to average the error of counting in each integration period. The compromise between time consumption and counting error has been considered. Eight cycles of integrating have been proved to be a good choice [3]. The sequence diagram of duty-cycle modulation is shown in Fig. 6. At the time t1, the state machine is reset at the falling edge of the rst signal. And then at the time t2, the conversion is initialized at the rising edge of the tempconv signal. The chopper signal is provided by the controller in each period of integration to weaken the offset of amplifiers simultaneously. Furthermore, the Win signal changes from 11 → 01 → 00 → 01 → 11 in a complete integration cycle. So it repeats eight times in eight integration cycles. In this way, analog signal PTAT and CTAT currents can be transformed into counts, achieving the so-called duty-cycle modulation.

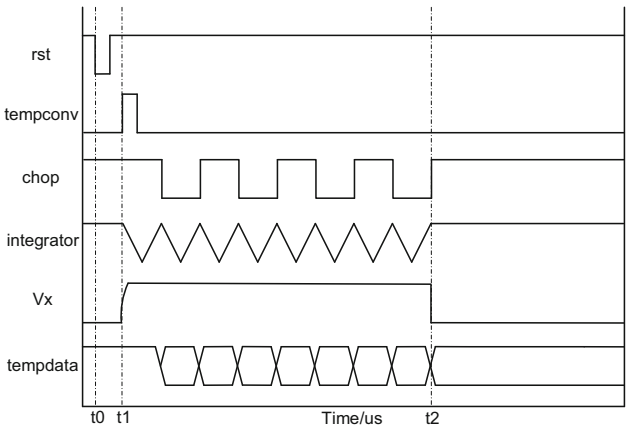

Fig. 6 The main sequence diagram of the duty-cycle modulation (eight cycles)

2.3 DEM and chopping

In the semiconductor process, the size scale of the device has trended from μm to nm. It is hard to avoid dimension error in such an accurate fabrication. The mismatches of MOS transistors and BJTs in the PTAT and CTAT currents generator result in errors of PTAT and CTAT currents, and then lead to deviations of integration time, whereupon lead to counting errors, result in inaccurate temperature data at last. DEM is a commendable method to solve this problem. In DEM technique, many sub-modules switch the roles in circuits alternately, to average the deviation of sub-modules. The circuit diagram of the PTAT current module with DEM is shown in Fig. 7. There are eight current mirrors on the top, and four PNP transistors at below, two rows DEM switches in the center which control the currents flow of current mirrors and BJTs at the special sequence. There are $8 \times 3 \times 4 \times 2 = 192$ different combinations (eight current mirrors for 1:4 currents, remaining three current mirrors for $1 + 2$ or $1 + 2$ dummy currents, four BJTs for 1:3 currents, and two CTAT resistors). As stated previously, 192 integration cycles consume a long time. Actually, simultaneously rotating all the component groups during the DEM process, instead of rotating them one after one, reduces the number of DEM periods significantly, making the measurement speed much faster [3].

What is more, the amplifier amp1 and amp2 (as shown in Fig. 2) have an input offset about a scale of mV when the chopping technique is not utilized. The chopping technique is proposed to minimize the offset voltage. The circuit diagram of the chopper amplifier is shown in Fig. 8. The amplifier's first stage is a folded cascode amplifier, which has characteristics of high output impedance and high voltage gain. The second stage is a common source amplifier that current mirror as a load, which provides high current drivability and fast response. The miller compensation has been utilized between two stages, to guarantee the stability of amplifier [13]. The input signal pairs flow through different branches in turn with the control of choppers. So the average offset is close to zero. There are four times chopping due to the eight integration cycles, as shown in Fig. 6.

2.4 Parameter calibration

As mentioned, the PTAT and CTAT currents are operated by integration, leading to the counts reg_ptat and reg_ctat

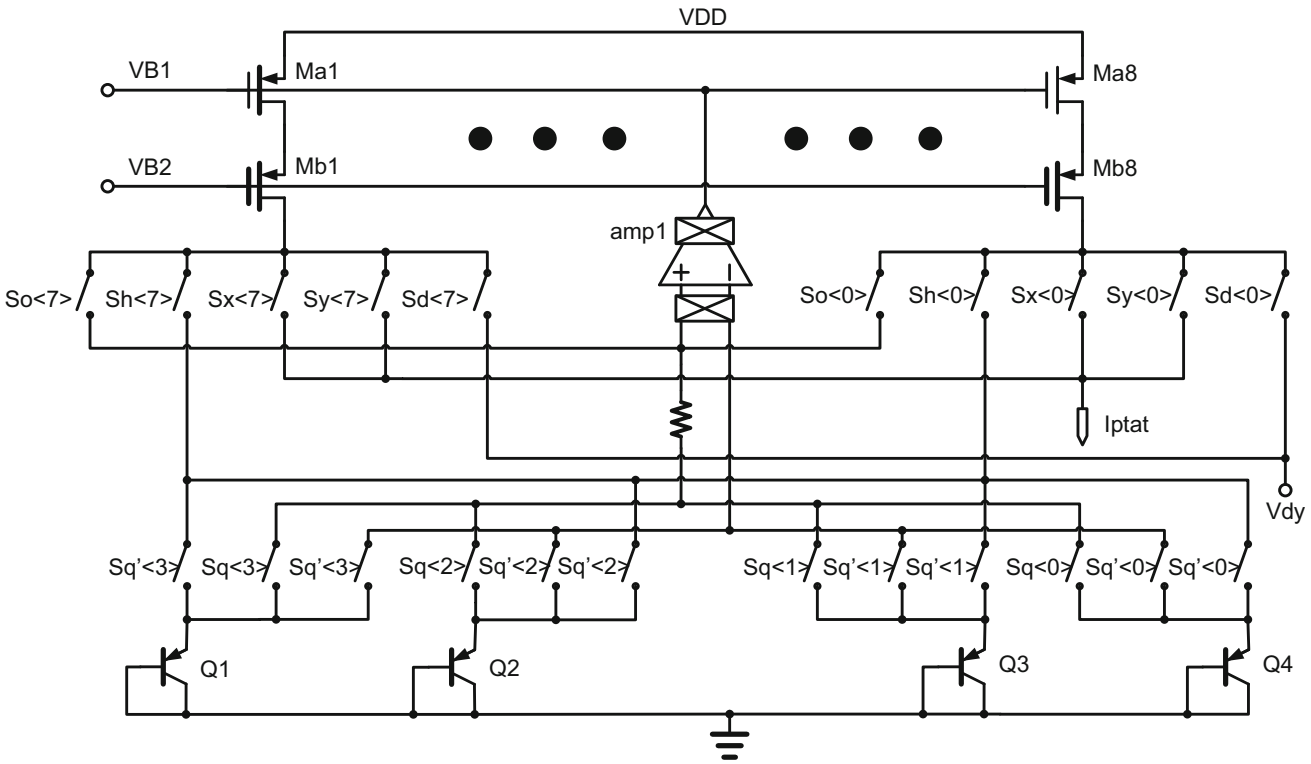

Fig. 7 The circuit diagram of PTAT current module with DEM

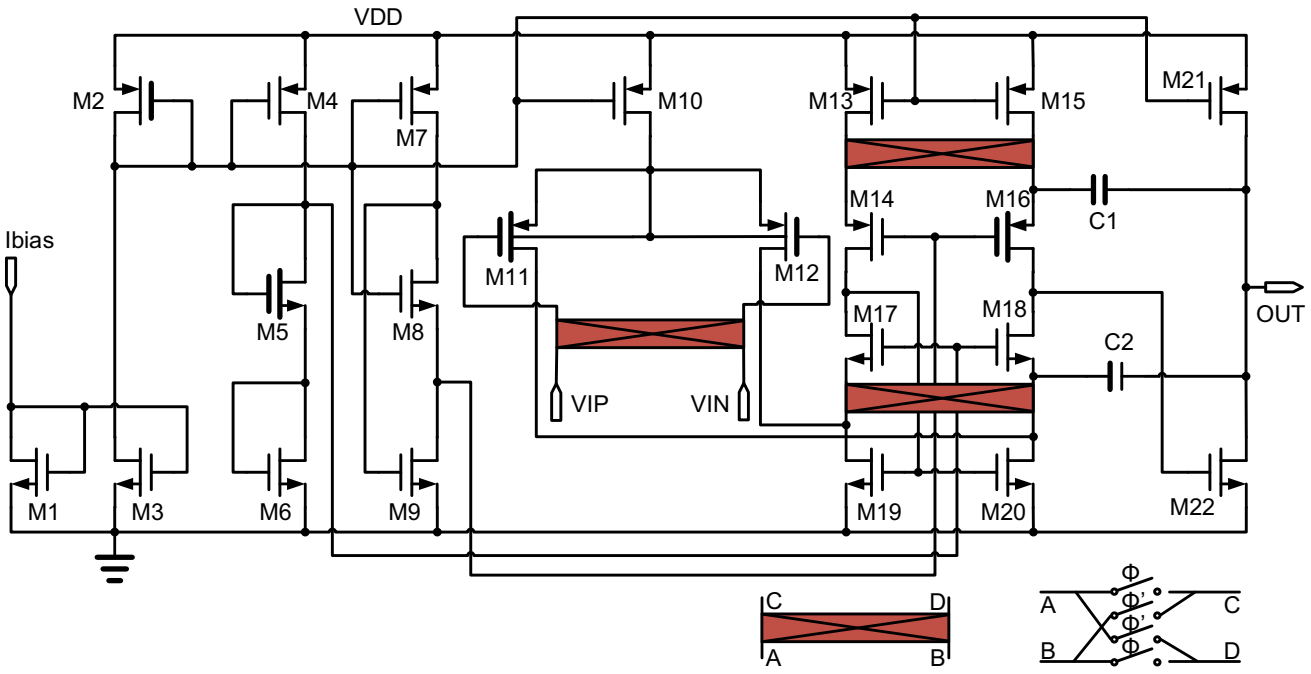

Fig. 8 The circuit diagram of chopper amplifier

which are proportional to the currents. The duty is defined as a time ratio of CTAT current integration to a single integration cycle, as

$$duty = \frac{I_{ctat}}{I_{ptat} + I_{ctat}} = \frac{reg\_ctat}{reg\_ptat + reg\_ctat} \tag{9}$$

Actually, I_{ref} is not a horizontal line but has a little slope as shown in Fig. 3. It means that I_{ref} is not a constant when the temperature changed. So it needs a trim to formula (9), the new formula as

$$duty = \frac{I_{ctat}}{I_{ptat} \times ftrim + I_{ctat}} = a0 + a1 \times T = \frac{reg\_ctat}{reg\_ptat \times ftrim + reg\_ctat} \tag{10}$$

where $a0$ and $a1$ are coefficients, T is the temperature in centigrade, reg_ptat and reg_ctat are obtained by circuit simulation. The sub-graphs (a–c) in Fig. 9 show the impacts to the temperature error from parameters $a0$, $a1$ and *ftrim*. It is clear that the $a0$ changes the horizontal position of error curve, the $a1$ influences the inclination (slope) of error curve, and the *ftrim* impacts the concavity and convexity of temperature error curve. The sub-graph (d) in Fig. 9 shows the curve of simulated temperature error versus temperature. In the simulation result, an inaccuracy of $\pm 0.1\,^{\circ}\mathrm{C}$ is achieved over the temperature range from -45 to $115\,^{\circ}\mathrm{C}$. It provides a basis for the parameter calibration.

It is worth mentioning the fluctuation of the calibrated curve in Fig. 9(d). Define it by ε_t. It has two sources: high-order nonlinear components in current combines, and counting error. To verify the nonlinearity of currents, the values of currents are picked out from the simulation circuit and substituted into formula (10). The curve of temperature error is obtained in Fig. 9(e) after trimming. In this way, the counting error is ruled out. As shown in Fig. 9(e), the residual error ε_p can be perfect to fit a 5-order polynomial:

$$\varepsilon_p(T) = \alpha_1 T^5 + \alpha_2 T^4 + \alpha_3 T^3 + \alpha_4 T^2 + \alpha_5 T + \alpha_6 \tag{11}$$

where T is the temperature in centigrade, $\alpha_1 = 2.9519 \times 10^{-12}$, $\alpha_2 = 2.5363 \times 10^{-9}$, $\alpha_3 = 5.1087 \times 10^{-7}$, $\alpha_4 = 6.1205 \times 10^{-4}$, $\alpha_5 = 0.1046$, $\alpha_6 = -11.0762$. On the other hand, to study the counting error, combining the formula (7), (8) and (10), and Subtracting the nonlinear error mentioned above, the rounding error from counting can be acquired. The scatters of counting error are shown in Fig. 9(f). Define the counting error by ε_c. Therefore, the curve in Fig. 9(d) has a "random" shape: $\varepsilon_t = \varepsilon_p + \varepsilon_c$. The 5-order polynomial fitting in Fig. 9(d) is coincident with this explanation.

Originally, a group of optimized parameters ($a0$, $a1$, *ftrim*) is selected as an initial value at the stage of circuit design. This set of parameters can be programmed into the chip by SPIparameter module. The temperature is calculated in TScalculator module (Fig. 1) as:

$$T = \left[\frac{reg\_ctat}{reg\_ptat \times ftrim + reg\_ctat} - a0\right] \Big/ a1 \tag{12}$$

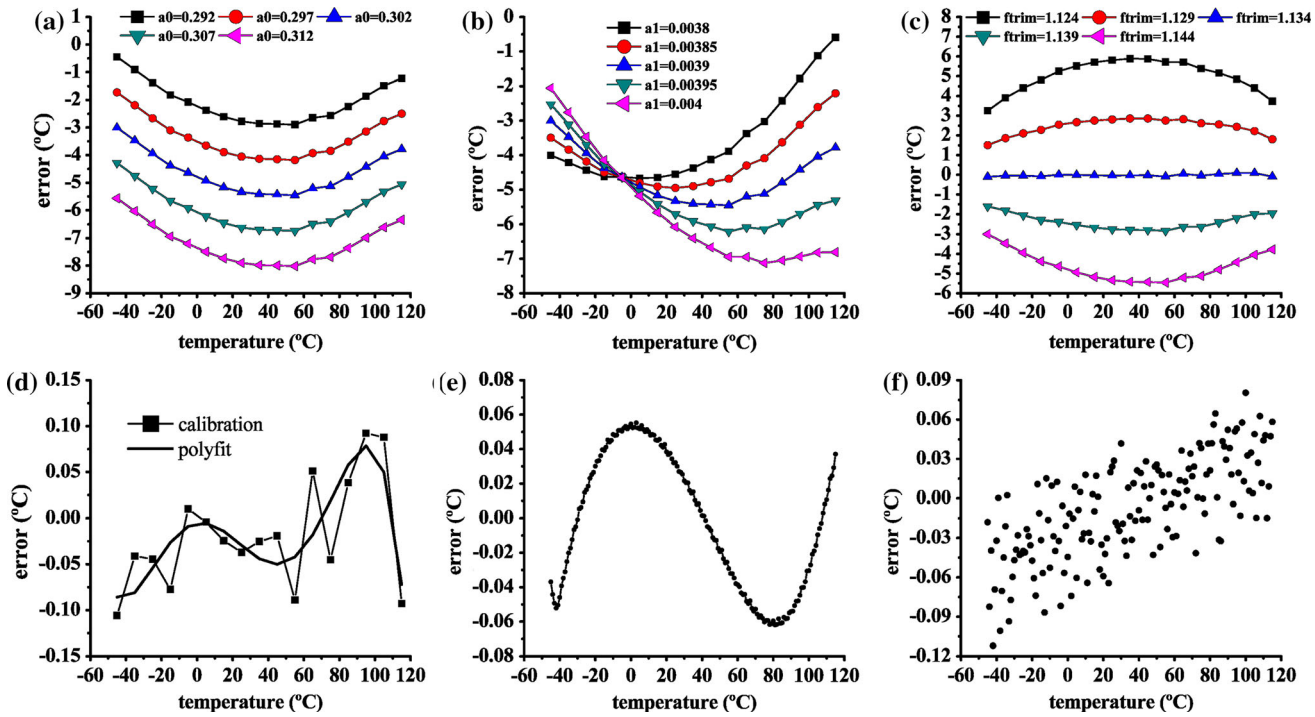

Fig. 9 The simulated curves of temperature error versus temperature with different parameters $a0$, $a1$ and *ftrim* in formula (10) refer to sub-graph **a**–**c**, respectively. **d** Are simulated temperature error versus temperature and its 5-order polynomial fitting. **e** Shows the high-order nonlinear components in the temperature error which come from the nonlinearity of currents. **f** Shows the scatters of counting error during the temperature range

In the calculation, the temperature data are represented in the form of binary complement, and the 12-bit binary serial data output through SPIdout module (Fig. 1). Table 2a illustrates the significance of each bit of 12-bit digital output data. It can be observed that the most significant bit (MSB) contains the sign bit, denoting whether the temperature is positive or negative. The low 4 bits are the decimal of temperature. For instance, Table 2b lists some typical temperature relationship of digital output to the measured temperature. To test and verify the functions of the sensor effectively and sufficiently, the *reg_ptat* and *reg_ctat* are outputted with the temperature data successively at the serial port of SPIdout module.

3 Measurement results

A micrograph of the proposed CMOS temperature sensor with a circuit area of 2.3 mm^2 in a 0.5 µm CMOS process is shown in Fig. 10. It occupies a larger area than reference [3] due to the temperature digitization and calibration on chip. With a single supply voltage of 2.5 V, the power dissipation is 0.83 mW at a conversion rate of 0.5 kSa/s with a resolution of 0.0625 °C/LSB. It is about 80% consumed by analog circuit and 20% for digital circuit. The chips are packaged in DIP 24-pin with 11 pieces. The dies come from the random position of one wafer.

To understand the performance of the proposed sensor, the measurements are performed in an interval of 10 °C with a −35−85 °C temperature range by using an advanced temperature source (Thermotron s-1.5-3200) that is calibrated by a thermocouple. It is worth mentioning that the equipment declares it only has a ±0.5 °C resolution. So maybe it is not a perfect environment for measurement.

Table 2 Temperature/data relationships

MSB	11	10	9	8	7	6	5	4	3	2	LSB
(a) 12-bit digital output data											
Sign	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
Temperature (°C)	Digital output (binary)						Digital output (hex)				
(b) The exact relationship of digital output to measured temperature											
+85	0101 0101 0000						550h				
+25.0625	0001 1001 0001						191h				
+0.5	0000 0000 1000						008h				
0	0000 0000 0000						000h				
−0.5	1111 1111 1000						FF8h				
−25.0625	1110 0110 1111						E6Fh				

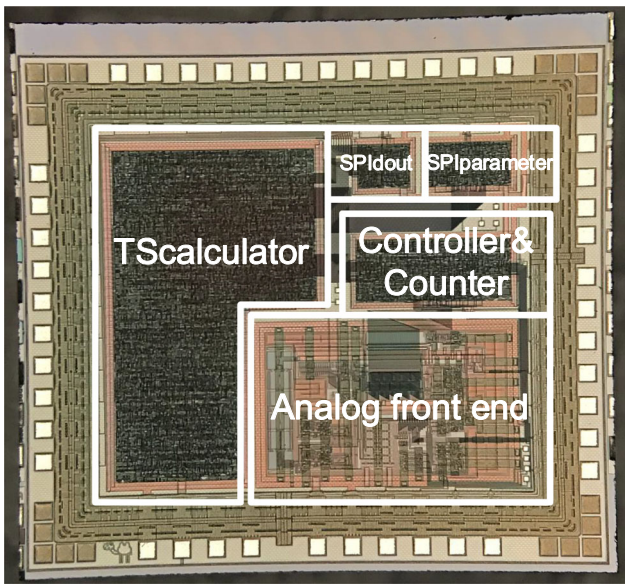

Fig. 10 The micrograph of the test chip

The step of start to convert at a rate of 300 samples per second is issued by the FPGA DE0-Nano Board from Terasic, which provides a 4 MHz clock, and gives commands and instructions to the sensor as a master. The digital output codes are sampled by using the FPGA and software Quartus II (Quartus Prime 17.0) Lite Edition from Altera. At the condition of initial parameter: $ftrim = 1.134$, $a1 = 0.0039$, $a0 = 0.302$, without trimming the sensors exhibit about −8−10 °C error at the temperature range of −35−85 °C as shown in Fig. 11(a). These curves have the same trend. So the first scheme, loading the *reg_ptat* and *reg_ctat* data to the MATLAB program to find an optimized $a1$ and *ftrim*. When the optimized parameters *ftrim* and $a1$ are fixed for all the sensors, the $a0$ is variable for each chip to trim the error curve by shifting up and down. With this method, the inaccuracy of the 11 chips is about −2.5−1.5 °C from −35 to 85 °C as shown in Fig. 11(b). And the second scheme, when the optimized parameter *ftrim* is fixed for all the sensors, $a1$ and $a0$ are variable for each chip. The choices of $a1$ and $a0$ obey (calibration at 25 °C):

$$a1(trim) = a1(init) \times \left[1 + \frac{\Delta T(85\,^{\circ}\mathrm{C}) - \Delta T(-35\,^{\circ}\mathrm{C})}{120\,^{\circ}\mathrm{C}}\right]$$

$$a0(trim) = a0(init) + T(25\,^{\circ}\mathrm{C}) \times a1(init) - 25 \times a1(trim)$$

where the $a1(trim)$ and $a0(trim)$ are the calibration parameters that need to be programmed in each chip, $a1(init)$ and $a0(init)$ are the initial parameter which is assigned at the state of circuits design. $T(25\,^{\circ}\mathrm{C})$ is the measured value at 25 °C, $\Delta T(85\,^{\circ}\mathrm{C})$ is the temperature difference between the measured value and true value when the true value is 85 °C, the others Similarly. So it

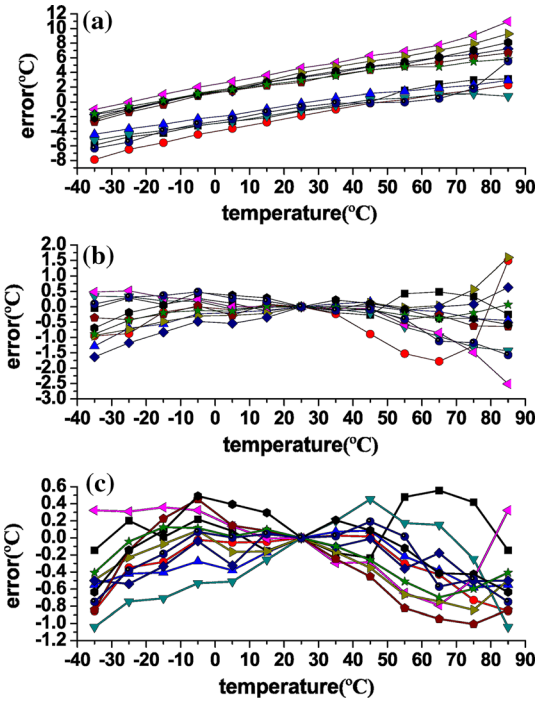

Fig. 11 The measurement results of temperature error of 11 test chips at the temperature range of −35−85 °C. **a** Shows the inaccuracy (−8−10 °C) with the initial parameter: *ftrim* = 1.134, $a1 = 0.0039$, $a0 = 0.302$. **b** Shows the inaccuracy (−2.5−1.5 °C) with fixed *ftrim* and $a1$, variable $a0$ after calibration at 25 °C. **c** Shows the inaccuracy (−1.1−0.5 °C) with fixed *ftrim* and variable $a1$, $a0$ after calibration at 25 °C

needs to measure three temperature data to calibrate each chip. They are $T(-35\,^{\circ}\mathrm{C})$, $T(25\,^{\circ}\mathrm{C})$ and $T(85\,^{\circ}\mathrm{C})$, respectively. With this method, the systematic error versus temperature for 11 samples after parameter calibration is shown in Fig. 11(c). It can be observed that an inaccuracy of −1.1−0.5 °C is obtained from −35 to 85 °C. Actually, the curves have big nonlinearity at the high temperature over 85 °C which may be caused by big leakage current. It is possible that the resistors in this process have a big temperature nonlinearity at high temperature. Nonetheless, it is still an issue needs more supporting evidence.

Finally, to understand the nonlinear error of curves, the polynomial fitting has been used at the post-processing stage. From the formula (10), it is clear that the temperature fitting of the test chip is first order. The inaccuracy is not small enough owing to the nonlinear error. The polynomial fitting is used to eliminate some nonlinear error. Essentially, each sensor has a set of separate parameters. Figure 12 shows the inaccuracy of (a) second-order, $duty = a0 + a1 \times T + a2 \times T^2$; (b) third-order, $duty = a0 + a1 \times T + a2 \times T^2 + a3 \times T^3$; (c) fourth-order, $duty = a0 + a1 \times T + a2 \times T^2 + a3 \times T^3 + a4 \times T^4$; (d) fifth-order, $duty = a0 + a1 \times T + a2 \times T^2 + a3 \times T^3 + a4 \times T^4 + a5 \times T^5$ polynomial fitting at the temperature range of −35−85 °C. The inaccuracy is about (a) −0.65−0.45 °C, (b) −0.4−0.38 °C, (c) −0.38−0.27 °C, (d) −0.27−0.22 °C, respectively. The higher order polynomial contains more coefficients, which increases the complexity of parameter

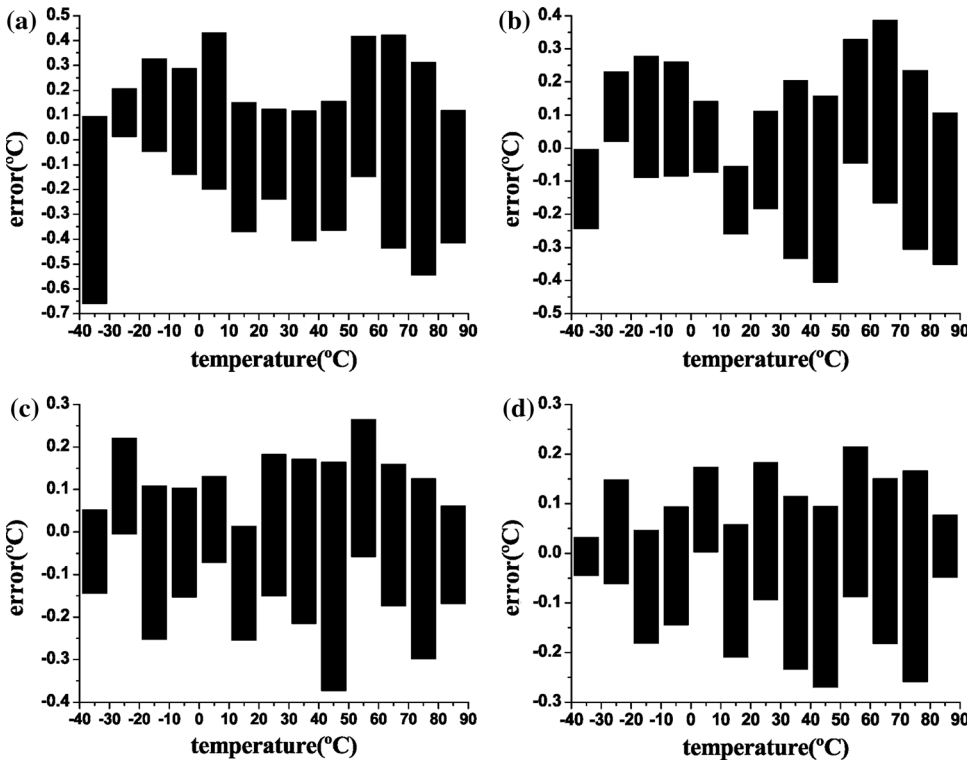

Fig. 12 The inaccuracy of 11 test chips that uses the polynomial fitting. **a** Second-order, **b** third-order, **c** fourth-order, **d** fifth-order

Table 3 Performances comparison among recent smart temperature sensors

Parameter	Resolution (°C)	Error (°C)	Energy/conversion (μJ/Sa)	Sampling rate (Hz)	Area (mm^2)	Temperature range (°C)	CMOS technology (μm)	Resolution FoM† ($nJ°C^2$)	Accuracy FoM* ($nJ\%^2$)
[2], 2016	0.01	±0.2	0.55	2	0.198	25−45	0.18	0.055	2200
[3], 2017	0.003	±0.3	0.356	550	2.21	−45−130	0.7	0.0032	41.8
[14], 2016	0.001	±0.1	1.6	10	0.25	20−50	0.18	0.0016	711.1
[15], 2017	N/A	±0.8	0.06	390	0.0578	−55−175	0.04	N/A	2904
[16], 2017	0.21	±1.93	0.00054	4.8	0.15	−20−40	0.065	0.024	22
[17], 2017	0.18	±1	0.0665	1000	0.19	−40−85	0.18	2.155	170
[18], 2018	0.016	±0.47	1.6	195	0.29	−40−125	0.13	0.41	520
[19], 2018	0.039	±0.85	0.007	123	0.1	−30−120	0.18	0.011	8.95
This work	0.0625	−1.1−0.5	1.66	500	2.3	−35−85	0.5	6.48	2951.1

† Resolution FoM = Energy/conversion × (resolution)^2 [20].

∗ Accuracy FoM = Energy/conversion × (relative error)^2. Relative error (%) = Maximum sensing error/temp. range [20]

calibration. It is established that an N-order polynomial needs N + 1 measurements to solve the N + 1 parameters.

4 Conclusions

In summary, a CMOS temperature sensor based on duty-cycle modulation with parameter calibration is presented. The 12-bit binary temperature data can be obtained directly. The calibration parameters can be programmed into the chip to trim the temperature accuracy. An inaccuracy of −1.1−0.5 °C is obtained from −35 to 85 °C after the calibration at 25 °C. The comparison is made with different state-of-the-art MOSFET/BJT based low power temperature sensors in Table 3. The proposed temperature sensor achieves a high sampling rate at moderate resolution, featuring digital output and on-chip digital calibration. Finally, the polynomial fitting method is discussed to verify the curvature correction on the basis of experimental data. With the increment of the order, more nonlinear errors are expected to be corrected.

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References

1. Hung, C. C., & Chu, H. C. (2016). A current-mode dual-slope CMOS temperature sensor. *IEEE Sensors Journal*, *16*(7), 1898–1907.
2. Law, M. K., Lu, S., Wu, T., Bermak, A., Mak, P. I., & Martins, R. P. (2016). A 1.1 μW CMOS smart temperature sensor with an inaccuracy of ±0.2 ° C (3σ) for clinical temperature monitoring. *IEEE Sensors Journal*, *16*(8), 2272–2281.
3. Wang, G., Heidari, A., Makinwa, K. A. A., & Meijer, G. C. M. (2017). An accurate bjt-based CMOS temperature sensor with duty-cycle-modulated output. *IEEE Transactions on Industrial Electronics*, *64*(2), 1572–1580.
4. Chen, C. C., & Chen, H. W. (2014). A low-cost CMOS smart temperature sensor using a thermal-sensing and pulse-shrinking delay line. *IEEE Sensors Journal*, *14*(1), 278–284.
5. Fisk, R. P., & Hasan, S. M. R. (2011). A calibration-free low-cost process compensated temperature sensor in 130 nm CMOS. *IEEE Sensors Journal*, *11*(12), 3316–3329.
6. Jalalifar, M., & Byun, G. S. (2016). A wide range CMOS temperature sensor with process variation compensation for on-chip monitoring. *IEEE Sensors Journal*, *16*(14), 5536–5542.
7. Chen, P., Chen, T. K., Wang, Y. S., & Chen, C. C. (2009). A time-domain sub-microwatt temperature sensor with digital set-point programming. *IEEE Sensors Journal*, *9*(12), 1639–1646.
8. Razavi, B. (2013). *Design of analog CMOS and integrated circuits*, 1st edn. McGraw-Hill Education (Asia) Co. and Xian Jiaotong University Press.
9. Abdollahpour, M., & Heidari, A. (2015). A 1-volt temperature sensor with duty-cycle-modulated output in 0.18μm CMOS technology. In *2015 23rd Iranian conference on electrical engineering* (pp. 1089–1092).
10. Heidary, A., Wang, G., Makinwa, K., & Meijer, G. (2014). A bjt-based CMOS temperature sensor with a 3.6pj-K^2-resolution FoM. In *2014 IEEE international solid-state circuits conference digest of technical papers (ISSCC)* (pp. 224–225).

11. Song, B. S., & Gray, P. R. (1983). A precision curvature-compensated CMOS bandgap reference. *IEEE Journal of Solid-State Circuits*, *18*(6), 634–643.
12. Meijer, G. C. M., van Gelder, R., Nooder, V., Drecht, J. V., & Kerkvliet, H. (1986). A three-terminal wide-range temperature transducer with microcomputer interfacing. In *Solid-state circuits conference, 1986. ESSCIRC '86. Twelfth European* (pp. 161–163).
13. Sansen, W. M. C. (2008). *Analog design essentials* (1st ed.). New York/Beijing: Springer/Tsinghua University Press.
14. Deng, C., Sheng, Y., Wang, S., Hu, W., Diao, S., & Qian, D. (2016). A CMOS smart temperature sensor with single-point calibration method for clinical use. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *63*(2), 136–140.
15. Di, Z., & Liter, S. (2017). A 0.058 mm^2 24 *mu*W temperature sensor in 40 nm CMOS process with $\pm 0.5\,^{\circ}$ C inaccuracy from -55 to 175 $^{\circ}$ C . *Circuits Systems and Signal Processing*, *37*(6), 2278–2298.
16. Wang, H., & Mercier, P. P. (2017). A 113 pW fully integrated CMOS temperature sensor operating at 0.5 v. In 2017 IEEE SENSORS (pp. 1–3).
17. Tran, T., Peng, H., Chao, P. C., & Hsieh, J. (2017). A low-ppm digitally controlled crystal oscillator compensated by a new 0.19-mm^2 time domain temperature sensor. *IEEE Sensors Journal*, *17*(1), 51–62.
18. Tang, Z., Fang, Y., Yu, X., Shi, Z., & Tan, N. (2018). A CMOS temperature sensor with versatile readout scheme and high accuracy for multi-sensor systems. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *65*(11), 3821–3829.
19. Wang, B., Law, M., Tsui, C., & Bermak, A. (2018). A 10.6 pjk^2 resolution FoM temperature sensor using astable multivibrator. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *65*(7), 869–873.
20. An, Y. J., Ryu, K., Jung, D. H., Woo, S. H., & Jung, S. O. (2014). An energy-efficient time-domain temperature sensor for low-power on-chip thermal management. *IEEE Sensors Journal*, *14*(1), 104–110.

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