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An energy-efficient and ultra-low-voltage power oscillator in CMOS 65 nm

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Abstract
In a direct modulation scheme and particularly in portable and wireless sensor network applications, the oscillator limits the transmitter efficiency therefore, the oscillator efficiency is critical and high-efficiency and high-power oscillators are increasingly required. This paper presents a high-efficiency and ultra-low-voltage power oscillator that operates at 2.4 GHz and is implemented in 65 nm CMOS technology. The power oscillator is a self-oscillating class-E power amplifier (PA) that utilizes a positive feedback system. A class-E PA is selected due to its high efficiency. The power oscillator has an optimized power consumption and output power, where a 2.4 mW power consumption is achieved under a 0.4 V power supply. The proposed oscillator demonstrates a maximum output power of -0.45 dBm and a peak efficiency of 37.5%. The oscillator is tunable between 1.66 and 2.78 GHz. The oscillator is robust to a $\pm 15\%$ frequency deviation from a 2.44 GHz nominal frequency due to process, voltage, temperature variation.

Keywords Power VCO · CMOS · 65 nm · Power oscillator · Energy-efficient · Class-E PA · Class-E VCO · Class-E oscillator · Power amplifier · High-efficiency

1 Introduction

The voltage controlled oscillator (VCO) is a very important building block in communication systems. It is used in different applications either as a carrier generator or as a clock for digital circuits. The VCO characteristics limit the transmitter performance in a direct modulation scheme. This is even more clear in limited power budget applications. Therefore, energy-efficient oscillators are required. Furthermore, the output power is critical in directly modulated VCOs to maintain a reasonable transmission range and to achieve a low bit error rate.

Power consumption, tuning range, output power and efficiency are key parameters for power oscillator design. The power consumption must be minimized to maximize the efficiency without degrading the output power of the PA. Note, PAs with an output power of the order of 1 Watt, have high efficiency around 65% [1, 2]. However, for PAs with milli-watt output power levels, low efficiency around 10% are usually reported [3–5]. Implementing PAs in CMOS technology limit the power supply due to the low breakdown voltage in CMOS and the high drain swing in class-E PA. This leads to a low output power and a poor efficiency compared to other technologies. In [6, 7] a class-E PA is implemented in GaAs technology, the higher break-down voltage in GaAs helped to use a high power supply and this results in a higher output power and improved efficiency. Also, a wide frequency tuning range is important to compensate for PVT variation. The frequency tuning is limited by the loop gain of the circuit. Generally, a capacitor divider is usually employed at the feedback network to achieve a $\pm 360^{\circ}$ phase shift to implement a positive feedback. This capacitor network degrades the gain which is necessary to maintain the oscillation.

Although several designs were reported in the literature for a high-efficiency power oscillator in CMOS technology [8–10], a limited tuning range and high power consumption were associated with these designs. In [8], a relatively good efficiency is achieved, however it consumes a high power.

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While in [11, 12], a very limited tuning range is achieved to maintain a high output power since the frequency tuning is limited by the loop gain of the circuit.

An alternative design approach for a high-efficiency power oscillator and a relatively high output power is presented here along with system and circuit level design methodology. This approach maintains a low-power consumption and achieves a wide tuning range thanks to a pre-amplifier stage that used to replace the capacitor divider in the feedback network. This oscillator can be employed in a direct modulation transmitter design for a WSN and RF-powered applications.

This paper is organized as: In Sect. 2, system level considerations and design methodology of the power oscillator are described. In Sect. 3, circuit design techniques to achieve high efficiency are presented. Section 4 presents the complete circuit design of class-E VCO. Section 5 demonstrates the simulation results and finally in Sect. 6, the conclusions are formalized.

2 Design methodology

Switching PAs classes (E and F) are preferred in many applications due to their high efficiency. A class-E PA is selected here to design a power oscillator. A class-E PA was first introduced by Sokals in 1972. It is a nonlinear amplifier where the transistor acts as a switch with ideal efficiency equal 100%. Figure 1 depicts the circuit of a class-E PA. It includes a single NMOS transistor acts as a switch Q_1, a series resonant filter is designed to pass the fundamental sinusoidal to the load where it composes of L_{res} and C_{res}. The RF choke inductor L_{choke} connects the DC power supply with the transistor Q_1 to allow a DC current to flow. C_p is the parasitic capacitor of Q_1 and the antenna is modeled with a $50\,\Omega$ load resistance. Sokal made two assumptions or conditions to minimize the power dissipation by the switch. The first condition is the zero voltage switching (ZVS) condition, where the voltage across the MOS switch should be minimized when the current flows. The current should be minimized whenever non zero voltage occurs across the switch. The second condition is the zero voltage derivative switching, (ZVDS) condition where the switching time when the voltage and the current are on, has to be minimized. When the switch is turned off, all the switch current will be transferred to the shunt capacitor and this will result in a high peak drain voltage theoretically equal to (3 VDD) [13].

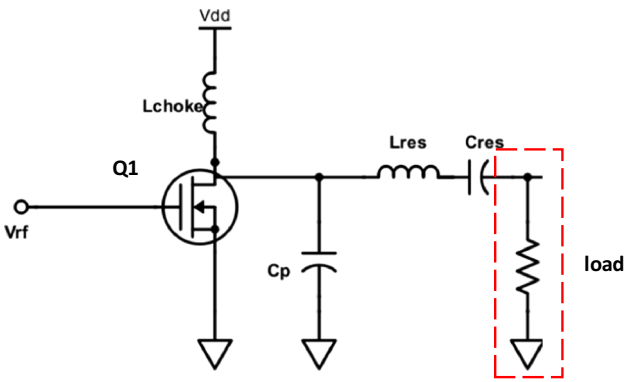

Fig. 1 Class-E PA circuit design

The oscillator is a closed-loop system that has no input and sustains a periodic output signal due to a positive feedback. The Power oscillator is a self oscillating class-E PA that amplifies its own noise and oscillates at ω_o. Recall that any closed-loop system with a positive feedback where A is the forward gain and β is the feedback gain can be represented by the following transfer function:

$$H(s) = \frac{A}{1 - A\beta} \tag{1}$$

The Barkhausen criterion states two conditions for a stable sustained oscillation:

$$magnitude = |A\beta| > 1 \tag{2}$$

$$phase = \angle A\beta = 2.n.\pi \tag{3}$$

where n is any integer. The proposed closed-loop system of a class-E power oscillator is shown in Fig. 2. The network A includes two stages: the class-E PA and a pre-amplifier stage this is necessary to provide the required $(2\pi n)$ phase shift to sustain the oscillation and to maintain enough gain for the oscillation during frequency tuning, while maintaining low dissipated power. An inverter circuit is selected as a pre-amplifier stage and the network β is a unity. The detailed closed-loop system is implemented as shown in Fig. 3(a).

Figure 3(b) depicts the model of the closed-loop system where a class-E PA is modeled as a transconductance $(-G_m)$ amplifier and a series RLC circuit with an equivalent impedance $(Z(s))$. The inverter stage is modeled as a gain stage -1. The series RLC circuit can be expressed as:

$$Z(s) = \frac{R}{L_{res}} \frac{s}{s^2 + (R/L_{res})s + 1/LC_{res}} \tag{4}$$

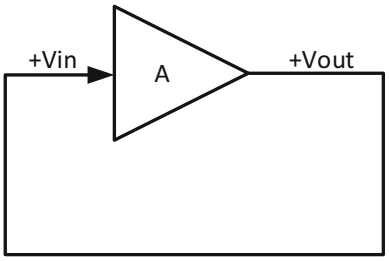

Fig. 2 The block diagram of the proposed oscillator

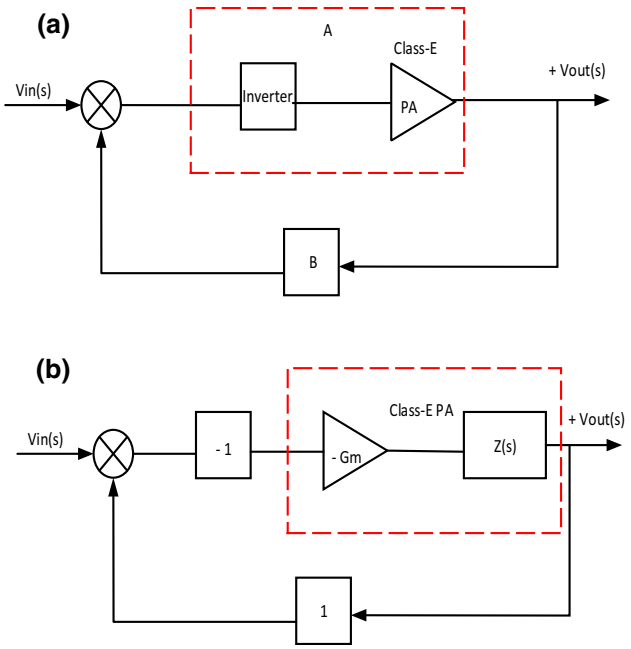

Fig. 3 The feedback model of a class-E PA based oscillator **a** block diagram. **b** Detailed closed-loop system

The loop gain is:

$$G_{loop}(s) = G_m \frac{R}{L_{res}} \frac{s}{s^2 + (R/L_{res})s + 1/LC_{res}} \tag{5}$$

The closed-loop transfer function is:

$$\frac{vout(s)}{vin(s)} = \frac{G_m \frac{R}{L_{res}} \frac{s}{s^2+(R/L_{res})s+1/LC_{res}}}{1 - G_m \frac{R}{L_{res}} \frac{s}{s^2+(R/L_{res})s+1/LC_{res}}} \tag{6}$$

$$\frac{vout(s)}{vin(s)} = \frac{G_m \frac{R}{L_{res}} s}{s^2 + (1 - G_m)\frac{R}{L_{res}} s + \frac{1}{LC_{res}}} \tag{7}$$

The closed-loop complex-conjugate poles are:

$$S_{1,2} = \frac{-\left(\frac{R}{L_{res}}\right)(1 - G_m) \mp \sqrt[2]{\left((1 - G_m)\left(\frac{R}{L_{res}}\right)\right)^2 - \frac{4}{LC_{res}}}}{2} \tag{8}$$

In order to understand more about the oscillation process, the root locus plot is used to show the trajectory of the closed-loop poles in the complex s-plane. When $G_m \frac{R}{L_{res}} > 1$, the poles have positive real part and are located on the right half of the s-plane. When $G_m \frac{R}{L_{res}} > 1$, the poles have positive real part and are located on the right half of the s-plane. When $G_m \frac{R}{L_{res}} = 1$, the poles only have an imaginary part and are located exactly on the imaginary axis. When $G_m \frac{R}{L_{res}} < 1$, the poles have a negative real part and are located on the left half of the s-plane. To start the oscillation, $G_m \frac{R}{L_{res}}$ has to be greater than one where the oscillation amplitude starts to grow exponentially. Due to the MOSFET nonlinearities, the poles go back to the imaginary axis and the oscillation reaches a steady-state (Fig. 4).

3 High efficiency PA circuit design

The design of the PA starts by selecting the MOS size depending on the power supply and the power consumption requirements. Although the MOSFET transistor in a class-E PA is modeled as an ideal switch, in reality there is no ideal switch. Therefore, using MOSFET results in some associated on-resistance (r_{on}) that degrades the efficiency.

$$r_{on} = \frac{L}{\mu_n C_{ox} W (V_{gs} - V_{th})^2} \tag{9}$$

where L is the channel length, μ_n is mobility of N-FET $cm^2/(Vs)$, C_{ox} is the oxide capacitance per unit gate area (F/m^2) and V_{th} is the threshold voltage. The losses associated with r_{on} are studied by Sokals and Raab and can be found as:

$$P_{loses-ron} = 1.3365 \frac{r_{on}}{R} P_o \tag{10}$$

where P_o is the output power and R is the load impedance.

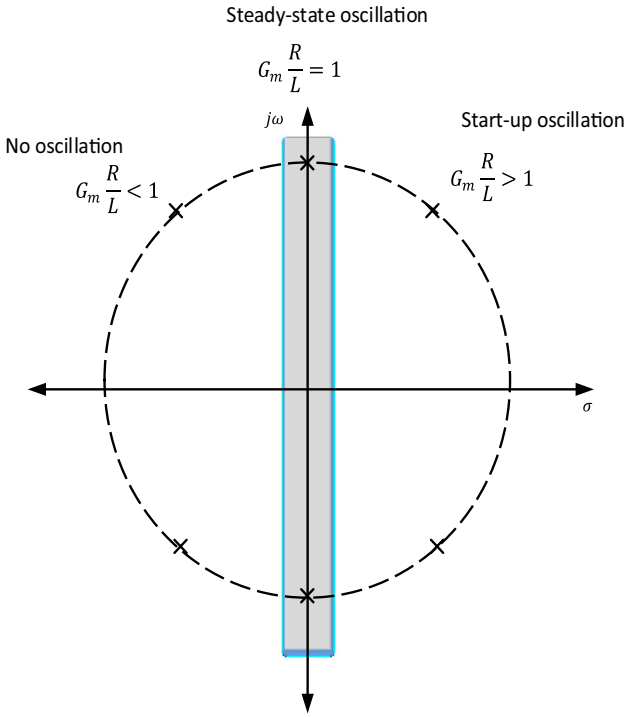

Fig. 4 Root locus analysis of closed-loop poles

$$\eta_{PA} = \frac{1}{1 + 1.4(r_{on}/R_L)} \tag{11}$$

To increase the PA output power, enlarging the MOS size is the most intuitive approach. However, MOS size can not be increased unlimitedly. Figure 5(a) shows the output power and the efficiency of a class-E PA as a function of the transistor width. As expected, the output power increases almost linearly with the MOS size. The efficiency increases linearly due to the reduced r_{on} and to the improved ratio of (r_{on}/R) as expressed in (11). However, after the 80 μm size, the efficiency starts to decline. Figure 5(b) demonstrates the relation between the power consumption (P_{dc}) of a class-E PA and the dimension of the device with respect to Vdd. It shows that the power consumption directly rises with larger devices and a higher Vdd. However, the increment in the dissipated power for a higher Vdd is significantly more than the dissipated power in larger devices. For instance, there is a 0.3 mW increment in P_{dc} for every 10 μm increment in the MOS width under a 0.5 V supply, while a 2 mW increment in P_{dc} occurs under a 1.2 V power supply and the same MOS size.

On the other hand, larger devices increase the associated parasitic capacitances seen at the gate, as can be found in (12). The large MOS devices limit the maximum operating frequency and increase the required power to drive the PA as can be seen in (13), and this leads to more power consumption. Therefore, selecting the optimum dimension for the transistors is critical due to constraints imposed by the resources and by the CMOS technology.

$$f_{max} = 0.0798 \frac{P_{out}}{C_{drain} Vdd^2} \tag{12}$$

$$P_{drive} = f.C_G.V_{gs} \tag{13}$$

where f is the operating frequency, C_G is the total capacitance seen at the gate, V_{gs} is the gate voltage of the PA transistor and C_{drain} is the total capacitance seen at the drain.

The high drain voltage swing is critical in PAs and it must be well controlled in CMOS devices. Figure 6 represents the drain voltage swing in a class-E PA for a varying MOS width, multiple Vdd and a varying gate voltage (V_{gs}).

As shown in Fig. 6(a), the drain voltage increases as the MOS width and Vdd increase. Note, the drain swing becomes more prominent in larger transistors under a high power supply. For example, for a 50 μm MOS width and a

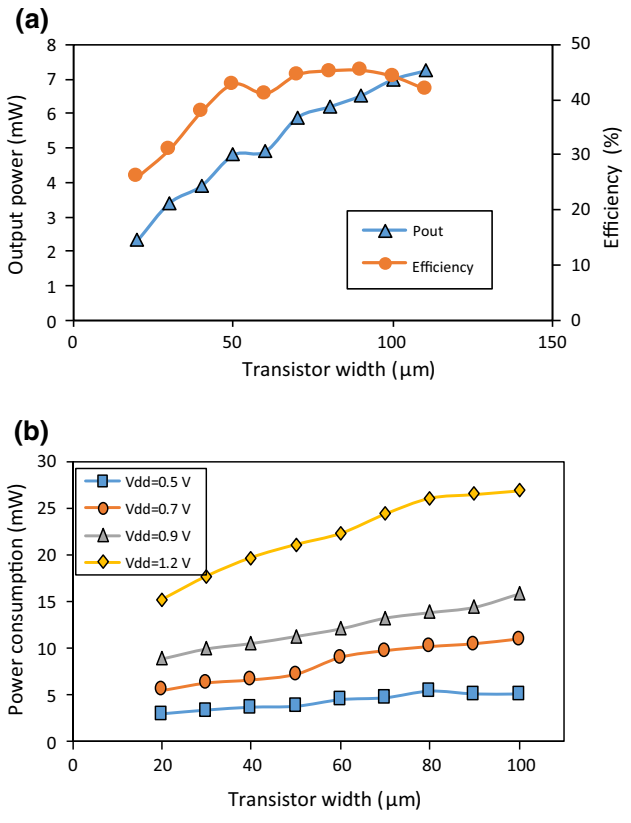

Fig. 5 A class-E PA **a** output power and efficiency verse MOS dimension. **b** DC power consumption of PA versus MOS dimension and Vdd

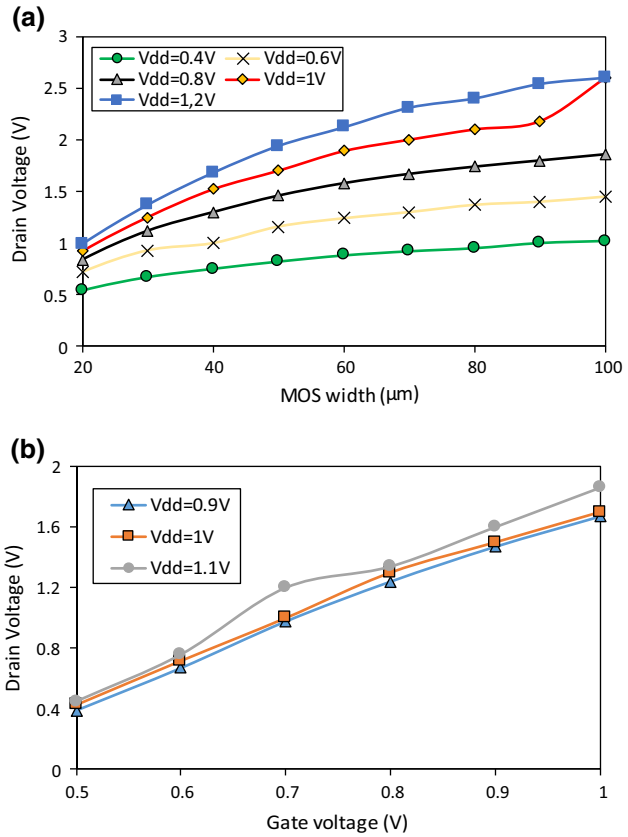

Fig. 6 A class-E PA drain swing **a** versus MOS dimension and Vdd, where Vgs = 1 V, **b** versus gate voltage and Vdd where, MOS width equals to 50 μm and Vdd varies between 0.9 and 1.1 V

0.6 V power supply, the drain swing is 1.1 V, while for a MOS width equal to 100 μm and 1.2 V power supply, the drain swing is 2.6 V.

Figure 6(b) demonstrates the relationship between the gate voltage and the drain swing for 50 μm MOS width and Vdd varies between 0.9 and 1.1 V. Although there wasn't much change in the drain swing for a higher Vdd, the drain voltage increased linearly as V_{gs} increased from 0.5 to 1 V.

The load impedance R_L is determined by the output power requirement as can be seen in (14). The efficiency can be improved by increasing R_L.

$$R_L = 0.577 \frac{V_{dd}^2}{P_{out}} \tag{14}$$

4 Class-E VCO circuit design

Figure 7 shows the detailed architecture of the proposed power oscillator. We have considered a single-end structure and made a careful choice of its parameters. The inverter is implemented with the transistors M_2 and M_3 with 15 μm and 10 μm width respectively. A 0.9 V power supply is selected to maintain a minimum power dissipation at the inverter stage.

The two on-chip inductors are: $L = 4.18$ nH and $L_{res} = 1.1$ nH. In our work, the maximum current through the PA is set to a peak value 7 mA. The optimum width for the PA transistor M_1 is 50 μm. A 0.4 V power supply is selected to control the drain swing and minimize power consumption. The load impedance (R_L) is set to be 50 Ω.

The wide frequency tuning is important to compensate for PVT variation. The frequency tuning is limited by the loop gain of the circuit. Therefore, a small tuning range is selected to reduce the voltage division ratio. To vary the oscillation frequency in series configuration, a large off-chip inductor L_{bias} that provides a DC bias voltage is used. The frequency tuning is implemented by using a varactor bank. The varactor bank includes a MIMCAP with the capacitance C_{fix} in parallel with a dual varactor pair C_{var}. C_{fix} maintains an AC path from the input to the output, while the varactor pair provides the frequency tunability. The value of C_{fix} and C_{var} have been chosen properly to allow frequency tunability without degrading the gain.

$$C_{eff} = C_{fix} + \frac{C_{var}}{2} \tag{15}$$

The effective capacitance C_{eff} varies with a ratio equal to $C_{max}/C_{min} = 1.7$ to tune the frequency between 1.6 and 2.7 GHz when the control voltage $(V_{control})$ changes

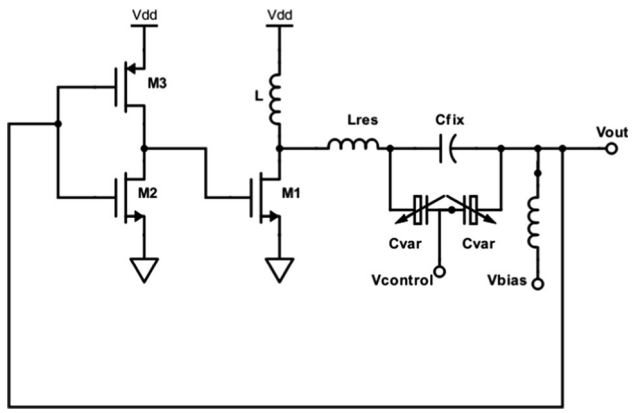

Fig. 7 The proposed class-E power oscillator circuit design

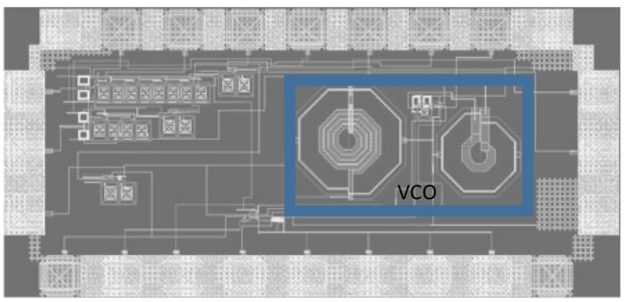

Fig. 8 Photograph of the proposed oscillator layout

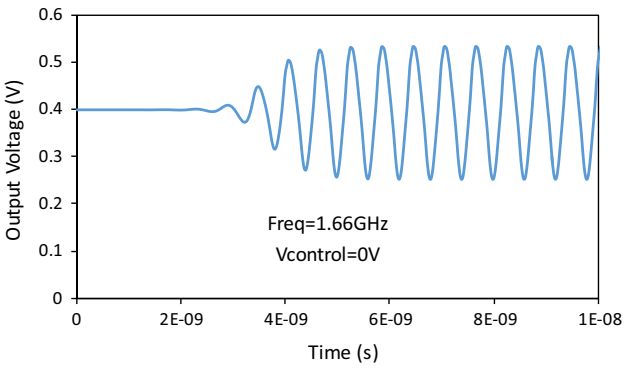

Fig. 9 The oscillator output voltage at time domain

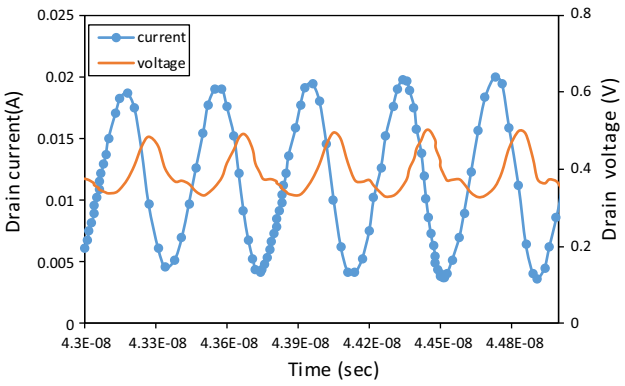

Fig. 10 The voltage and the current curves of the PA drain

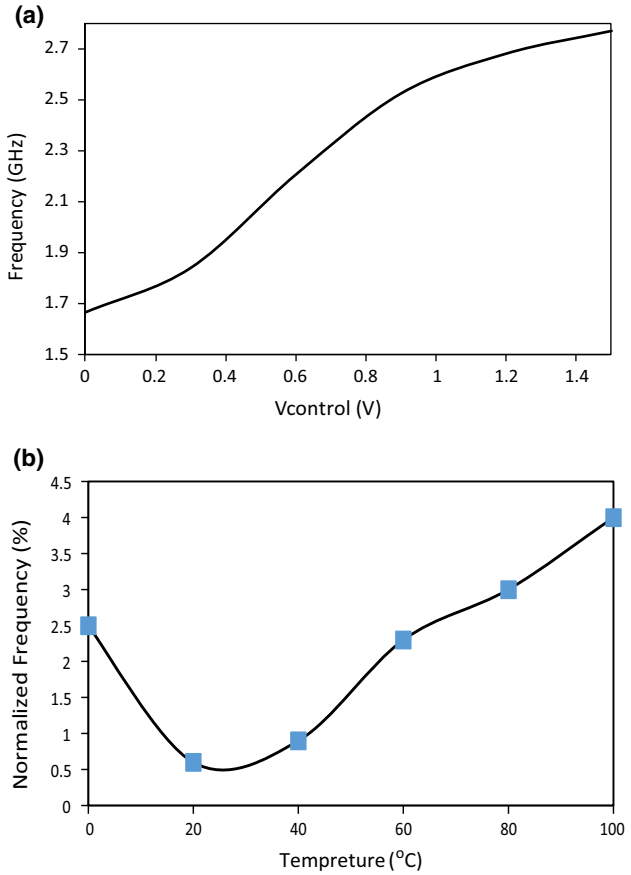

Fig. 11 The oscillator post-layout results for **a** the tuning range, **b** the frequency offset versus temperature

between 0 and 1.5 V, where $C_{fix} = 0.3$ pF, $V_{bias} = 0.4$ V and $L_{bias} = 100$ nH, such that:

$$f = \frac{1}{2\pi\sqrt{L_{res}\, C_{eff}}} \tag{16}$$

5 Implementation and results

The proposed oscillator is implemented in CMOS 65 nm. The layout photograph is shown in Fig. 8. The core of the VCO occupies an active area of about 0.16 mm^2. Figure 9 illustrates the oscillation amplitude at the time domain. The circuit starts to oscillate after 3 ns with peak-peak value equal to 300 mV (Vcontrol = 0 V). The drain voltage swing and the switching behavior of the PA is shown in Fig. 10.

Figure 11(a) demonstrates the post-layout results of the tuning range. It is between 1.66 and 2.7 GHz under a tunable control voltage between 0 and 1.5 V and a supply voltage of 0.4 V. This wide tuning range enables the oscillator to compensate for PVT variation. The oscillator is robust to ±15% frequency deviation from a 2.44 GHz

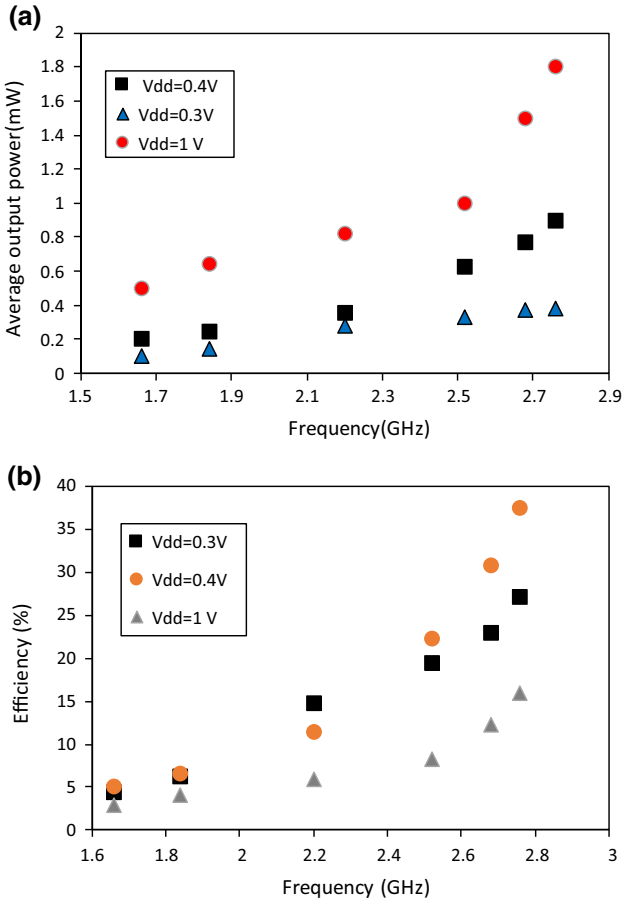

Fig. 12 The proposed oscillator post-layout results for **a** the average output power, **b** the power efficiency

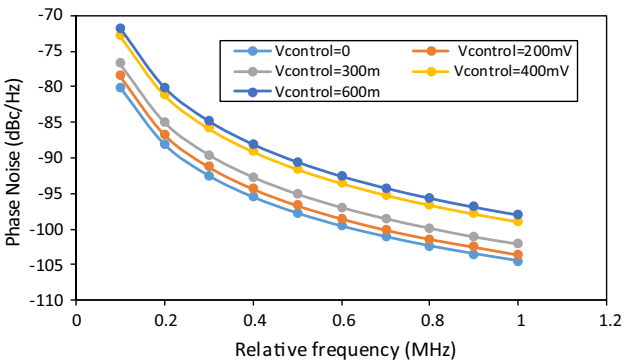

Fig. 13 The phase noise results with respect to control voltage at 1 MHz offset frequency

nominal frequency. The PA and the varactor are nonlinear and this reflects on the transmitter spectrum shown in Fig. 11(a) where the operating frequency does not increase linearly with the increases of the control voltage that applied to the varactor. The oscillator performance against the temperature variation between 0°C to 100 °C is illustrated in Fig. 11(b). The results show that less than ±5%

Table 1 Performance comparison with previous state-of-the-art VCO designs

Specifications	This work	[14]	[9]	[16]	[15]
Process	CMOS 65 nm	CMOS 65nm	CMOS 65 nm	CMOS 65nm	CMOS 65nm
Frequency (GHz)	2.4	59	1.95	3.9–6.1	60 GHz
Tuning range (GHz)	1.1	5.4%	0.4	42%	10 GHz
Power supply (V)	red 0.4	1	2.5	1.3	0.5
Power dissipation (mW)	2.4	16.5	337	13–23	157
Output power (dBm)	− 0.45	− 0.9	22	–	9.7
Efficiency, $\eta(\%)$	37.5	4.9	46.8	–	31
Phase noise (dBc/Hz)	− 108	− 90.3	N/A	− 123	− 91
FOM* (dBc/Hz)	− 172	− 167.3	N/A		164.1

$FOM^* = L(\Delta\omega) + 10\log(PD/1\,\mathrm{mW}) - 20\log\omega_o/(\Delta\omega)$

frequency deviation occurs over 100 °C temperature change.

Figure 12(a) shows the oscillator output power between 0.1 and 2 mW under a supply voltage is between 1.3 and 1 V and a frequency range of 1.66 to 2.77 GHz respectively. The oscillator efficiency between 5 and 37.5% under a supply voltage is between 1.3 and 1 V as depicted in Fig. 12(b). The results reveal that the efficiency decreases with high Vdd due to the increased power dissipation . A 0.4 V power supply is the optimal due to the achieved 37.5 % efficiency, 0.9 mW output power and 2.4 mW power dissipation

The VCO achieves a figure of merit (FOM) ranging from −158 to −172 dBc/Hz as described in (17) with trade-off parameters that include phase noise ($L(\Delta\omega)$), power dissipation (PD), carrier frequency (ω_o) and offset frequency ($\Delta\omega$) . The phase noise of the VCO at 1 MHz offset frequency is ranging between − 100 to − 110 dBc/Hz as demonstrated in Fig. 13.

$$FOM = L(\Delta\omega) + 10\log(PD/1\,\mathrm{mW}) - 20\log\omega_o/(\Delta\omega) \quad (17)$$

A summary of the results is given in Table 1, and the performance comparison with recently reported CMOS VCOs is carried out. The comparison reveals that in terms of power supply and power consumption, this work uses the lowest power supply and it has the lowest power consumption in compare to all the reported designs. Our output power is higher than [14] and lower than [9, 15]. Our power efficiency is the highest among others except in [9] where the oscillator consumes more power. Moreover, our phase performance is better than all the reported designs except [16]. Finally, the FOM of this work is the highest in compare with other state of the arts.

6 Conclusion

An energy-efficient, low-voltage, class-E power oscillator in CMOS 65 nm is presented. The requirements and the trade-off between design parameters were reviewed. A system-level design methodology for a class-E power oscillator was demonstrated. Finally, a complete circuit design of a low voltage class-E oscillator in CMOS 65nm was presented. The design utilized a class-E PA as the core of the design with a positive feedback. The oscillator achieved a peak output power of −0.5 dBm and a peak efficiency of 37.5% under a 0.4 V power supply and frequency tuning range between 1.66 and 2.7 GHz.

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