



A compact 0.045–2.3 GHz frequency synthesizer with a wide tuning range low phase noise VCO for software defined radios

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Abstract

A compact 0.045–2.3 GHz wideband fractional-N frequency synthesizer (FS) for software defined radios (SDR) applications is presented in this paper. Based on a single phase locked loop (PLL) that employs one integrated inductor-capacitor voltage controlled oscillator (VCO), the proposed FS can provide a wide operating frequency range. The VCO adopts an optimized circular inductor to mitigate the phase noise degradation caused by the high VCO gain. The in-band phase noise is optimized by employing current mode logic dividers and true single phase clock dividers. The PLL provides the differential outputs ranging from 2.3 to 4.6 GHz and the 0.045–2.3 GHz quadrature local oscillator signals are generated by the following divider chain. The proposed FS is implemented in TSMC 180 nm RFCMOS process and provides a phase noise performance less than -116 dBc/Hz at 1 MHz offset. The maximum power consumption is 54 mW. The die size including pads and I/O is 1.92 mm² with an active core area of 1.13 mm². This proposed circuit has the great potential for SDR applications.

Keywords Frequency synthesizer (FS) · Voltage controlled oscillator (VCO) · Phase locked loops (PLL) · Software defined radio (SDR)

1 Introduction

With the developing requirement for higher data rate, longer operating range and shorter latency applications, many wireless protocols and standards are springing up, such as the NB-IoT, LoRa and Sigfox. The main differences between these standards and protocols are the realizations of the digital base band and the media access control layer. In other words, the analog base band and the radio front end could be implemented by employing the unified structure. In order to support as much protocols and standards as possible, the software defined radio (SDR) is a possible solution. One of the most challenging and important block in such a SDR is the frequency synthesizer

(FS), which should provide octave frequency range, suitable performance and consume reasonable power.

There are three representative structures of such a wideband synthesizer. The first one is to generate broadband outputs with several phase locked loop (PLL) and each PLL covers a narrow band outputs, as presented in Fig. 1(a). By utilizing this structure, the performance of the FS can be optimized conveniently in the traditional way at the cost of larger die size.

The second one is to utilize multiple voltage controlled oscillator (VCO) cores that are at different frequencies and followed by a set of dividers [1–3], as shown in Fig. 1(b).

By reusing some blocks such as the phase frequency detector (PFD) and the charge pump (CP), the die size is reduced. The synthesizer can provide a wide tuning range by switching between these VCO cores. Compared with the first FS structure, this one occupies smaller area. However, as the VCO cores occupy larger than the reused blocks, the reduced die size is negligible.

The third method is to utilize quadrature VCOs (QVCOs) and single side band (SSB) mixers [4, 5] and the representative structure is shown in Fig. 1(c). This

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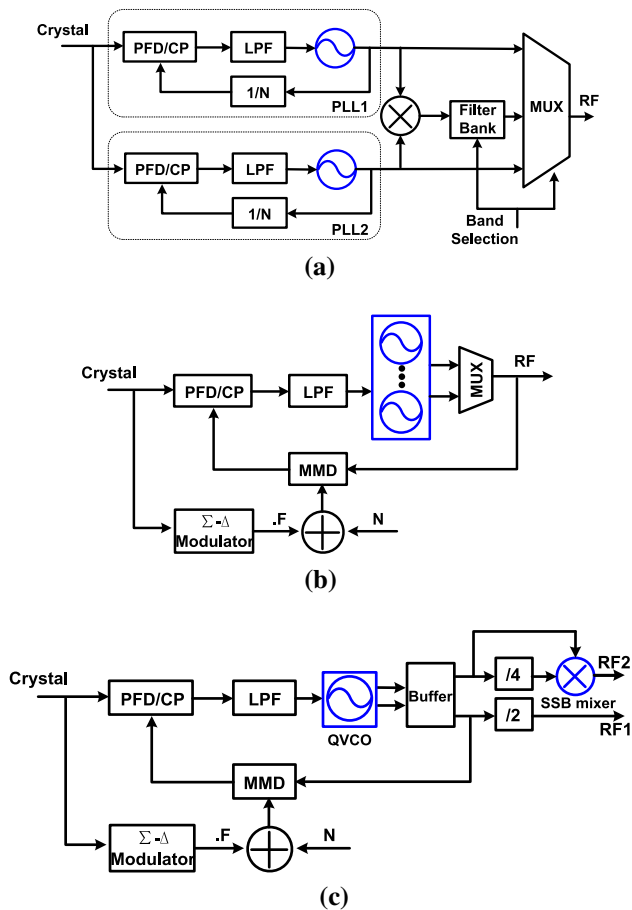


Fig. 1 **a** Multi-loop frequency synthesizer structure, **b** frequency Synthesizer with several VCOs, **c** frequency synthesizer adopting QVCO and SSB mixer

structure releases the requirement of the VCO frequency tuning range, thus adopting one QVCO is sufficient. However, at least two inductor coils should be employed in a QVCO. Moreover, the inductor-capacitor (LC) loads are usually utilized in the SSB mixer to provide sufficient image sideband rejection ratio (ISRR), which means that this kind of FS structure could also occupy large area. In addition, the harmonics and unwanted sidebands in the output are harmful for the performance.

The aforementioned structures, which are widely used in broadband FS design, mainly focus on the FS performance, and neglect the area cost. A comparison between the FS area and the inductor-related circuit area is shown in Fig. 2. The proportion of the inductor-related circuits in FS is 30–50%. Reducing the use of inductor coils in FS can save area significantly. As the process design kit (PDK) provides inductor coils that are not optimized for certain applications, it is better to design and optimize the inductor with our own for the quality factor (Q) sensitive blocks such as the VCO.

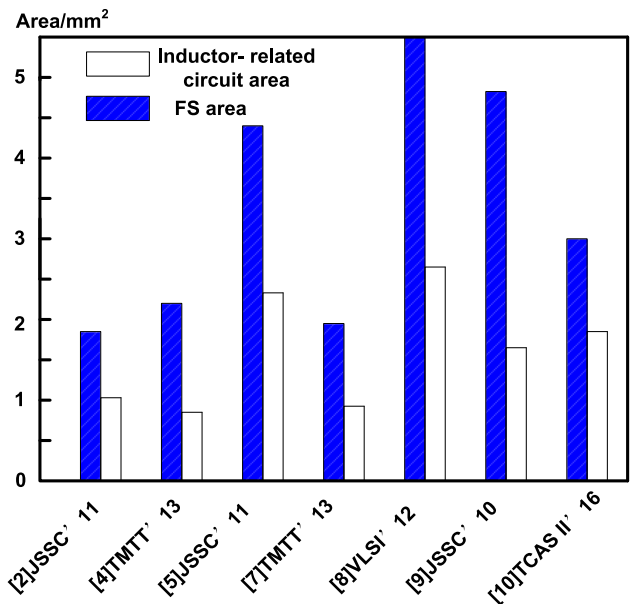


Fig. 2 The area proportion comparison between FS and inductor-related circuits in [2–5, 9–11]

The aim of this paper is to design and implement a wideband and compact frequency synthesizer with small area. By utilizing only one VCO core, the FS could occupy small area. However, as the VCO frequency tuning range is fixed, the VCO gain could be very large. In order to mitigate phase noise degradation caused by the large VCO gain, the inductor coil is custom designed and optimized.

The paper is organized as follows. The frequency synthesizer architecture the frequency planning are discussed in Sect. 2 The inductor optimization and the wideband low phase noise VCO design is presented in Sect. 3. The rest of the important building blocks of the proposed synthesizer are described in Sect. 4 and the measurement results are presented in Sect. 5. The paper is closed with the conclusion in Sect. 6.

2 FS architecture and frequency planning

The proposed FS is depicted in Fig. 3(a). The PLL core gives differential outputs from 2.3 to 4.6 GHz. The VCO in the proposed FS employs only an optimized inductor. The upper frequency of VCO should be two times larger than the lower frequency to generate successive quadrature signals by divide-by-two operation. The programmable multi-mode divider (PMMD) consists of a 17-bit MASH 1-1-1 sigma-delta modulator and an analog divider (DIV) and provides the division ratio from 64 to 254. The output of the PMMD is a 24 MHz clock, which feeds back to the input of the PFD for frequency and phase detection. A charge pump (CP) leveraging 15 parallel replica-biased

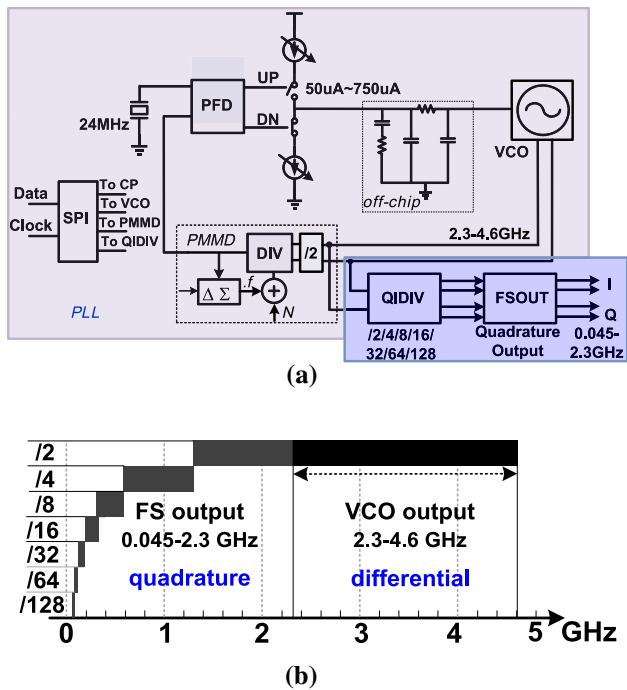


Fig. 3 a The proposed FS structure, b frequency planning

current units is employed to compensate the bandwidth variation caused by different division ratios and VCO gains. The configurable 50–750 μA CP current is fed into the off-chip filter. A frequency resolution better than 10 kHz can be obtained over the entire frequency range. The quadrature divider (QIDIV) provides division ratio of 2/4/8/16/32/64/128 for post synthesizing. All these controlling signals are programmed by the on-chip serial peripheral interface (SPI). The frequency planning is presented in Fig. 3(b). The differential VCO outputs are post processed by QIDIV and then the 0.045–2.3 GHz quadrature outputs are obtained.

3 Inductor optimization and VCO design

3.1 Inductor optimization

The quality factor of inductor affects the VCO performance significantly. Although the PDK inductors are widely employed in some Q-insensitive circuits, they are not optimized and are inadequate for certain applications. As one VCO core is employed in the PLL to cover 2.3–4.6 GHz, the VCO gain is relatively large. To mitigate the phase noise degradation caused by the large VCO gain, the inductor used in the VCO core is custom designed and optimized.

For the circular inductors provide good symmetry characteristic and provide superior Q performance, a circle

shape inductor coil is optimized and utilized in the VCO. The proposed inductor is shown in Fig. 4 with two parallel turns spacing 4 μm. The width of the two parallel turns is 27 μm and the radius of the outer turn is 420 μm. The inductor coil is implemented with the ultra-thick top metal6 (M6), which is of 4.6 μm for radio frequency use. The distance between M6 and substrate is 8.15 μm. The thickness, resistivity, and permittivity of the substrate are 250 μm, 10 Ω cm and 11.9, respectively.

The simulation results of the inductance (L) and Q are presented in Fig. 4. Compared with a same dimension PDK-inductor, the optimized inductor provides a smaller inductance of 40–50 pH in the frequency range from 0.1 to 10 GHz. From 2 to 5 GHz, the optimized inductor provides an inductance of 600–610 pH while achieving a Q of 16–19. The peak Q is 20 at 3.6 GHz and that of the PDK-inductor is 18.5. The optimized inductor presents a higher Q of 1–2 than the PDK-provided one from 1 to 4 GHz. As frequency increasing over 4.5 GHz, the PDK-inductor shows a higher Q. The area of the optimized inductor is 520 × 520 μm². Two ground-signal-ground (G-S-G) pads with 100 μm pitch size are added for on-wafer testing and the signal pad only uses M6 for low parasitic capacitance. The measurement results in Fig. 5 shows that the optimized inductor provides an inductance of 570 pH with Q varying from 24.4 to 20 in the frequencies between 2 GHz and 5 GHz.

3.2 Amplitude analysis

$$L(\Delta\omega) = 10 \log \left[\frac{2FkT}{P_{sig}} \left[1 + \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right] \left(1 + \frac{\Delta\omega_1/f^3}{\Delta\omega} \right) \right] \quad (1)$$

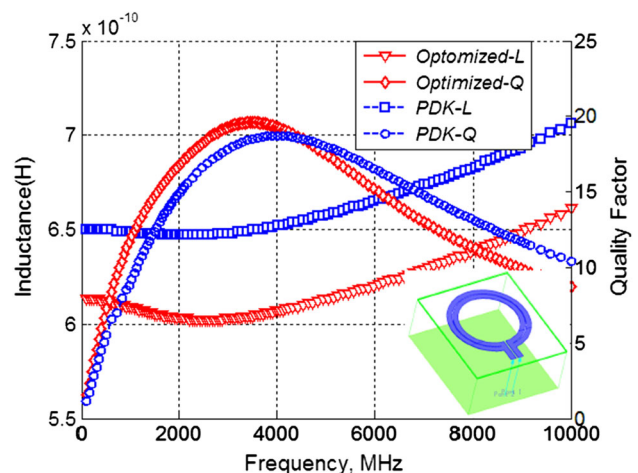


Fig. 4 Inductance and Q comparison between optimized inductor and PDK-inductor

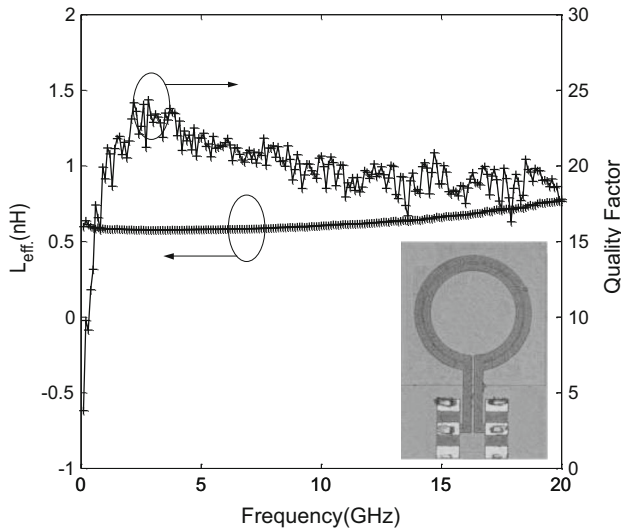


Fig. 5 Micrograph of the proposed inductor and the measurement results

According to Lesson’s model, the phase noise could be optimized by increasing the VCO output amplitude as shown in (1). However, the increased amplitude would be accompanied with a larger factor F , which represents the noise contribution of the cross-coupled negative pair, thus deteriorating the phase noise. The effects of the VCO output on phase noise performance have been observed and the voltage limit region and current limit region are proposed. It is believed that the VCO provide optimal phase noise performance when working at the boundary between the two regions. Many VCO structures have been proposed with automatic amplitude calibration (AMC) circuit for optimal phase noise [6–8]. In addition, the large output signal would drive the negative cross-coupled pair from saturation region into linear region, so the small signal linear model of MOSFET is inadequate for analysis.

The amplitude is such a crucial element that affects phase noise, so the optimal phase noise performance would be achieved if the amplitude is selected properly. As for a VCO that oscillates at frequency ω_0 , the transconductance is strictly periodic. Therefore, the output amplitude effects on phase noise can be analyzed by utilizing Fourier series. The simulation schematic and transconductance simulation results are presented in Fig. 6(a, b) separately. The transconductance can be presented in Fourier expression as:

$$g_m = \sum_{n=-\infty}^{+\infty} \overrightarrow{g^{(n)}} e^{jn\omega_0 t} \tag{2}$$

If the output signal is $V_0(t) = V_A \cos(\omega_0 t)$, the current $I_0(t)$ flowing through M_1 or M_2 is given by:

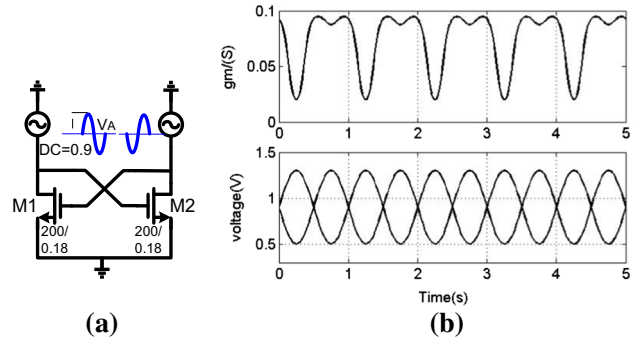


Fig. 6 a Simulated schematic of negative pair, b simulation results of transient transconductance

$$I_0(t) = \int g_m \frac{dV_0(t)}{dt} dt \tag{3}$$

For $\overrightarrow{g^{(2)}} = \overrightarrow{g^{(-2)}}^*$, where $*$ denotes conjugate, $\overrightarrow{g^{(2)}} = G_2 e^{j\varphi}$, $\overrightarrow{g^{(-2)}} = G_2 e^{-j\varphi}$. $\overrightarrow{I_0(t)}$ can be written as:

$$\overrightarrow{I_0(t)} = V_A G_0 \cos(\omega_0 t) - V_A G_2 \cos(\omega_0 t + \varphi). \tag{4}$$

The effective transconductance $\overrightarrow{g_{eff}}$ is given by the ratio between the output current and the input voltage.

$$\overrightarrow{g_{eff}} = \overrightarrow{g^{(0)}} - \overrightarrow{g^{(2)}} \tag{5}$$

Considering a narrow band voltage noise at $n\omega_0 - \alpha$ with power spectrum density of N_0 , the generated current source is

$$i_{n,gm} = \left(\frac{V_{noise}}{2} e^{j(n\omega_0 - \alpha)t} + \frac{V_{noise}}{2} e^{-j(n\omega_0 - \alpha)t} \right) \times \sum_{n=-\infty}^{+\infty} \overrightarrow{g^{(n)}} e^{jn\omega_0 t}. \tag{6}$$

where $v_{noise} = \sqrt{2N_0}$ and α is the offset frequency. The noise current sources around ω_0 are:

Upper side:

$$\frac{v_{noise,l}}{2} \overrightarrow{g^{-(n+1)}} e^{-j(\omega_0 + \alpha)t} + \frac{v_{noise,l}}{2} \overrightarrow{g^{(n+1)}} e^{j(\omega_0 + \alpha)t} \tag{7a}$$

Lower side:

$$\frac{v_{noise,l}}{2} \overrightarrow{g^{-(n-1)}} e^{j(\omega_0 - \alpha)t} + \frac{v_{noise,l}}{2} \overrightarrow{g^{(n-1)}} e^{-j(\omega_0 - \alpha)t} \tag{7b}$$

Considering the single side band noise current, for instance, the upper side band noise, it is

$$i_{n,gm,u} = v_{noise,l} G_{n+1} \cos((\omega_0 + \alpha)t + \varphi_{n+1}) + v_{noise,u} G_{n-1} \cos((\omega_0 + \alpha)t + \varphi_{n-1}) \tag{8}$$

Provided that the noise currents are uncorrelated, the SSB noise power spectrum density can be given by:

$$\overrightarrow{i_{n,gm,u}^2} = 2N_0 \sum_{n=0}^{\infty} (G_n)^2 \tag{9}$$

The impedance of the LC tank at a small offset frequency α may be approximated by:

$$|Z(\omega_0 + \alpha)| \approx \frac{\omega_0 R}{2Q\alpha} \tag{10}$$

Multiplying the current noise by the squared magnitude of the tank impedance, the voltage SSB power spectrum density is

$$\overline{v_{n, gm, u}^2} = 2N_0 \sum_{n=0}^{\infty} (G_n)^2 \left(\frac{\omega_0 R}{2Q\alpha}\right)^2 \tag{11}$$

For the amplitude control characteristic of the oscillators, only one half of the noise power turn into phase noise. Therefore, the phase noise caused by transconductance nonlinearity is

$$L(\alpha) = 10 * \log \left(\frac{N_0 \sum_{n=0}^{\infty} (G_n)^2 \left(\frac{\omega_0}{Q\alpha}\right)^2}{2V_A^2 \left(\overrightarrow{g^{(0)}} - \overrightarrow{g^{(2)}}\right)^2} \right) \tag{12}$$

Setting the conversion gain in (10) as:

$$G = \frac{\sum_{n=0}^{\infty} (G_n)^2}{2V_A^2 \left(\overrightarrow{g^{(0)}} - \overrightarrow{g^{(2)}}\right)^2} \tag{13}$$

The simulation results of the conversion gain against the output amplitude is presented in Fig. 7. In the current limited region, phase noise decreases as output amplitude increases. The optimal amplitude is around 550 mV, beyond which the phase noise then increases. The simulation result is in accordance with the conventional theory of amplitude effects, which is usually an empirical model. When V_A increases beyond 800 mV, the conversion gain G decreases again because of the large output amplitude.

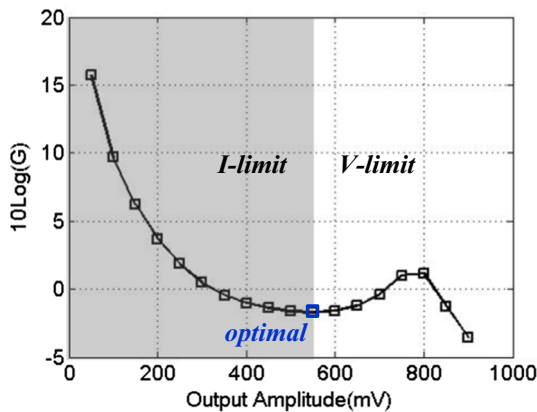


Fig. 7 Relationship between conversion gain and output amplitude

3.3 VCO design

The proposed wideband low phase noise VCO with the optimized inductor is presented in Fig. 8(a). The VCO consists of a current bank, a switch-cap bank, and a pair of negative resistance and provides the tuning range from 2.3 to 4.6 GHz. In order to extend the frequency tuning range without sacrificing VCO gain, a switched metal–insulator–metal (MIM) cap bank is utilized. The metal–oxide–semiconductor field effects transistors (MOSFETs) PM5 and PM6 detect the peak output amplitude and feed it back to PM1 and PM2 to control the output amplitude in a reasonable region, as the aforementioned analysis suggests. For example, as the output amplitude increasing, the over drive voltages of PM1 and PM2 decrease accordingly, yielding a smaller current flowing through the VCO. This feedback mechanism can make the VCO output amplitude within a reasonable region. The cross-coupled NMOS and PMOS pairs are employed for sufficient negative resistance. A current bank is adopted to adjust the current consumption of the VCO as oscillating frequency changes and prevent the VCO working in the voltage-limit region.

The phase noise simulation results of the VCO with the proposed inductor and the PDK-inductor at carrier frequencies of 2.5 GHz and 5.6 GHz are provided in Fig. 8(b). At the carrier frequency of 2.5 GHz, the spot phase noise of the VCO with the optimized and the PDK inductor at 100 kHz offset are -106.5 dBc/Hz and -104.5 dBc/Hz respectively. The proposed VCO with the optimized inductor provides 2–3 dB lower phase noise than the PDK-inductor. The simulation results demonstrate that the optimized inductor and the amplitude control structure are beneficial for better phase noise performance.

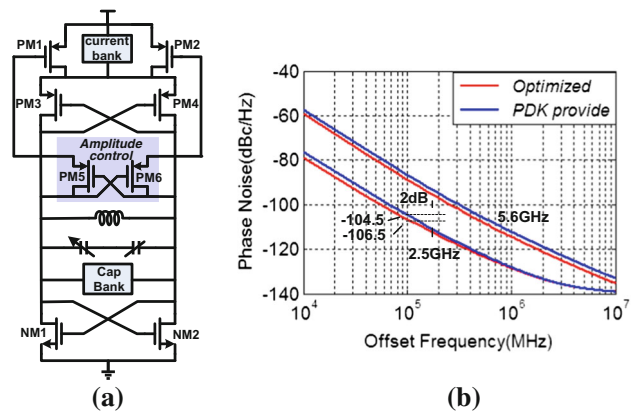


Fig. 8 a The proposed VCO, b phase noise comparison

4 Resting important building blocks

4.1 DIV design

The proposed analog divider is made up of six cascaded divide-by-2/3 dividers and the structure is presented in Fig. 9(a). The effective divider stages are five or six respectively when the controlling signal OUP <6> is logic low or high. The divider provides the successive division ratio from 32 to 127. The current-mode logic (CML) divider can work at higher frequency while it consumes static current. The operating frequency of a true single-phase clocked (TSPC) divider is lower while it does not consume static power. Moreover, this TSPC divider can not only save power but also decrease phase noise, which is

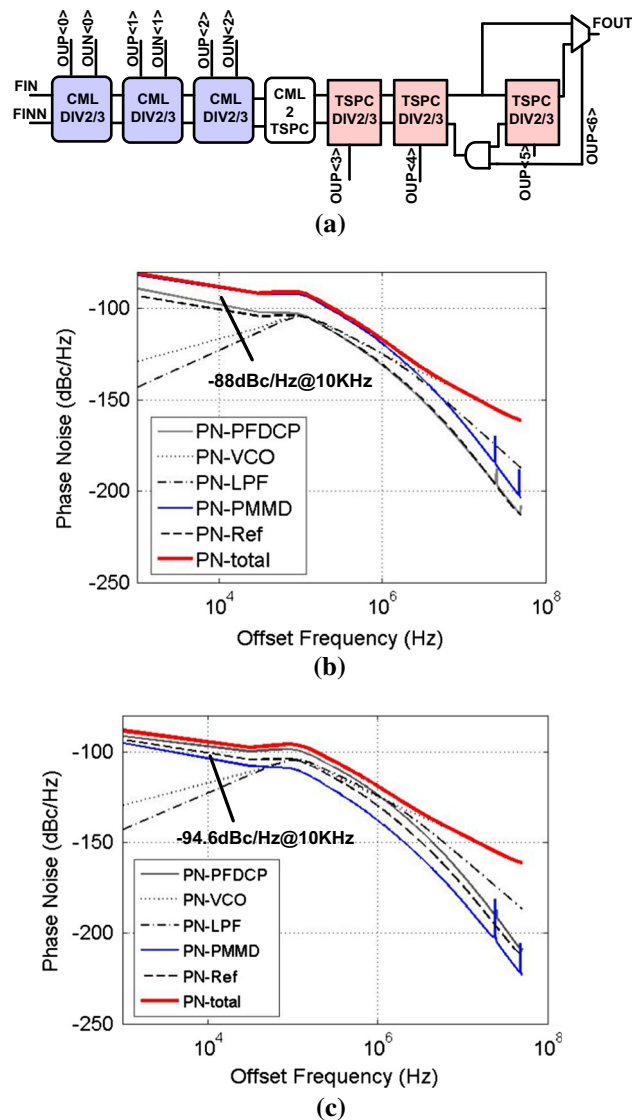


Fig. 9 a Designed PMMD structure, b FS phase noise with all CML dividers, c FS phase noise with CML and TSPC dividers

usually neglected. Therefore, the first three stages are composed of CML dividers for higher operating frequency and the last three stages are TSPC dividers for lower power consumption and phase noise. The phase noise simulation results at the PLL output when employing the all CML dividers and the CML-TSPC dividers are presented in Fig. 9(b, c) separately. As shown in Fig. 9(b), the spot phase noise at 100 kHz offset is -88 dBc/Hz from a 5 GHz carrier frequency and the in-band phase noise is dominated by the divider noise. The spot phase noise decreases to -94.6 dBc/Hz when utilizing the proposed CML-TSPC divider. At this situation, the in-band phase noise is dominated by PFD and CP output noise, as presented in Fig. 9(c).

4.2 CP design

The proposed current steering CP cell is depicted in Fig. 10(a) with a 1.8 V supply. The MOSFETs PM1/PM2 and NM1/NM2 are the current mirrors with the bias voltage VB1–VB4 respectively. The source and sink current of the cell are 50 μ A with a mismatch less than 1%. PM3/

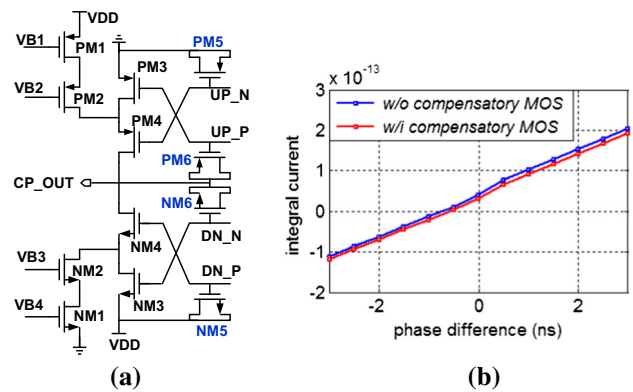


Fig. 10 a The optimized current steering CP cell, b simulation results with and without compensatory MOSFETs

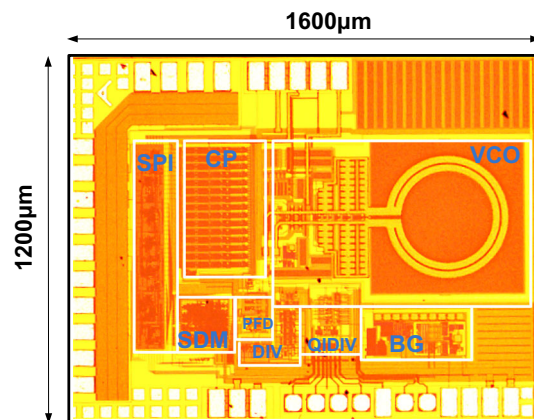


Fig. 11 Micrograph of the proposed FS

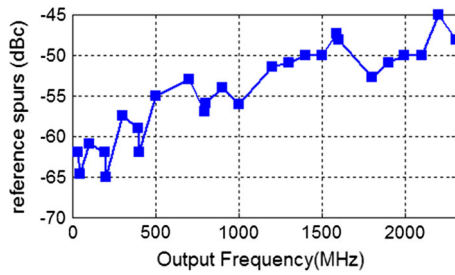


Fig. 12 Reference spurs measurement results

PM4 and NM3/NM4 are the current switches controlled by the PFD outputs UP_P/UP_N and DN_P/DN_N. When PM4 turns off, the source current flows through PM1, PM2 and PM3, or through PM1, PM2 and PM4, conversely. This kind of CP cell reduces the switching time by employing the current switch. It is a useful characteristic as higher working frequency of PFD and CP is beneficial for the in-

band phase noise and reference spur. PM5/PM6 and NM5/NM6 are compensatory MOSFETs. The source and drain of PM5 are connected to ground and that of NM5 are connected to VDD. PM6 and NM6 are linked together with their source and drain connected to CP_OUT. When turning on, PM4 would absorb holes to invert the MOSFET channel from N-type to P-type. These holes could come from PM2, PM3 and the following loop filter if PM6 is not adopted, leading to the spark current and ripple voltage on the loop filter output. The function of these compensatory MOSFETs is to provide or absorb the channel carriers when the current switches turn on or off. The simulation results of the integral CP output current versus the UP_P to DN_P phase differences is presented in Fig. 10(b). The integral current of a CP cell with compensatory MOSFETs is less than that without compensatory MOSFETs, indicating the smaller spark current and reference spurs when PLL is locked.

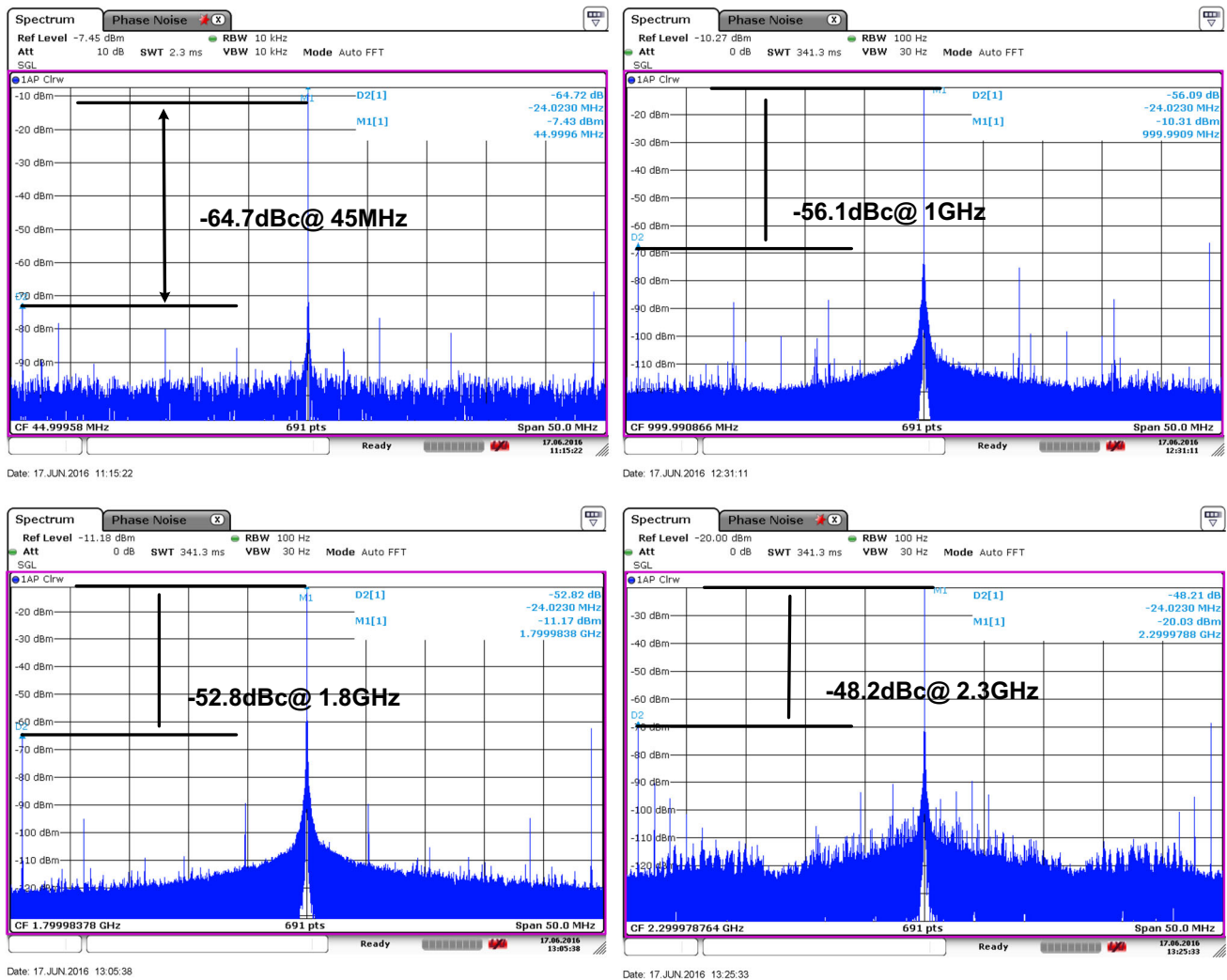


Fig. 13 Output spectrum at 45, 1000, 1800 and 2300 MHz

5 Measurement results

The proposed FS was implemented in TSMC 180 nm RFCMOS process and the micrograph is presented in Fig. 11. The area of the FS including PADS and I/O is $1200\ \mu\text{m} \times 1600\ \mu\text{m}$ and the active area is $1.13\ \text{mm}^2$. All blocks are integrated on chip except for the low pass filter. The VCO occupies an area of $0.51\ \text{mm}^2$. The chip was packaged in a QFN40L package and mounted on a printed circuit board for test. The FS is powered by an external low dropout regulator with an output voltage of 1.8 V. A 48 MHz crystal is utilized as the input reference signal and a divide-by-2 divider is insert between the crystal and the PFD. The output spectrum and phase noise performance are measured using a Rohde Schwarz FSV7 signal analyzer. The settling time is measured using the Tektronix oscilloscope. The maximum current consumption including I/O and test buffer is 30 mA. The VCO gain varies from 30 to 300 MHz/V.

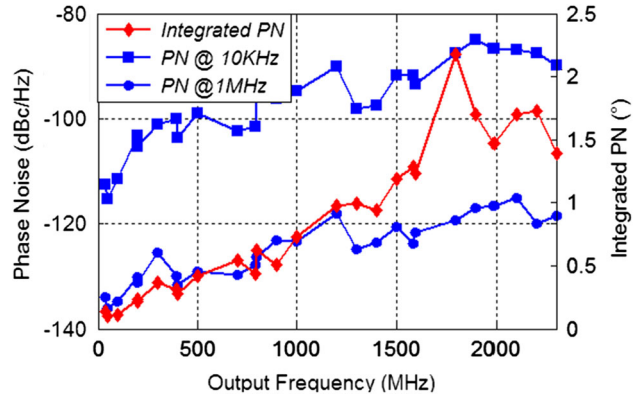


Fig. 15 Spot and integrated phase noise measurement results

The measurement reference spurs at 24 MHz offset from 45 to 2300 MHz is presented in Fig. 12 with the peak spurs of -45dBc at 2300 MHz. It is believed that the large reference spurs are caused by the CP mismatch and the

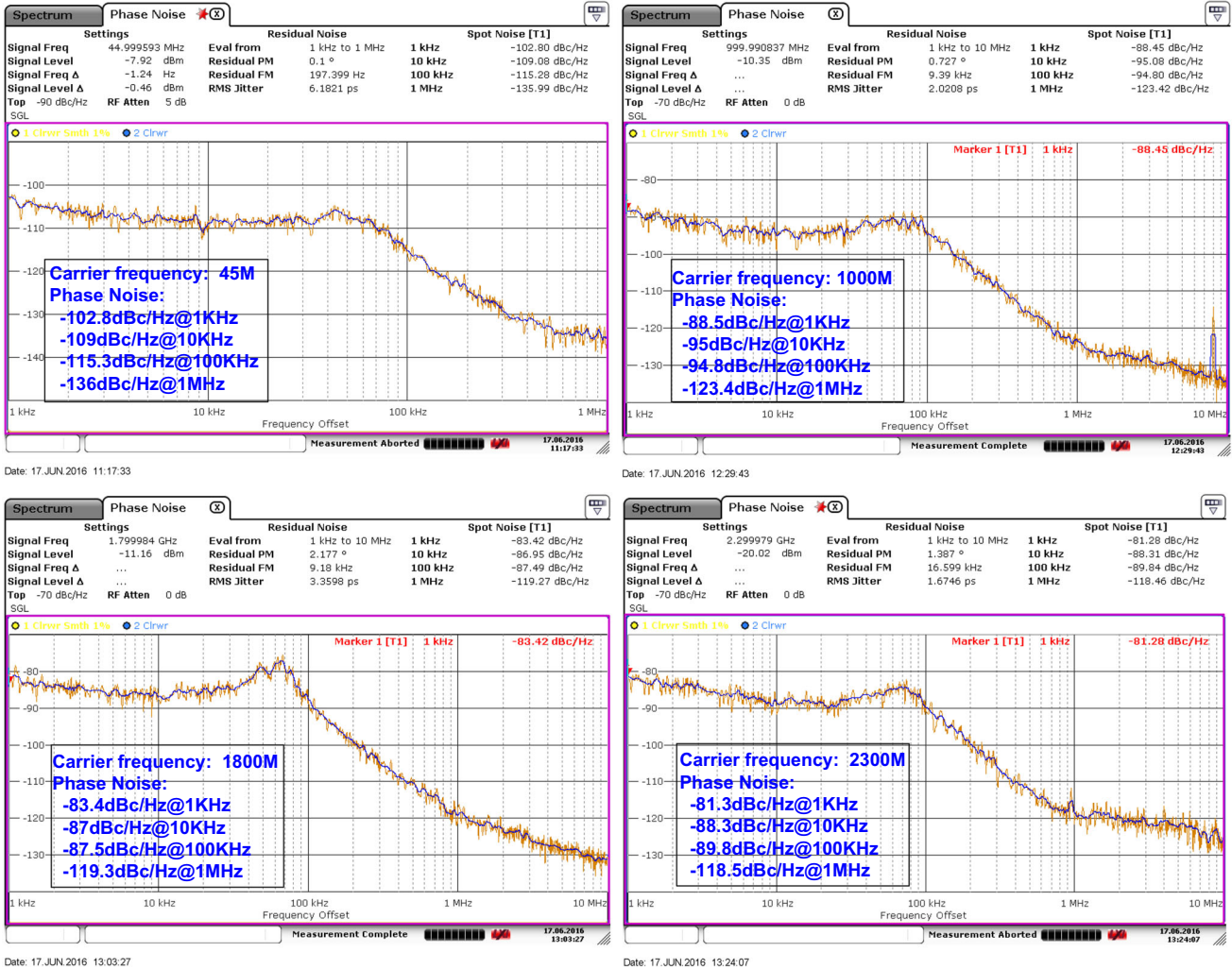


Fig. 14 Phase noise measurement results at 45, 1000, 1800 and 2300 MHz

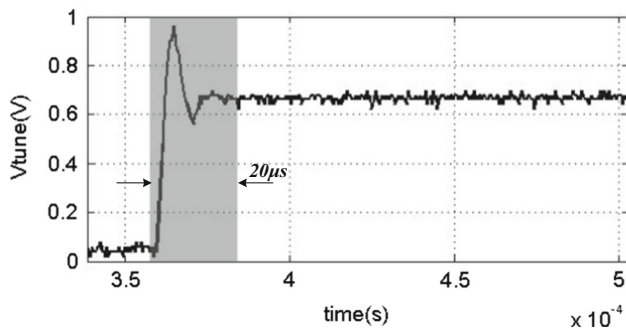


Fig. 16 Settling time at 900 MHz

clock feedthrough from the substrate and the power supply. Careful layout isolation and shield together with a properly optimized CP mismatch would be beneficial for the reference spurs. The output spectrum at 0.045/1.8/2.3 GHz are shown in Fig. 13 and the reference spurs are -64.7 , -56.1 , -52.8 and -48.2 dBc, respectively. There are some other spurs in the spectrum mainly caused by sigma-delta modulator and crystal signal interferer, and all of these spurs are smaller than the reference spur. The phase noise measurement results at 0.045/1.8/2.3 GHz are

presented in Fig. 14. The spot phase noises at 1 MHz offset, which are dominated by VCO performance, are -136 , -123.4 , -119.3 and -118.5 dBc/Hz respectively. The bandwidth is set to be 80–100 kHz. The integrated phase noise from 1 kHz to 10 MHz are 0.1° , 0.727° , 2.177° and 1.387° , which map RMS jitter of 6.182, 2.021, 3.36 and 1.675 ps separately. The spot phase at 10 kHz and 1 MHz offset and the integrated phase noise from 1 kHz to 10 MHz in the whole output range are plotted in Fig. 15, and are less than -84 dBc/Hz, -116 dBc/Hz and 2.209° respectively. The settling time is measured by oscilloscope and is 20 μ s at 900 MHz, as presented in Fig. 16. The PLL specifications of some widely used wireless standards and protocols are presented in Table 1. The proposed FS can provide the satisfied phase noise performance. However, as the output frequency is 0.045–2.3 GHz, it cannot be employed for Bluetooth and 802.11 a/b/g/n applications. The comparison results with the state of the art FS is presented in Table 2. Compared with these works, the proposed synthesizer provides a good performance. Since the PLL loop utilizes only one VCO, the active area of synthesizer is 1.13 mm². The total capacitance of the LPF is 250 pF and the process provides the capacitance of 1 fF/

Table 1 PLL phase noise requirement in some typical wireless standards

Standards		Operating frequency (MHz)	Out-Band PN (dBc/Hz)
ZigBee	802.15.4	868 M/915 M	$-110@10$ M
Broad-casting	DVB-T/H	54–108/174–223/470–890	$-87@10$ kHz $-115@1$ MHz
Position	GPS	1227.6/1381.05/1575.42/1841.4	$-105@1$ MHz
RFID	UHF	860–960	$-82.8@10$ kHz $-122.8@1$ MHz
Bluetooth	802.15.1	2400–2483.5	$-81@1$ MHz
WLAN	802.11 a/b/g/n	2400–2483.5/5150–5350/5725–5850	$-102@1$ MHz

Table 2 Performance comparison with other state-of-the-art wideband analog frequency synthesizer

Ref	Process	Output frequency (GHz)	VCO core number	Power (mW)	Output type	In-band PN@10 kHz (dBc/Hz)	Out-band PN@1 MHz (dBc/Hz)	Active area (mm ²)
[12]	0.5 μ m BiCMOS	1.15–1.75	1	54.6	None	-80.1 (LO 1.4037G)	-130 (LO 1.4037G)	4.56 ^a
[4]	0.13 μ m CMOS	1.8–6	2	35.6–56.62	Quad.	-92 (LO 1.87G)	-125 (LO 1.87G)	1.86 ^a
[3]	0.18 μ m BiCMOS	0.125–32	4	284–498	Diff.	-95 (LO 1500 M)	-131 (LO 1500 M)	4.41 ^b
[13]	0.18 μ m CMOS	3.43–7.92	2	48	None	-78 (LO 4488 M)	-103 (LO 4488 M)	1.43 ^b
[5]	0.18 μ m CMOS	0.05–4.8	2	94	None	-98 (LO 1.5G)	-127 (LO 1.5G)	1.9 ^c
[11]	0.13 μ m CMOS	0.05–10	2	33–83	Quad.	-91 (LO 2G)	-128 (LO 2G)	3 ^a
		19–22						
		38–44						
This work	0.18 μ m CMOS	0.045–2.3	1	54	Quad.	-87 (LO 1.8G)	-119.3 (LO 1.8G)	1.13 ^b

^aWith on-chip loop filter

^bWithout on chip loop filter

^cExclude a conventional VCO and the band-selecting filters

μm^2 . If the LPF is integrated on chip, the active area of the FS is 1.43 mm^2 considering some margin. Nevertheless, it is the smallest among these works. The measurement results validate that the designed FS has great potential for SDR applications.

6 Conclusions

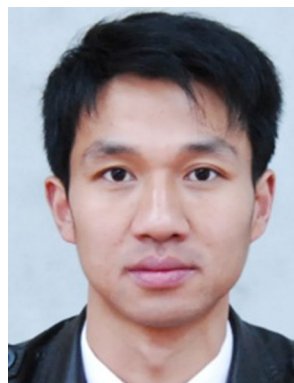
A wideband fractional-N sigma-delta frequency synthesizer is presented in this paper. In order to reduce the FS area, one wideband VCO with an optimized inductor is employed. The proposed FS provides 0.045- to 2.3-GHz quadrature outputs with an active area of 1.13 mm^2 . The in-band and out-band phase noise at 10 kHz and 1 MHz offset are less than -84 and -116 dBc/Hz respectively. The measurement results validate that this FS possesses great potential for software defined radios applications.

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