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MIXED SIGNAL LETTER

A novel split capacitor array switching scheme with proportional coefficient for SAR ADC

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Abstract
A novel switching scheme with proportional coefficient for successive approximation register analog-to-digital converter is presented in this work. The proposed switching scheme realize proportional coefficient by means of charge-sharing, which can achieve a high energy efficiency. Due to the split capacitor array structure is adopted here, the total capacitance can be reduced by 96.9% over the conventional structure. Moreover, the bridge capacitor is the unit capacitor, which is very convenient for layout design and capacitance matching. Furthermore, the proposed switching scheme reduces the energy by 99.9% compared with the conventional architecture through using the MSB-split switching structure and the single-side method. The proposed switching scheme also has a good performance in reset energy consumption and linearity. Based on the MATLAB simulation results, the maximum differential nonlinearity and maximum integral nonlinearity results of the proposed switching scheme are 0.626 LSB and 0.727 LSB, respectively.

Keywords SAR ADC · Split capacitor array · Proportional coefficient · Energy-efficiency · Area-saving

1 Introduction

Because of the low energy consumption required in the fields of wireless sensor, biomedical medical equipment and wearable electronic devices, successive approximate register (SAR) analogue-to-digital converters (ADCs) are having been widely used. Generally speaking, the power consumption of SAR ADCs mainly comes from digital control circuit, comparator and switching energy. And based on many published literatures, the digital-to-analogue converter capacitor arrays occupy a major part in the total power consumption of SAR ADCs. Thus, many switching methods [1–11] have been presented to reduce the switching energy consumption. The set and down switching technique [1] achieves an 81.26% reduction in switching energy when compared to the conventional switching scheme. The switching scheme reported in Ref. [2], the V_{CM}-based monotonic scheme (VMS) in Ref. [3] and the switching scheme introduced in Refs. [4–6] reduce the switching energy by 93.7, 97.66, 98.05, 98.40 and 99.75%, respectively. The recently related switching scheme [7] save 99.8% of the switching energy compared to the conventional scheme. However, the bridge capacitor is not the unit capacitor or the integer multiple of the unit capacitor. It raises a huge challenge to layout design and capacitance matching [8]. The proposed switching scheme save 99.9% of the switching energy and the bridge capacitor is the unit capacitor, whereas it distinguishing from the previously having proposed switching scheme. Furthermore, the proposed switching scheme not only reduces the number of capacitors by 96.9% compared with the conventional architecture, but also requires no reset energy.

2 SAR switching scheme

The overall structure of the proposed switching scheme for a 10-bit SAR ADC is shown in Fig. 1. The spilt capacitor array which the bridge capacitor is the integer value capacitor is adopted in the proposed switching scheme. The positive voltage potential side is composed of two

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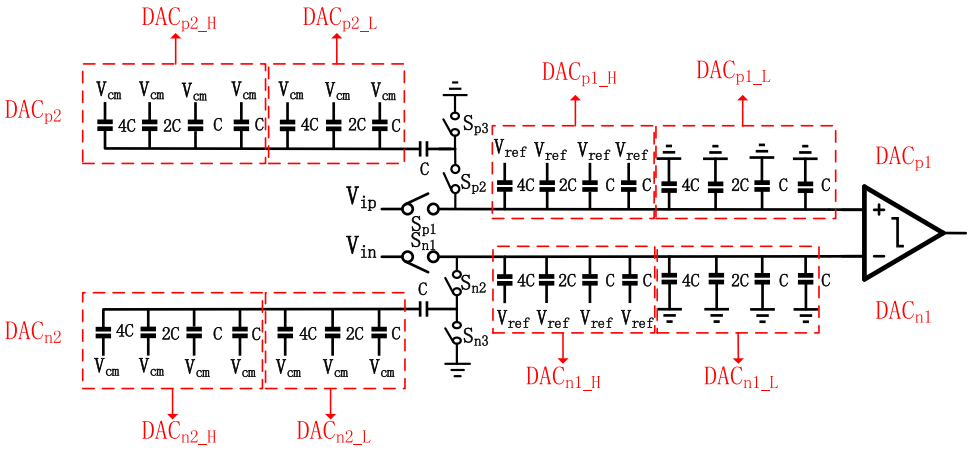

Fig. 1 The illustration of the proposed 10-bit SAR ADC

capacitor arrays: DAC_{p1} and DAC_{p2}. And the the most-significant bit (MSB) capacitor splitting technology is applied in both DAC_{p1} and DAC_{p2}, so as to enhance the power efficiency. And the totally symmetric capacitor array structure is applied in order to improve the linearity. In the second comparison cycle, whether is $V_{ip} > V_{in}$ or $V_{ip} < V_{in}$, the voltage change is completed in the positive voltage potential side. In the other comparison cycles, the voltage change is all completed in the negative voltage potential side. The monotonic switching method is used to reduce energy consumption to a large extent.

During the sampling phase, the switches $S_{p1}(S_{n1})$ and $S_{p3}(S_{n3})$ keep the connection, the switches S_{p2} and S_{n2} are off. Then the top plates of DAC_{p1} and DAC_{n1} complete sampling of differential inputs and the bottom plates of DAC_{p1} and DAC_{n1} are initially loaded as shown in Fig. 1. The voltage at the bottom of $DAC_{p2}(DAC_{n2})$ is fixed at V_{cm}, and the unit capacitor (C) is connected to gnd. The purpose of using top-plate sampling what has been used in many switching scheme is to ensure no energy consumption during the first comparison. Next the switches S_{p1} and S_{n1} open and the MSB is directly quantized. In the second comparison cycle, according to the monotonous change principle, all capacitors in DAC_{n1-H} are set to gnd or in DAC_{n1-L} are set to V_{ref}. At the same time, the switches $S_{p2}(S_{n2})$ from turn off to turn on and the switches $S_{p3}(S_{n3})$ break, so as to complete the redistribution of the charge to generate the fine bits. The situation of $V_{ip} > V_{in}$ is shown in Fig. 2. And the expressions (1) and (2) give a concrete

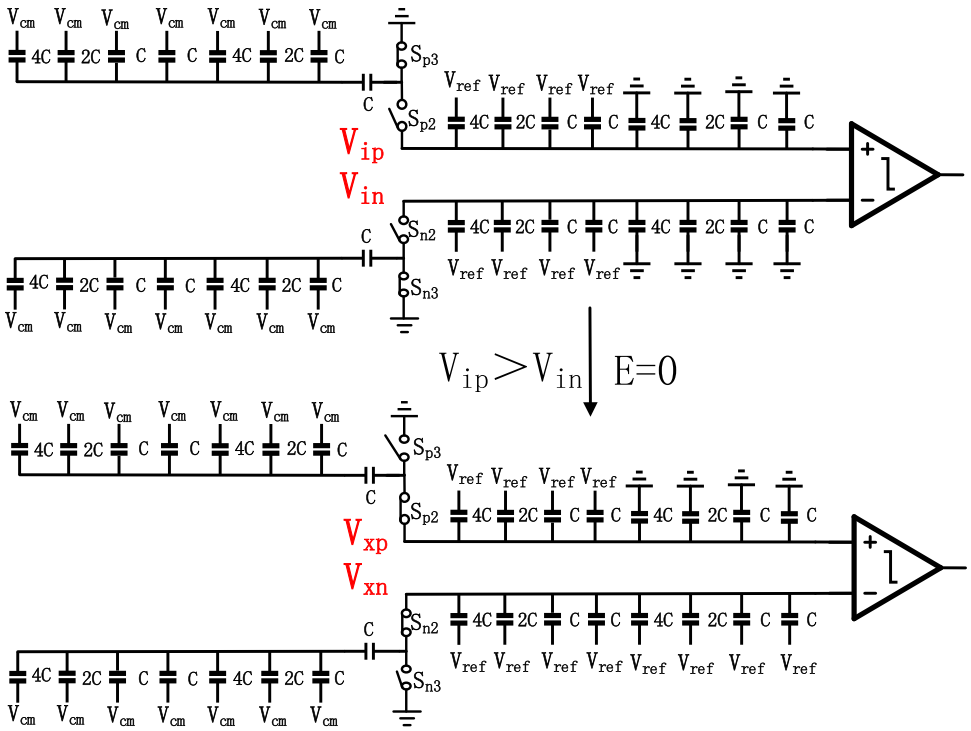

Fig. 2 The illustration of the redistribution of the charge

analysis. V_{xn} and V_{xp} is the voltages after the charge complete the redistribution.

$$\begin{aligned} &8C(V_{ip}-V_{ref})+8C(V_{ip}-gnd)+\frac{15}{16}C(gnd-V_{cm}) \\ &\quad=8C(V_{xp}-V_{ref})+8C(V_{xp}-gnd)+\frac{15}{16}C(V_{xp}-V_{cm}) \\ &V_{xp}=K\times V_{ip} \\ &K=\frac{256}{271} \end{aligned} \tag{1}$$

$$\begin{aligned} &16C(V_{in}+V_{cm}-V_{ref})+\frac{15}{16}C(gnd-V_{cm}) \\ &\quad=16C(V_{xn}-V_{ref})+\frac{15}{16}C(V_{xn}-V_{cm}) \\ &V_{xn}=K\times(V_{in}+V_{cm}) \\ &K=\frac{256}{271} \end{aligned} \tag{2}$$

As shown in expressions (1) and (2), V_{xp} (V_{xn}) is proportional to V_{ip} (V_{in}), and the scale factor is $K=\frac{256}{271}$.

Then the second MSB is generated. If $V_{xp1} > V_{xn1}$, all the capacitors in DAC_{p1-H} are set to V_{cm}. If $V_{xp1} < V_{xn1}$, all the capacitors in DAC_{p1-L} are set to V_{cm}. The situation of b2 = 1 is shown in the Fig. 3. The voltage change is shown in the following expression (3). The next three comparison cycles obey the same operation.

$$\begin{aligned} &\Delta V_{xp}=\frac{8CV_{cm}}{C_{p1}+(C//C_{p2})} \\ &\Delta V_{xp}=\frac{256}{271}\times\frac{1}{2^2}V_{ref} \\ &\Delta V_{xp}=K\times\frac{1}{2^2}V_{ref} \end{aligned} \tag{3}$$

After the upper five bits are all determined, the determination of the lower five bit codes are performed. Next the b6 is generated. If b6 = 1, all the capacitors in DAC_{p2-H} are set to gnd. Otherwise, all the capacitors in DAC_{p1-H} are set to V_{ref}. The situation of b6 = 1 is displayed in the Fig. 4. The voltage change is expressed in the following expression (4). The decision of the remaining bits obeys the same operation during the switching procedure.

$$\begin{aligned} &\Delta V_{yp}=\frac{8CV_{cm}}{C_{p2}+(C//C_{p1})} \\ &\Delta V_{xp}=\Delta V_{yp}\times\frac{C}{C+C_{p1}} \\ &\Delta V_{xp}=\frac{4}{271}V_{ref} \\ &\Delta V_{xp}=\frac{256}{271}\times\frac{1}{2^6}V_{ref} \\ &\Delta V_{xp}=K\times\frac{1}{2^6}V_{ref} \end{aligned} \tag{4}$$

Figure 5 depicts the switching procedure for a 6-bit SAR ADC as an example in order to simplify the analysis. Resulting from the symmetric DAC structure, the switching scheme of MSB = 1and the second MSB = 1 is analogous to the counterpart of MSB = 0 and the second MSB = 0, respectively. Thus, the situation of MSB = 1 and the second MSB = 1 is only introduced. The waveform of novel proposed switching scheme is shown in Fig. 6.

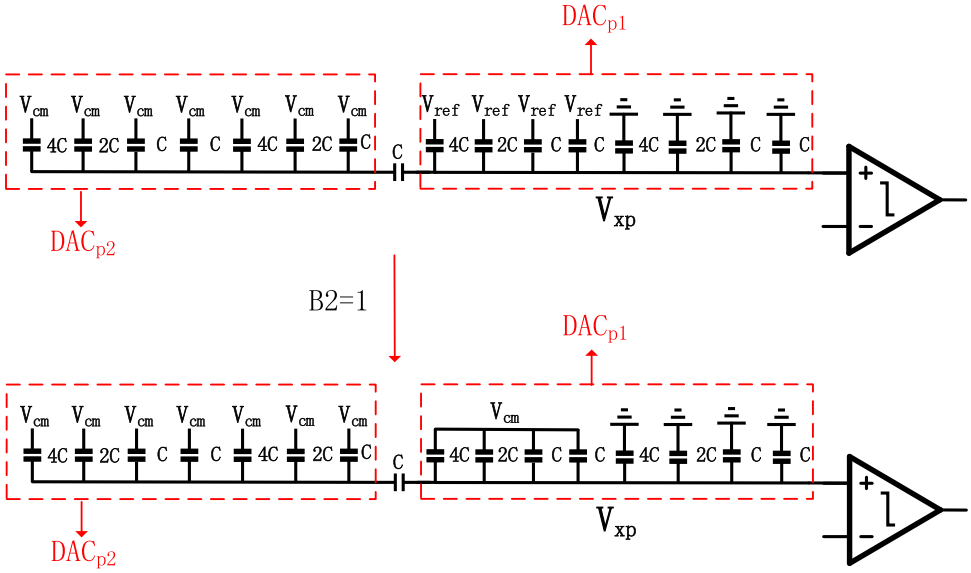

Fig. 3 The illustration of proposed switching scheme to achieve the second MSB bit

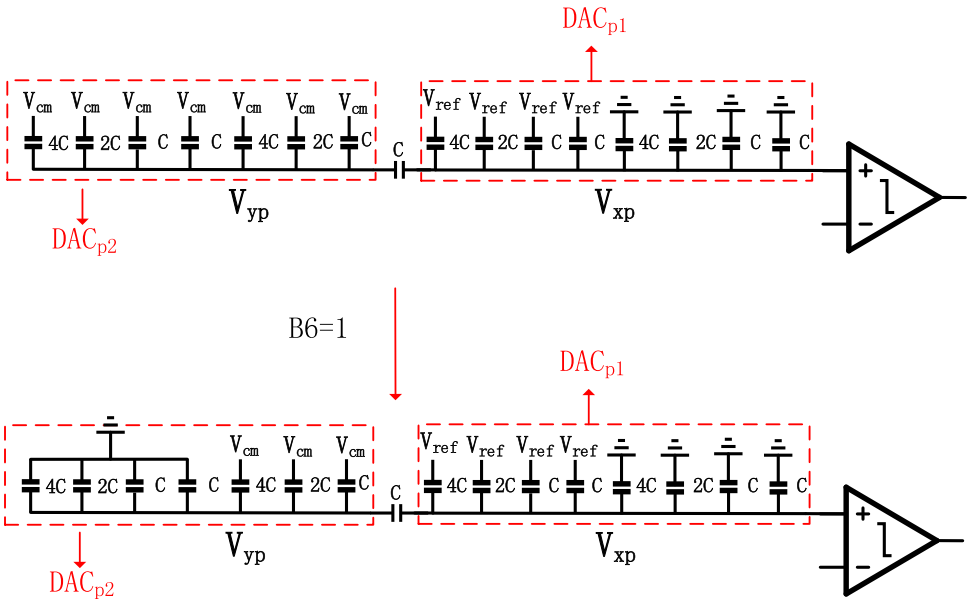

Fig. 4 The illustration of proposed switching scheme to achieve b6

3 Logic complexity

In the proposed switching scheme, apart from the first cycle voltage change is achieved by the DAC_{n1} capacitor array, the remaining comparison cycle voltage changes are completed by the DAC_{p1} capacitor array or the DAC_{p2} capacitor array. All the cycles are single-side change. Moreover, the decision of MSB is independent. The settlement of b3, b4, b5 is closely concerned to b2 and of the fine bits are related to b6. So logic complexity of the proposed switching scheme is acceptable.

4 Analysis of energy consumption

4.1 Switching energy analysis

The proposed switching scheme reduces the power consumption by using the MSB-split switching technology and the single-side method. And in order to minimize power consumption, using top-plate sampling and completing the redistribution of the charge after the first comparison cycle to ensure no energy consumption during the first two comparison cycles. From the behavioural simulation that was performed in MATLAB, Fig. 7 shows the results of switching energy against output codes of the 10-bit proposed switching scheme and the switching schemes reported in Refs. [2, 3, 4]. As shown in Fig. 7, the average energy of the proposed switching scheme is small relative to the other mentioned switching schemes and is only $1.3CV^2_{ref}$, which achieve a 99.9% reduction compared to the conventional 10-bit SAR ADC which the average energy consumption is 1363.3 CV^2_{ref}. What's more, Table 1 summarises some main features of the proposed switching scheme and the previously published switching schemes.

4.2 Reset energy analysis

The reset energy is consumed to make the capacitor array restore to the initial state between two sampling periods. As a result, the reset energy should be considered for the switching scheme. However, the previous reset method should be improved to fit the new proposed technology. According to the proposed two-step rest method in [9], for the proposed switching scheme, just needing to add a switch $S_{p4}(S_{n4})$ between DAC_{p1_H} (DAC_{n1_H}) and DAC_{p1_L} (DAC_{n1_L}). Then capacitor array on each side is separated into three groups through using the switch. When the last bit cycle is completed, the switches S_{p2}, S_{p4}, S_{n2} and S_{n4} turn off, the switches S_{p3} and S_{n3} turn on. At the same time, all the capacitors reset to the initial voltages. Then sampling switches S_{p1}, S_{n1} and so on turn on and DAC_{p1-H} (DAC_{n1-H}) and DAC_{p1-L} (DAC_{n1-L}) sample the input signal, respectively. And DAC_{p2} and DAC_{n2} reconnect to V_{cm}. Next the sampling switches turn off, the switches S_{p4} and S_{n4} turn on to operate the next cycle. To simplify the analysis of the reset procedure, Fig. 8 is as an example to explain. It can be concluded that the reset energy is zero.

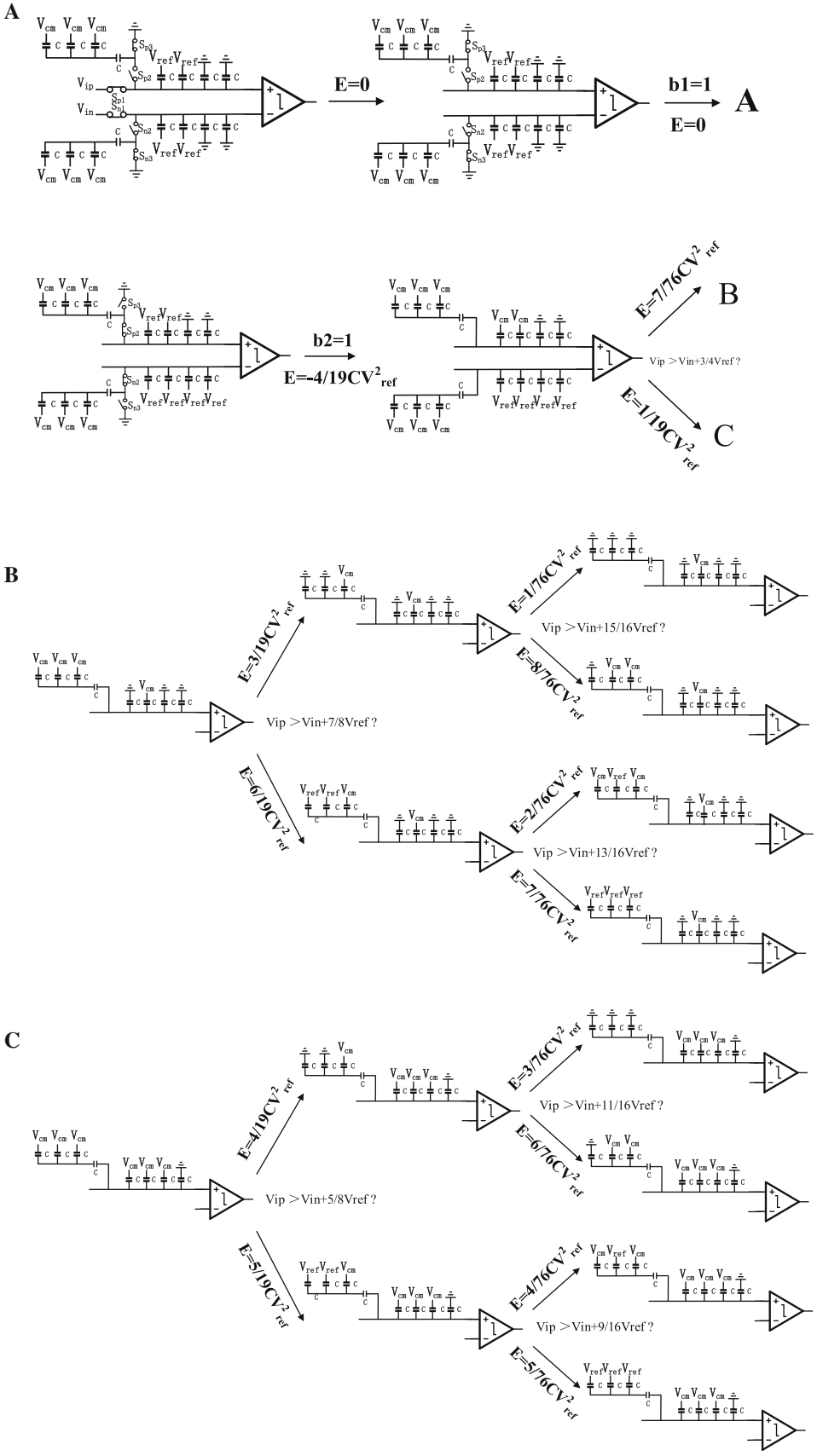

Fig. 5 The proposed switching scheme of 6-bit SAR

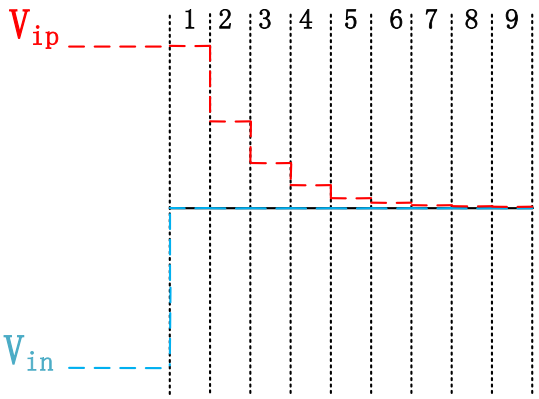

Fig. 6 Waveform of the proposed switching technique

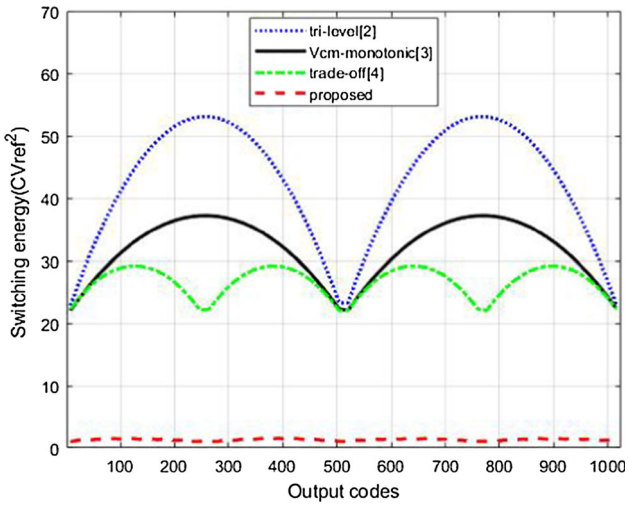

Fig. 7 Switching energy against output codes

5 Analysis of linearity

5.1 DNL and INL

As known the linearity of SAR ADC is important, and the linearity is related to the number of capacitor and the deviation of matching [10]. As the number of capacitors decreases, switching energy consumption reduces. However, there is no doubt that the linearity would be deteriorated. In the following, the linearity of the proposed switching scheme will be discussed. Each capacitor in the DAC is the sum of the nominal capacitor value and the mismatch value. The simulation results of 500 Monte Carlo runs of 10 bit SAR ADC with proposed switching scheme is shown in Fig. 9, with the deviation of the unit capacitor valuing $\sigma_u = 0.01$ C. Because of using of the single-side method, the worst case DNL and INL occur at $1/2V_{ref}$ and $1V_{ref}$, where the root-mean-square (RMS) of maximum DNL and the root-mean-square RMS of maximum INL are 0.627 LSB and 0.727 LSB, respectively. According to the method introduced in [3], the standard deviation of the maximum DNL is expressed in (5).

$$\begin{aligned} DNL_{\max} &= \sqrt{\frac{(2^{N-6}-1)\delta_u^2 \times \left(\frac{16}{271}V_{ref}\right)^2 + (2^{N-6}-1)\delta_u^2 \times \left(\frac{1}{271}V_{ref}\right)^2}{(2^{N-5})^2 \times C_u^2}} \\ &= \sqrt{\frac{(2^{N-6})\delta_u^2}{(2^{N-5})^2 \times C_u^2} \times \left(\frac{16}{271}\right)^2 \times (2^N)^2} \times LSB \\ &\approx \frac{16}{271}\frac{\sqrt{2^{n+4}} \times \delta_u}{C_u} \times LSB \end{aligned} \tag{5}$$

5.2 Parasitic capacitor influence analysis

As shown in Fig. 10, there are two main types of parasitic capacitor, parasitic capacitances of the bottom plate (C_{pb}) and parasitic capacitances of the top plate (C_{pt}) [6]. Figure 10(a) illustrates the parasitic capacitances of n side in the first comparison cycle, and Fig. 10(b) illustrates the parasitic capacitances of p side in the sixth comparison cycle. As shown in Fig. 10(a), we can get in the first comparison cycle, the effect of parasitic capacitance on the ADC is similar to Refs. [6, 11], that is, the C_{pb} capacitors do not have direct influence on the linearity of

Table 1 Comparison of switching scheme for a 10-bit SAR ADC

Switching schemes	Average switching energy (CV_{ref}^2)	Energy savings	Area reductions	Bridge capacitor (Cu)	Reset energy (CV_{ref}^2)
Conventional	1363.3	Reference	Reference	No	0
Set and down [1]	255.5	81.26%	50%	No	0
Tri-level [2]	84.9	93.70%	75%	No	0
VMS [3]	31.88	97.66%	75%	No	105.4
Trade-off [4]	26.54	98.05%	75%	No	0
Sanyal and Sun [5]	21.3	98.40%	75%	No	95.75
Two step [6]	3.44	99.75%	85.9%	No	0
Area reduction [7]	2.8	99.8%	97.4%	1.14	0
This work	1.3	99.9%	96.9%	1	0

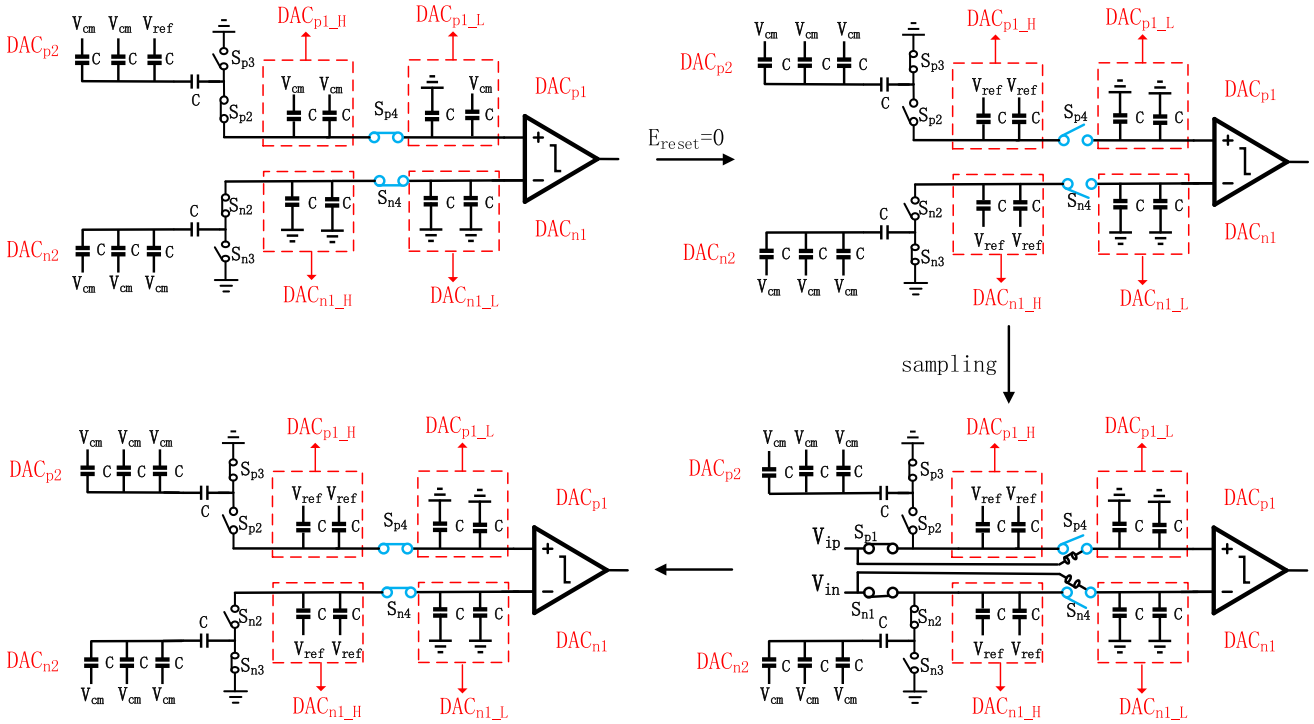

Fig. 8 Reset method applied to switching technique

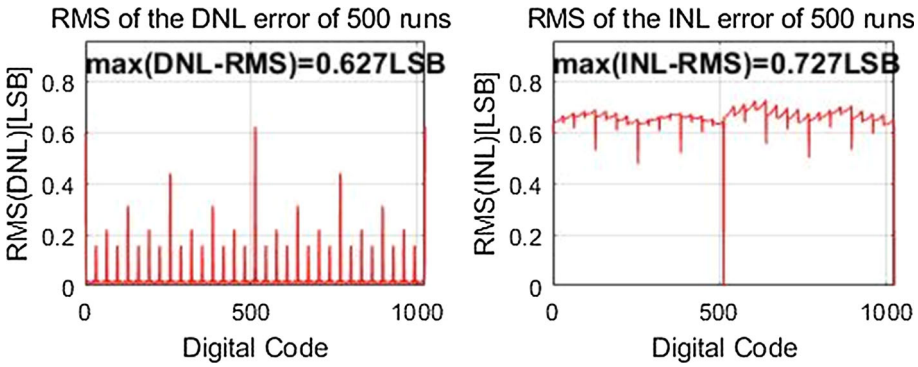

Fig. 9 The standard deviation of DNL and INL versus output codes

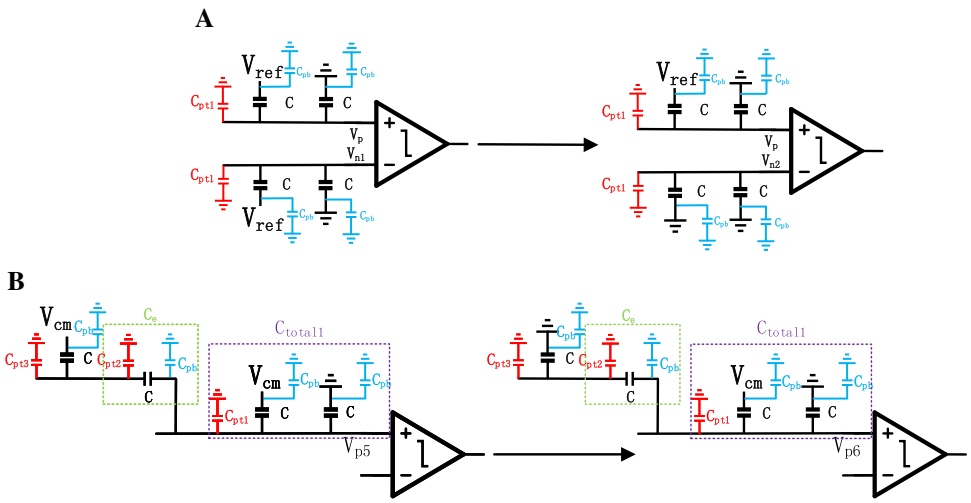

Fig. 10 **a** The parasitic capacitor in the first comparison cycle, **b** the parasitic capacitor in the sixth comparison cycle

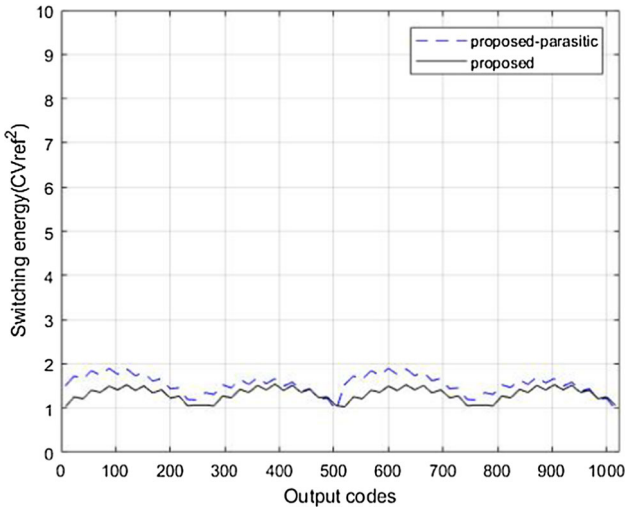

Fig. 11 Switching energy comparison for 10-bit SAR ADC with parasitic capacitors (C_{pt} = 0.1 Ctotal, C_{pb} = 0.15 Cu)

the DAC, C_{pt} and C_{pb} raise the power consumption. As for Fig. 10(b), we can get the voltage variation in V_p:

$$V_{p6} - V_{p5} = \frac{(0 - V_{cm}) \times (C + C_{pb})}{(C + C_{pb}) + C_{pt3} + (C_e // C_{total1})} \tag{6}$$

The difference is that the C_{pt} and C_{pb} affect the linearity and increase energy consumption in this situation. Energy consumption is increased from 1.3 CV_{ref}^2 to 1.54 CV_{ref}^2 as shown in Fig. 11.

6 Conclusion

A high energy-efficiency and area-saving split capacitor array switching scheme which the bridge capacitor is the unit capacitor for the SAR ADC is presented. By means of split capacitor array structure, MSB-split method and monotonic switching technology, the proposed switching procedure not only achieves 99.9% energy saving, but also reduces the number of capacitors by 96.9% compared with the conventional architecture. Moreover, the two-step reset method is used to ensure that the reset energy consumption is zero. The DNL and INL of the proposed switching method are 0.627 LSB and 0.727 LSB, which can be improved by the calibration technique. The proposed switch scheme has a good overall performance for the SAR ADC.

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