Analog Integrated Circuits and Signal Processing (2019) 98:321–329
https://doi.org/10.1007/s10470-018-1369-0

A CMOS PFM buck converter employing a digitally programmable voltage level-shifting technique

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Received: 4 June 2018 / Revised: 5 October 2018 / Accepted: 15 November 2018 / Published online: 10 December 2018

Abstract
This paper describes a CMOS pulse frequency modulation (PFM) buck converter employing a digitally programmable voltage level-shifting technique capable of adjusting peak inductor current and output ripple voltage for different load currents. The conventional PFM buck converters employ either an adaptive delay time control circuit or a fixed delay time control circuit to control output ripple voltage and power efficiency with the switching frequency. However, they suffer from a large peak inductor current, resulting in reduced power efficiency. The digitally programmable voltage level-shifting circuit, based on a common source amplifier, is capable of sensing inductor current through the voltage drop caused by on-resistance of the power switch, and can control peak inductor current. The precision needed to control the magnitude of the peak inductor current can be obtained with the number of bits in the digitally programmable voltage level-shifting circuit that are dependent on the input common mode range of the comparator. Employment of one comparator with pre-control logic and post-control logic circuits allows the proposed circuit to improve power efficiency by removing additional circuits, compared with the conventional PFM buck converters. The proposed converter was implemented with a 180 nm CMOS process. The effective chip size of the core block occupies 900μm × 590μm. The proposed PFM mode buck converter with a precision of four bits to control peak inductor current is capable of accommodating an input voltage range of 2.7–3.3 V, and can produce output voltage of 1.2 V. The operational switching frequency measured is on the order of several to several hundred kHz, the load current range is under 150 mA, and the measured output ripple voltage varied, depending on the digital programming status. The measured power efficiency ranged between 70 and 84%.

Keywords PFM buck converter · Digitally programmable · Voltage level-shifting · Peak inductor current · CMOS

1 Introduction

With the rapid advancement of CMOS technology, circuit performance has drastically improved and power consumption has been reduced owing to the development of circuit design techniques and reductions in power supply voltage. This has allowed portable devices (smart phones, tablets, wearable devices, and IoT devices) to come to market [1, 2]. Most of these portable devices utilize battery resources, so power management integrated circuits (PMICs) are employed that are capable of managing energy in battery resources with efficiency. It is well known in PMICs that PFM buck converters perform at higher efficiency under low load–current conditions than pulse width modulation (PWM) buck converters [3].

In order for a conventional PFM buck converter to control output ripple voltage and power efficiency with a switching frequency, it usually employs either an adaptive delay time control circuit [4] or a fixed delay time control circuit [5, 6]. PFM buck converters with a fixed delay time control circuit produce peak inductor current in proportion to input voltage. As the input voltage becomes high, an over-current may occur due to the steep slope of the inductor current. On the other hand, as input voltage becomes low, the slope of the inductor current stays low,

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which results in a narrow operational range for the load current. An adaptive delay time control circuit enables PFM buck converters to control the on-time of the p-channel power switch. This circuit technique is able to eliminate the disadvantage of the fixed delay time control circuit—dependence of the peak inductor current on input voltage. However, the adaptive delay time control circuit still suffers from producing large peak inductor current and requiring additional circuitry to improve the accuracy of controlling the inductor peak current, which results in a reduction in power efficiency.

In order to overcome the disadvantages of the conventional delay time control circuit techniques, a current mode PFM buck converter employs a technique to restrict the inductor current to a predetermined peak inductor current [7]. This technique directly detects the inductor current through the sensing circuit and converts it to a voltage through the V-I converter to sense the peak inductor current. The current mode technique takes advantage of controlling the peak inductor current with higher accuracy than the delay time control circuit techniques. However, since this technique requires employment of additional circuits such as inductor current sensing circuit and V-I converter, the power consumption of the control circuit may be increased. A digitally programmable voltage level-shifting technique is proposed to control peak inductor current with the switching frequency, and consequently, the output ripple voltage of the PFM buck converter. In addition, the proposed technique employs a simpler circuit structure than the other techniques [4–7] by sensing the inductor current through the level shifting circuit consisting of only six MOSFET devices. This paper is organized as follows. The proposed architecture and the digitally programmable voltage level-shifting technique are described in Section II. Measurement results of the proposed circuit are discussed in Sect. 3. Conclusions are drawn in Sect. 4.

2 The proposed architecture

An overall block diagram of the proposed architecture is in Fig. 1. It consists of the on-chip circuit within the dotted line and the off-chip circuit. The on-chip circuit includes power switches with gate drivers, a dead-time control circuit, a comparator, pre-control logic, post-control logic, a digitally programmable voltage level shifter, bandgap reference, and azero current detection (ZCD) circuit. The inductor, an output capacitor, a resistive feedback network, and the load are enclosed in the off-chip circuit.

When the p-channel power switch turns on in the steady state, the inductor current flowing through the p-channel power switch increases with a slope of $(V_{in} - V_{out})/L$, where V_{in}, V_{out}, and L are input voltage, output voltage, and inductance, respectively. V_{LX} on the LX node shows the voltage waveform slightly lower than V_{in} due to the voltage drop across the on-resistance of the p-channel power switch. Hence, this voltage waveform can be utilized to detect the peak inductor current. However, the voltage drop across the on-resistance (on the order of a few hundred milli-ohms) of the p-channel power switch is not significant, and it may not be within the input common mode range (ICMR) of the comparator, since it starts from V_{in}. Therefore, it requires a voltage level-shifting circuit to bring V_{LX} into the ICMR of the comparator. The magnitude of V_{LX} can be lowered by a certain level of voltage through the voltage level–shifting circuit, but the shape of the voltage waveform for V_{LX} remains unchanged. $V_{SF,amp}$ is the level-shifting voltage on the LX node and is compared with the digitally programmable $V_{LS,amp}$ made by V_{in} to determine the magnitude of the inductor current and output ripple voltage through pre-control logic and post-control logic circuits.

The schematic of the voltage level–shifting circuit to produce $V_{SF,amp}$ and $V_{LS,amp}$ is illustrated in Fig. 2. Since constant current I_{cons} flows through the transistor M_{N1}, level-shifting voltage V_{SF} can be obtained as follows:

$$V_{SF} = V_{LX} - V_{GS,M_{N1}} \tag{1}$$

$$V_{GS,M_{N1}} = \sqrt{\frac{2I_{cons}}{K_n S_1}} + V_{th} \tag{2}$$

$$V_{LX} = V_{in} - I_L R_{p,on} \tag{3}$$

where K_n, V_{th}, S_1, I_L, and $R_{p,on}$ are n-channel device transconductance parameter, threshold voltage, device aspect ratio (W/L) of M_{N1}, inductor current, and on-resistance of the p-channel switch, respectively.

Transistor M_{P1} and resistor R serve as driver and load of the common source amplifier to amplify the small signal variation in V_{LX} so that it may prevent the comparator from malfunctioning due to the small variation of V_{in}, I_L, and V_{LX}. The large voltage gain of the common source amplifier should be able to enhance the sensitivity of the voltage-level shifting circuit with respect to the variation of V_{LX} and I_L. However, the voltage gain should be carefully designed so that the driver, M_{P1}, should always be in the saturation region, and $V_{SF,amp}$ should be in the ICMR of the comparator. In a similar manner, the level-shifting voltages, V_{LS} and $V_{LS,amp}$ are generated as seen in Fig. 2(b). Since two circuits shown in Fig. 2 are implemented with the identical circuit structure, the voltage difference between V_{GS2} and V_{GS1}, namely $V_{d0} = V_{GS2} - V_{GS1}$, should be independent of variation in the process, supply voltage, and temperature. Transconductance(Gm) mismatch was minimized by utilizing the long channel length of 2um for both the transistors Mp1 and Mp2. Common

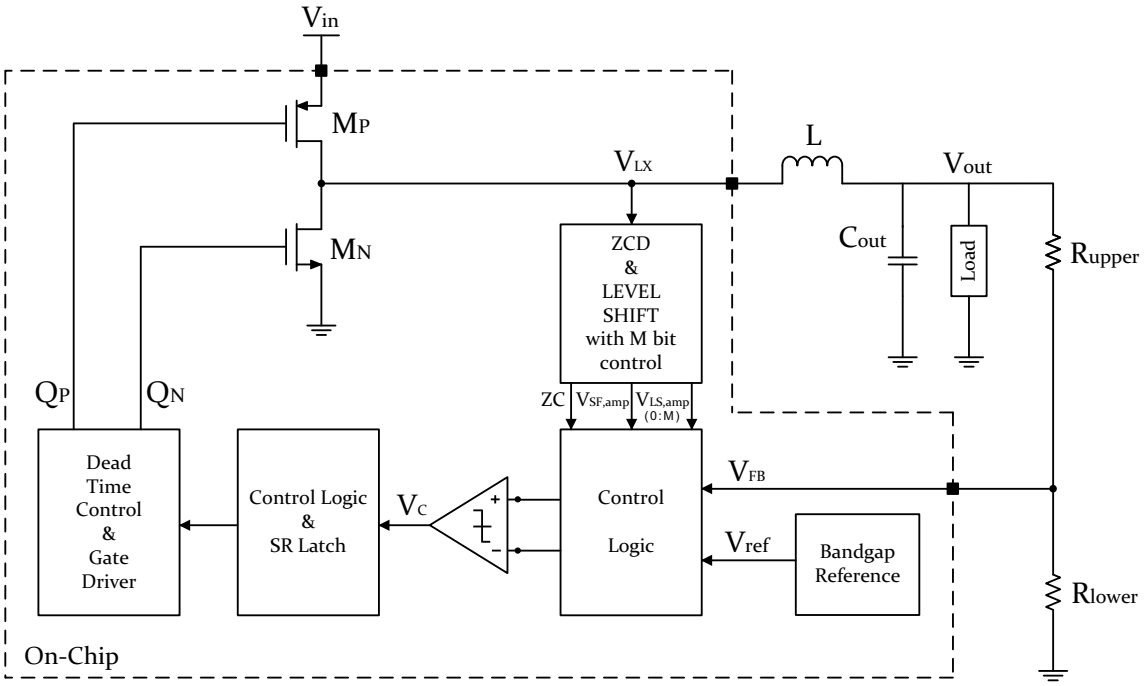

Fig. 1 The block diagram of the proposed PFM DC-DC buck converter

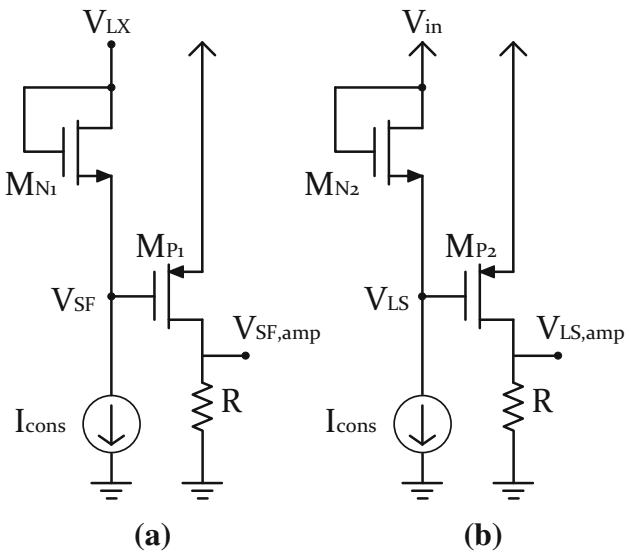

Fig. 2 Schematic of the voltage level–shifting circuit to generate **a** $\mathbf{V_{SF,amp}}$ and **b** $\mathbf{V_{LS,amp}}$

centroid layout technique was applied to minimize the mismatch on the resistor R. In this manner, the effect of device mismatches (Mp1, Mp2, and R) on the level shifting circuit was minimized. And the constant current I_{cons} of 10 μA is employed to obtain $V_{GS,M_{N1}}$ and $V_{GS,M_{N2}}$, so that device mismatch can be minimized.

The magnitude of the peak inductor current can be described by

$$I_{pk} = \frac{V_{d0}}{R_{p,on}} = \left(\frac{V_{in} - V_{out}}{L}\right) t_{p,on} \tag{4}$$

where I_{pk} and $t_{p,on}$ are the peak inductor current and the on-time of the p-channel power switch, respectively. It is well known that the conventional PFM mode buck converters suffer from requiring additional circuitries to detect the peak inductor current accurately [4]. Since V_{d0} and $R_{p,on}$ stay constant in (4), the peak inductor current, I_{pk}, remains constant regardless of variations in V_{in}. Therefore, it is necessary to adjust the amplitude of the peak inductor current, which should be detected by the PFM buck converter with a certain degree of sensitivity.

In order to adjust the magnitude of the peak inductor current, insertion of a digitally programmable voltage level-shifting resistor array is made between M_{N2} and the constant current source, as presented in Fig. 3.

The digitally programmable voltage level-shifting array contains a series of binary weighted resistor arrays associated with switches—b_0(LSB), b_1,…, $b_{M\text{-}1}$(MSB)—based on transmission gates. The magnitude of level-shifting voltage V_{array} is determined as follows:

$$V_{array} = \sum_{k=0}^{M-1} \bar{b}_k \cdot 2^k \cdot R \cdot I_{cons} \tag{5}$$

where M is the number of bits to be programmed by the user. The resultant gate voltage of M_{P2}, V_{LS}, is obtained as follows:

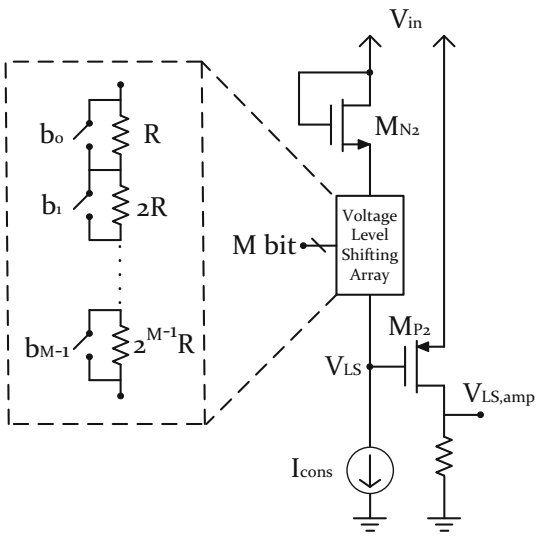

Fig. 3 Circuit diagram of the digitally programmable voltage level-shifting circuit

$$V_{LS} = V_{in} - V_{GS,MN2} - V_{array} \tag{6}$$

Since M_{P2} remains in the saturation region, the drain voltage of M_{P2}, $V_{LS,amp}$, can be assumed to be approximately the same as V_{LS}. A block diagram of the comparator with the switches (S_1, S_2, S_3) and the control logic circuit is in Fig. 4. The output voltage signal, V_C, of the comparator, and the output signal, $\bar{Q}$, of the third D flip-flop serve as the clock and clear signal for three D flip-flops in the control logic circuit, respectively.

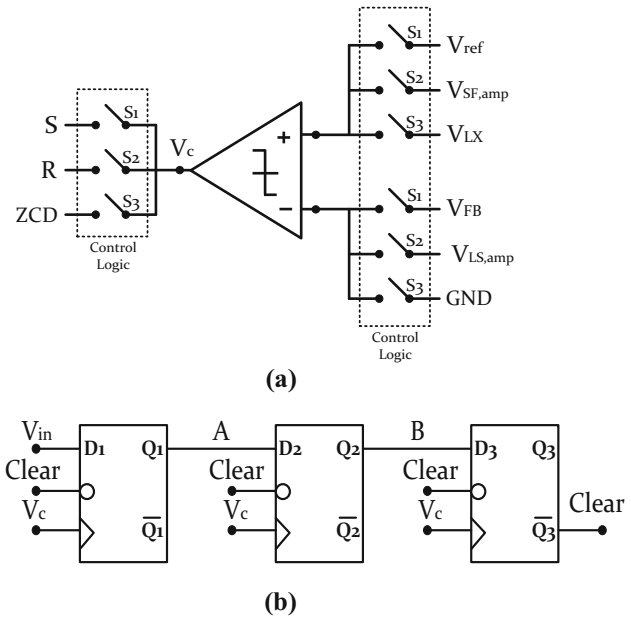

Fig. 4 Block diagram of **a** the comparator with the switches (S_1, S_2, S_3) and **b** the control logic circuit

The logic states (A, B) of the control logic circuit drive the logic circuit shown in Fig. 5 to determine the logic state of the three switches (S_1, S_2, S_3). The connections between the comparator and nine nodes are presented in Table 1.

A timing diagram of the eight signal waveforms associated with the comparator and the control logic circuit is in Fig. 6. It is assumed in the initial state that the logic state (A, B) of the control logic stays (0, 0), and it results in S_1 staying high, and S_2 and S_3 remaining low.

Hence, two input nodes and an output node of the comparator are connected to V_{ref}, V_{FB}, and the S node, respectively. If V_{ref} becomes greater than V_{FB}, clock signal V_C at time t_0 activates the first D flip-flop, logic state A becomes high, and it results in S_2 staying high and S_1 and S_3 remaining low. It drives the p-channel power switch to turn on, and inductor current I_L begins to increase until it reaches the peak current, which will be determined by the logic state of the digitally programmable voltage level–shifting circuit shown in Fig. 3. When $V_{SF,amp}$ reaches the point where it is greater than $V_{LS,amp}$ at time t_1, the clock signal activates the first and second flip-flops simultaneously. It results in the logic state of A and B staying high, S_3 staying high, and S_1 and S_2 remaining low. It makes the p-channel power switch turn off and the n-channel power turn on, which results in the inductor current decreasing until it reaches time t_2. As the comparator reaches time t_2, S_1 becomes high. This cycle is repeated over and over again. The time duration ($\Delta t = t_1 - t_0$) in which S_2 stays high determines the magnitude of the peak inductor current, as shown in Fig. 7. The longer the time duration, the larger the peak inductor current becomes. The magnitude of the peak inductor current (I_{pk}) in (5) is proportional to the time duration (Δt), and can be rewritten as

$$I_{pk} = \frac{V_{in} - V_{out}}{L}\Delta t = \frac{V_{in} - V_{out}}{L} \cdot \frac{V_{array} C_o}{I_{P2}} \tag{7}$$

where C_O and I_{P2} are the load capacitance and drain current of the p-channel device,M_{P2}, shown in Fig. 3.

Substituting (5) into (7), I_{pk} can be expressed as

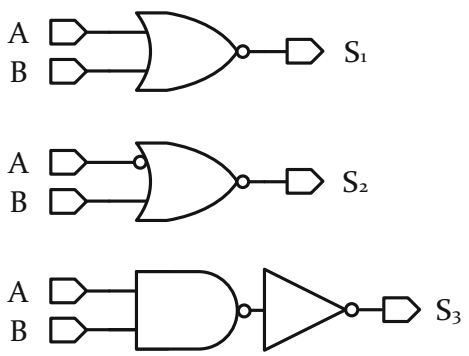

Fig. 5 Block diagram of the control logic circuit to determine the logic states of the three switches (S_1, S_2, S_3)

Table 1 Connections of the comparator with several signals through the three switches (S_1, S_2, S_3)

Comparator			A node	B node	Switch staying high
Input (+)	Input (−)	Output			
V_{ref}	V_{FB}	S	0	0	S_1
$V_{SF,amp}$	$V_{LS,amp}$	R	1	0	S_2
V_{LX}	GND	ZCD	1	1	S_3

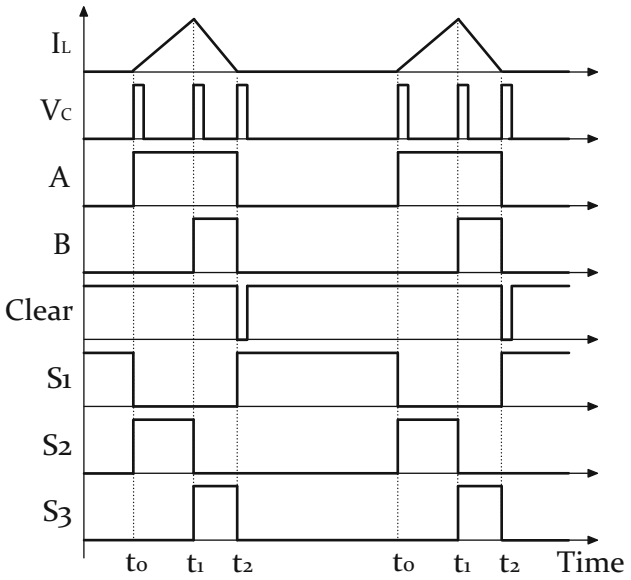

Fig. 6 Timing diagram of the eight signal waveforms associated with the comparator and the control logic circuit

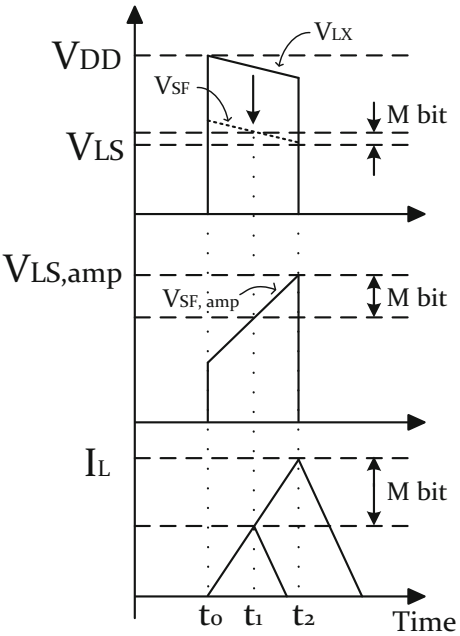

Fig. 7 The waveforms of V_{LX}, V_{SF}, $V_{SF,amp}$, V_{LS}, $V_{LS,amp}$, and I_L as a function of time with M bit control

$$I_{pk} = I_{pko} \cdot \sum_{k=0}^{M-1} \bar{b}_k \cdot 2^k \tag{8}$$

where $I_{pko} = \frac{V_{in}-V_{out}}{L} \frac{C_o \cdot I_{cons} \cdot R}{I_{P2}}$.

The peak inductor current normalized by I_{pko} determines the programmability of the proposed voltage level-shifting circuit with M bits. The maximum number of bits (M bit) of the digitally programmable voltage level–shifting circuit in Fig. 3 can be restricted by R, I_{cons}, and the ICMR of the comparator.

3 Measurement results

The proposed PFM buck converter was implemented with a 180 nm CMOS process. A microphotograph of the proposed circuit is in Fig. 8. It occupies 900μm × 590μm, excluding bonding pads, gate drivers, and power switches. The analog blocks, such as the band gap reference and the current bias circuit, are on the left-hand side of the photograph, such that they are isolated from the digital blocks. Placement of two power switches and two gate drivers is on the right-hand side of the chip layout. The control logic and comparator block were placed between analog blocks and power switches. Due to the ICMR of the comparator in the given process, the number of bits of the voltage level-shifting circuit in this implementation was chosen as 4.

Figure 9 demonstrated the corner simulated slew rate waveform of $V_{SF,amp}$ in the voltage level-shifting circuit.

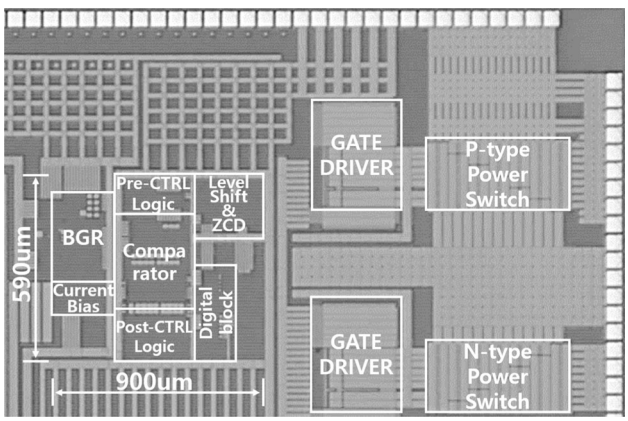

Fig. 8 Chip microphotograph of the proposed circuit

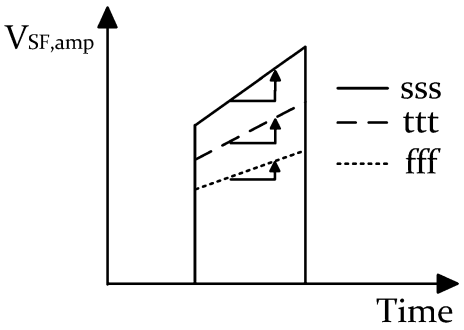

Fig. 9 The corner simulated slew rate waveform of $V_{SF,amp}$ in the voltage level-shifting amplifier

The slow case(sss), typical case(ttt), and fast case(fff) slew rates of $V_{SF,amp}$ are simulated to be 950 mV/μs, 809 mV/μs, and 620 mV/μs, respectively. The corner simulation result shows that the slew rate of $V_{SF,amp}$ is sufficient to be able to sense the inductor current.

The monte-carlo simulation on the level-shifting circuit, as shown in Fig. 10, was performed to investigate device mismatches due to process variation. Figure 10 demonstrated that the average voltage gain of the level shifting amplifier was 3.45 with standard deviation of the voltage gain as 0.01. Therefore the monte-carlo simulation confirmed the Gm mismatch of Mp1 and Mp2 as well as the mismatch on the resistor R was considered to be small due to process variation.

The number of bits for the digitally programmable voltage level-shifting circuit can be expanded to increase the accuracy in controlling the peak inductor current, depending on the ICMR of the comparator and the design of the common source amplifier. Two measurement results with a programing status of (0000) and (1111) are presented in Fig. 11(a), (b), respectively. Each measurement result with an input voltage of 3.0 V and a load current of 20 mA includes four waveforms (the output voltage of the proposed PFM buck converter, V_{out}, output voltage of the comparator, V_c, the load current, I_{load}, and the inductor

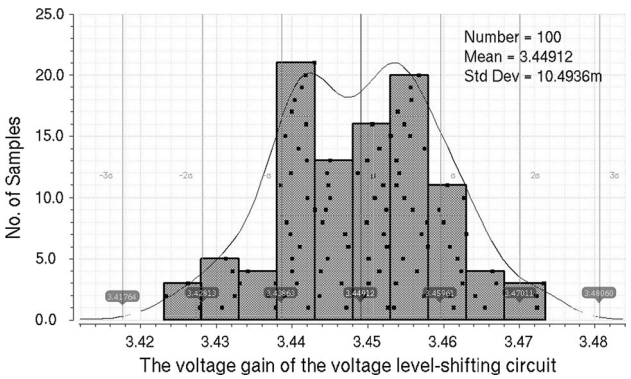

Fig. 10 The Monte-Carlo simulation of the voltage level-shifting circuit

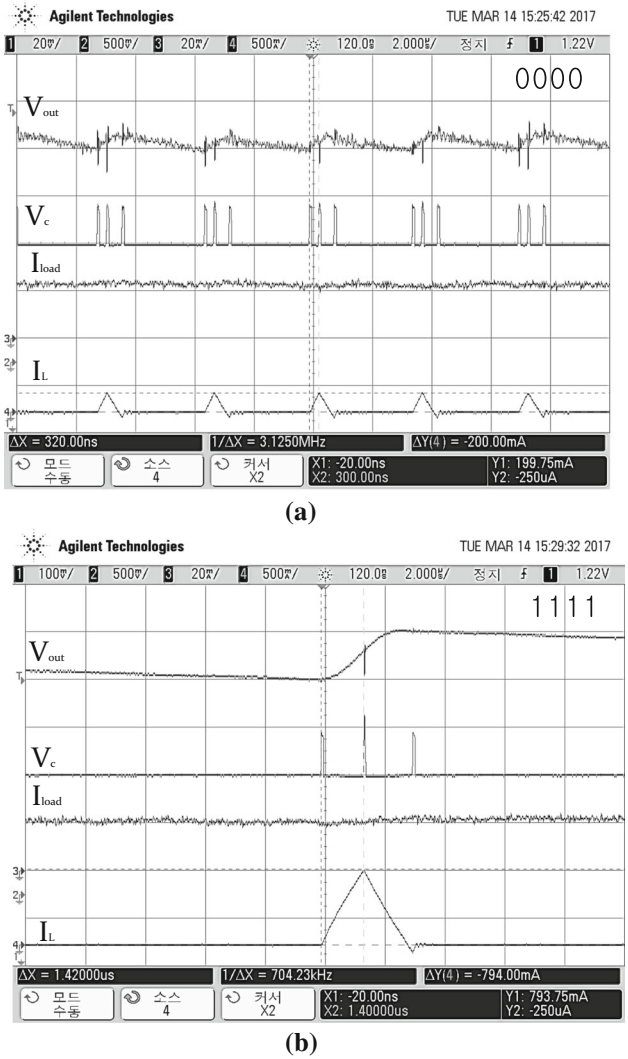

Fig. 11 Measured waveform of the output voltage of the proposed PFM buck converter, V_{out}, output voltage of the comparator, V_c, the load current, I_{load}, and the inductor current, I_L, with a programming status of **a** (0000) and **b** (1111)

current, I_L). The peak inductor current, the switching frequency, and the ripple output voltage with programming status (0000) in Fig. 11(a) were measured at 200 mA, 462 kHz, and 8.25 mV, respectively. The three pulse trains of V_c in Fig. 11(a) were proven to demonstrate the normal functionality of the comparator with control logic circuit, as shown in Fig. 6. It can be seen in Fig. 11(a) that the time interval between the first and second pulses determined the magnitude of the peak inductor current, 200 mA. In a similar manner, the appropriate functionality of the comparator with control logic circuit and logic status (1111), as presented in Fig. 11(b) can be explained. The peak inductor current, switching frequency, and ripple output voltage were measured at 802 mA, 18 kHz, and 104 mV, respectively. The ratio of time intervals with logic status (1111) between the first and second pulses with respect to

the period of the pulse train increased twice, compared to that with logic status (0000), as shown in Fig. 11(a), (b).

The switching frequency as a function of the digital programming code (0000–1111) with load currents of 10 mA and 20 mA was measured to decrease quadratically, and is presented in Fig. 12. The switching frequency with a load current of 20 mA was measured at approximately two times higher than with a load current of 10 mA.

The measured peak inductor current as a function of the digital programming code with load currents of 10 mA and 20 mA is shown in Fig. 13 to be almost linear, as expected in Eq. (8), within a tolerance of 10%. Nonlinearity of the peak inductor current as a function of the digital code comes from (1) the nonlinearity of the CS amplifier in the voltage level-shifting circuit, (2) resistance mismatches in the resistor array, and (3) the turn-on resistance of switches.

The power efficiency of the proposed PFM mode buck converter is measured with various load currents ranging from 1 to 150 mA, as presented in Fig. 14. The measured power efficiency starts with 70% at a low load current of 1 mA, increases up to 84% at a load current of 30 mA, and stays at an almost constant 82% at 150 mA.

A performance comparison of the proposed PFM buck converter was made against conventional converters and is shown in Table 2. The pulse skipping methodology of Yuan et al. [8] was adopted to reduce the switching frequency with output ripple voltage fixed at 10 mV, and to increase power efficiency at low-load current. However, since the basic architecture of Yuan et al. [8] is based upon driving the PWM mode, the power efficiency became lower than that of the general PFM circuit at a high load current. The adaptive technique on time, employed by Tsai et al. [9], allows the switching frequency to vary with the output ripple voltage fixed at 20 mV. The complexity of the circuit of Tsai et al. [9] leads to a large conduction loss and lower power efficiency. The proposed circuit employs the digitally programmable voltage level–shifting circuit to allow the peak inductor current, the switching frequency, and the output ripple voltage to be changed as a function of digital code for different load currents.

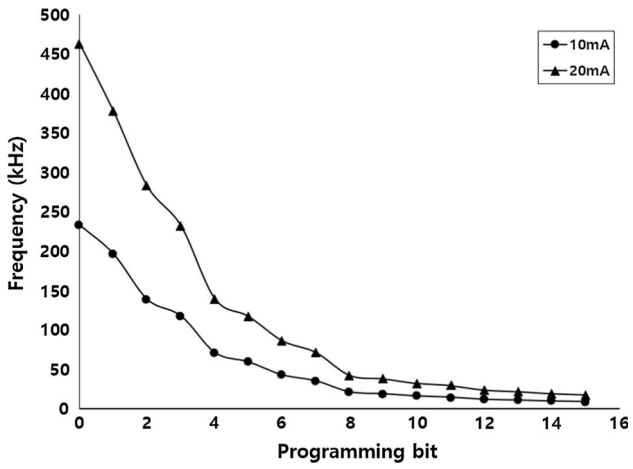

Fig. 12 The measured switching frequency as a function of the digital code in the voltage level-shifting circuit with load currents of 10 mA and 20 mA

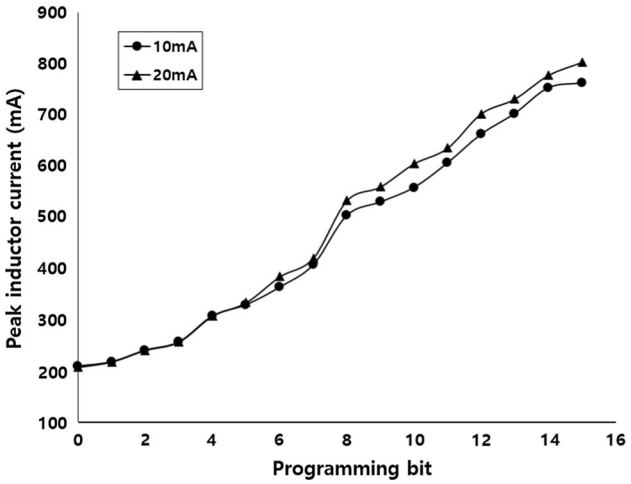

Fig. 13 The measured peak inductor current as a function of the digital code in the voltage level-shifting circuit with load currents of 10 mA and 20 mA

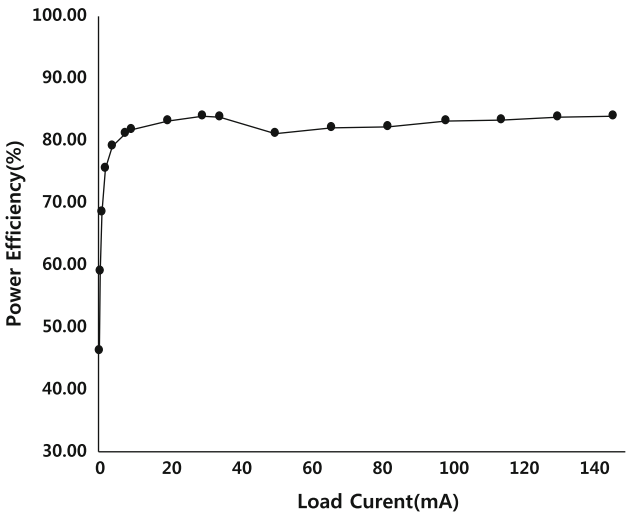

Fig. 14 The measured power efficiency as a function of load current ranging from 1 to 150 mA

4 Conclusions

This paper presented a PFM mode buck converter employing a digitally programmable voltage level–shifting technique and control logic circuit with only one comparator to control peak inductor current with the switching

Table 2 Comparison of the performance of the proposed PFM buck converter with conventional ones

Parameter	[8] (2013)	[9] (2016)	[10] (2016)	[11] (2018)	[12] (2017)	This work
Technology	0.5 μm	0.18 μm	90 nm	65 nm	0.13 μm	0.18 μm
Input voltage	2.5–5.5 V	2.7–3.6 V	1.8–4.2 V	1.8 V	2.2–3.3 V	2.7–3.3 V
Output voltage	0.9–5 V	1–1.2 V	0.9–1.4 V	0.5–1.5 V	1.7 V	1.2 V
Peak inductor current	Un-controllable	Un-controllable	Un-controllable	Un-controllable	Un-controllable	Digitally Programmable
Frequency	1 MHz	Variable	Variable	Variable	Variable	Variable
Ripple voltage	< 10 mV	20 mV@20 mA	< 30 mV	55 mV	–	Adjustable
Load range	10–100 mA	< 150 mA	< 40 mA	< 300 mA	< 20 mA	1–150 mA
Efficiency	83–90%	65–88%	78.5–86%	72–88%	74.2–90.2%	70–84%
Design technique	Pulse skipping	Adaptive on time	HA-AMOT	Adaptive on time	Triple mode	Level shifting

frequency, and consequently, output ripple voltage of the PFM buck converter under different load current conditions. The voltage level-shifting circuit, based on a common source amplifier, is capable of sensing inductor current through the voltage drop caused by the on-resistance of the power switch. Employment of one comparator with the pre-control logic and post-control logic circuits allows the proposed circuit to improve power efficiency by removing an additional circuit, compared to the conventional buck converters [4–6]. The proposed PFM buck converter was implemented with a 180 nm CMOS process. The effective chip size of the core block occupies 900μm × 590μm. The proposed PFM mode buck converter is capable of accommodating an input voltage range of 2.7–3.3 V and producing output voltage of 1.2 V. The operational switching frequency measured is on the order of several to several hundred kilohertz, the load current range is under 150 mA, and the measured output ripple voltage varied. The measured power efficiency ranged between 70 and 84%. The proposed technique employed by the PFM buck converter in this paper is expected to be useful not only to control peak inductor current, but also to control output ripple voltage and power efficiency, so it may be suited to different applications under various load currents.

Acknowledgements This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2010-0020163). The chip was fabricated under the IDEC MPW program.

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