Analog Integrated Circuits and Signal Processing (2018) 97:603–613
https://doi.org/10.1007/s10470-018-1339-6

MIXED SIGNAL LETTER

# Energy-efficient switching scheme for SAR ADC with only two reference voltages

Shubin Liu[1] · Haolin Han[1] · Ruixue Ding[1] · Zhangming Zhu[1]

Received: 11 April 2018 / Revised: 10 July 2018 / Accepted: 24 September 2018 / Published online: 26 September 2018


**Abstract**
An energy-efficient switching method for successive approximation register analog to digital converter is presented in this letter.The proposed two-step switching scheme using the goblet architecture achieves 99.52% less switching energy and 21.09% area reduction over the conventional switching scheme. Moreover, owing to the application of the goblet architecture, the proposed scheme employs only two reference voltages without any requirements for stability or accuracy of the third voltage level.

**Keywords** SAR ADC · Energy-efficient · Two reference voltages · Two-step switching · The goblet architecture

## 1 Introduction

Successive Approximation Register Analog to Digital Converters are widely used in low-power electronic applications as their energy efficiency. However, the switching energy consumed by the DAC array is considerable during a SAR operating cycle. Thus, many new switching sequences have been presented to reduce the DAC energy. The Vcm-based [1] and monotonic [2] achieve energy reduction by 87.54%, 81.2%, respectively. A novel two advanced energy-back SAR ADC switching scheme proposed by Osipov and Paul [3] achieves an energy reduction more than 99%, however, the horrible reset energy cannot be neglected. The LSB split [4] achieves the same energy saving as the two advanced energy-back scheme with a lower reset energy, and Capacitor-spitting presented by Xie et al. [5] consumed zero reset energy, but both of them applied a third reference voltage. It is worth mentioning that although Wu and Wu [6] has presented an ultra-low voltage switching scheme with only two reference, the total energy is yet not satisfying. The novel schemes [7, 8] have the same problem as the Capacitor-splitting and the two advanced energy-back scheme, respectively. Besides, V-aq based tri-level [10] used Vref/4 to achieve more area reduction. While, The added voltage references will result in uncontrollable power and area consumption. Note that the incremental reference voltage means instability and inaccuracy, which should always be considered.

In this letter, a new switching scheme taking account of both energy-efficiency and the reference voltage requirement is presented. The proposed architecture achieves 99.52% energy reduction over conventional scheme with the two-step method. Applying the goblet architecture, redundant reference voltage has been eliminated. The rest of this paper is organized as follows: the introduction of proposed switching scheme is described in Sect. 2, and the implements and advantages of using tow reference voltages are presented in Sect. 3. Section 4 gives explanation on parasitic capacitance and calculation on gain error. The energy consumption based on the analysis of reset energy is raised in Sect. 5. Section 6 provides the analysis and simulation results about linearity, while Sect. 7 concludes the whole switching scheme.

## 2 Proposed SAR switching structure

### 2.1 Proposed architecture

Figure 1 shows the DAC structure of a 10-bit proposed SAR ADC switching scheme. It adopts the two-step

✉ Ruixue Ding
rxding@mail.xidian.edu.cn

[1] Xidian University, Xi'an, Shaanxi, China

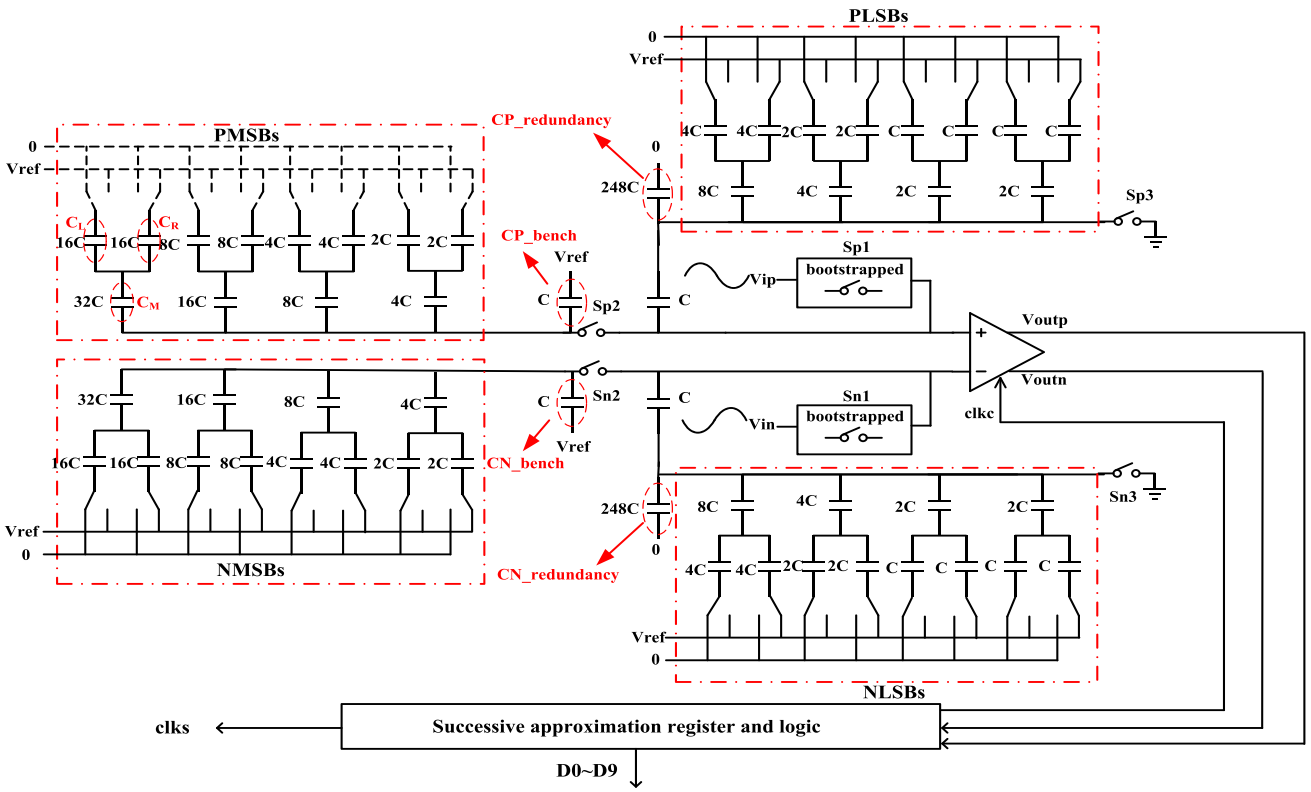



**Fig. 1** Proposed 10-bit SAR ADC switching scheme (M = 4)

architecture that the first (N-M) bits are decided in the first step at "MSBs", while the rest (M) bits are decided in the second step at "LSBs" with a resolution of N-bits. What's more, the proposed SAR ADC splits all the capacitors into the goblet structure which achieves better performance than other schemes with only two reference voltage.

## 2.2 SAR switching scheme

In Fig. 1, M is set to 4. In the sampling phase, all the switches are turned on (Sp1, Sp2, Sp3, Sn1, Sn2, Sn3), so the differential input signal is sampled onto the top plates of the PMSB (NMSB) capacitor arrays, and the top plates of the PLSB (NLSB) arrays sampled the voltage of Gnd. To both of the P-side and the N-side, the bottom plates of "$C_L$"(as is shown in Fig. 1) are connected to Gnd, while the bottom plates of "$C_R$" are connected to Vref. The voltage of "C_bench" which is applied to compensate the binary weighed capacitance array, should be set to Vref, and the voltage of "C_redundancy", similarly, is supposed to be fixed at Gnd. After sampling, the Sp1 and Sn1 are off. And the whole structure can be simplified into Fig. 2.

Due to the top plates sampling, MSB is decided without any energy dissipation. Considering to give a more specific instruction, an example with M equals 4 is presented in Fig. 3. During the MSB-1 comparison, assume that $Vip_N < Vin_N$, that is, $b_N$ equals 0, so $Vin_N$ should be pulled down by Vref/2 with all the bottom plates of the capacitors in NMSBs connecting to gnd, which consumes zero energy. Two approaches are compared in Fig. 4 for a better understanding. If C_bench and C_unit are all replaced by the goblet structure and voltages are initialized as 0 and Vref, then Vref/2 shift can be achieved by setting all the Vref to gnd. However, the least shift in the first step should be Vref/32, which indicates that the last two goblets in MSBs (2C, C, C) are wasted. Utilizing C_bench and C_unit, the same voltage shift can be obtained with more area efficiency. In other words, C_bench and C_unit are employed to make up the amount of binary-weighed capacitors, so they don't participate in the comparison cycles after MSB-1. From the MSB-2 comparison, only the voltages of the PMSBs' capacitors change, the reference voltages connecting to the bottom plates of capacitors in NMSBs are unchanged. If $Vip_{(N-1)} > Vin_{(N-1)}$, the bottom plate of "$C_{R\text{-}max}$" is pulled to Gnd and $b_{(N-1)}$ equels 1. Otherwise the bottom plate of "$C_{L\text{-}max}$" is pulled up to Vref. This process continues until b(N-M) is obtained.

During the second step, switches Sp2, Sp3, Sn2, and Sn3 are all turned off. Thus, Fig. 1 can be simplified into Fig. 5. Because there is no charge or discharge process on the top plate of "C_unit", in other words, the C_unit serves as a coupling capacitor which keeps the input signal all the

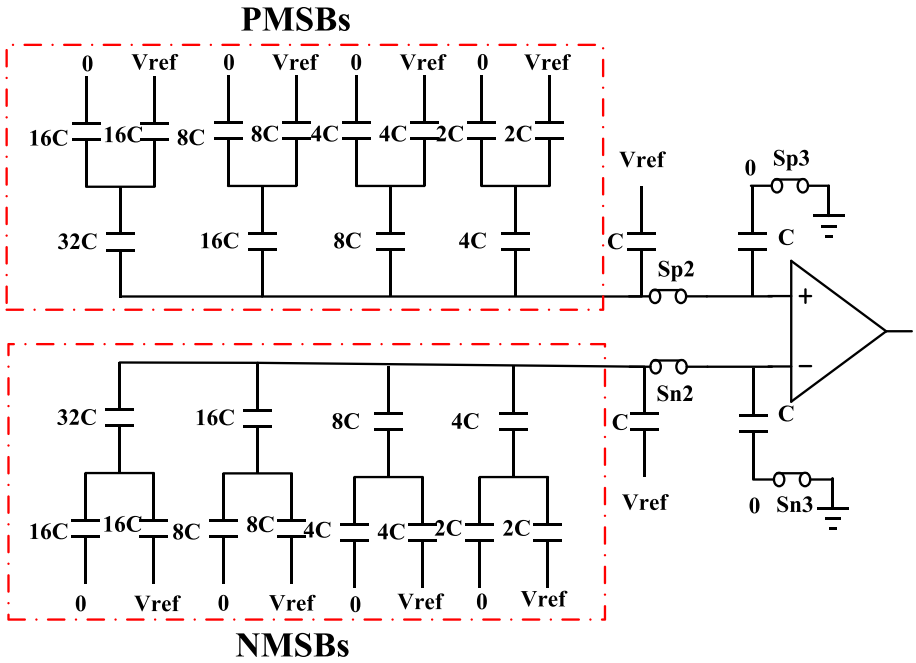



**Fig. 2** The simplified proposed 10-bit SAR ADC switching scheme during MSBs (M = 4)

time. Assuming $Vip_{(N-M-1)} > Vin_{(N-M-1)}$, then all the top plates of "$C_R$" in PLSB (shown in Fig. 1) DAC array should be pulled down to Gnd, and b(N-M-1) equals 1, and the voltage of positive terminal of comparator decreases $Vref/2^{N-M}$. Since the following comparison, only the voltages of the NLSBs' capacitors are supposed to be changed, which is similar to MSBs. If $Vip_{(N-M-2)} > Vin_{(N-M-2)}$, the corresponding bottom plate of "$C_R$" is pulled to Gnd and $b_{(N-M-2)}$ equels 1. Otherwise the bottom plate of "$C_L$" is pulled up to Vref. This process continues until $b_1$ is obtained.

In order to have a better understanding, the waveforms of the proposed SAR switching scheme and the clock signals are provided in Figs. 6 and 7, respectively. Three signals are demonstrate in the Fig. 7, clks, clkc, and RDY. When clks stays in high level, the circuits samples the input signal onto the top plates of the DAC array. After sampling, clkc begins to flow and the DAC array begins to switch. The RDY serves as a reset signal at each end of a comparison cycle.

In the N-bit proposed SAR ADC switching architecture, the LSB size is $Vref/2^{N-1}$. Considering the charge redistribution of the goblet structure, the sum of PLSBs (or NLSBs) should be $2^{N-2}$. Noting that the equivalent capacitance of the goblet architecture can be calculated from series and parallel connection as:

$$C_{eq}(i) = \frac{(C_L(i) + C_R(i)) * C_M(i)}{C_L(i) + C_R(i) + C_M(i)} \quad (1)$$

The value of C_redundancy is given as $(2^{N-2} - \sum_{i=0}^{M-1} C_{eq}(i))$*C), with M equaling to 4.

## 3 The number of reference voltages analysis

### 3.1 The goblet architecture for two reference voltages switching scheme

In a typical switching scheme with two reference voltages (as VDD and GND), if a normal capacitor has been charged into Vref, it cannot be pulled up to a higher level, thus an extra voltage as $V_{cm}$ is necessary to compromise this effect. While, applying the goblet architecture can solve the problem without using extra reference voltage. In a goblet architecture, "$C_L$" has the same value as "$C_R$", and the value of "$C_M$" equals to the sum of "$C_L$" and "$C_R$" as shown in Fig. 8. During the sampling phase, the bottom plate of $C_R$ is set to Vref and the bottom plate of $C_L$ is set to gnd, thus the whole goblet architecture can be both pulled up and down. As a result, an extra reference voltage can be saved.

### 3.2 The relationship analysis between reference voltage number and DAC performance

#### 3.2.1 Linearity

The influence of introducing an extra reference voltage has been analyzed in [3]. For example, according to Osipov's 50000 Monto-Carlo runs [3], if the adding voltage $V_{cm}$ has 1% offset, the maximum DNL error rises 4 × times and maximum INL for 20x times. Therefore, the more reference voltages applied in the switching scheme the worse linearity will be obtained. However, most high power

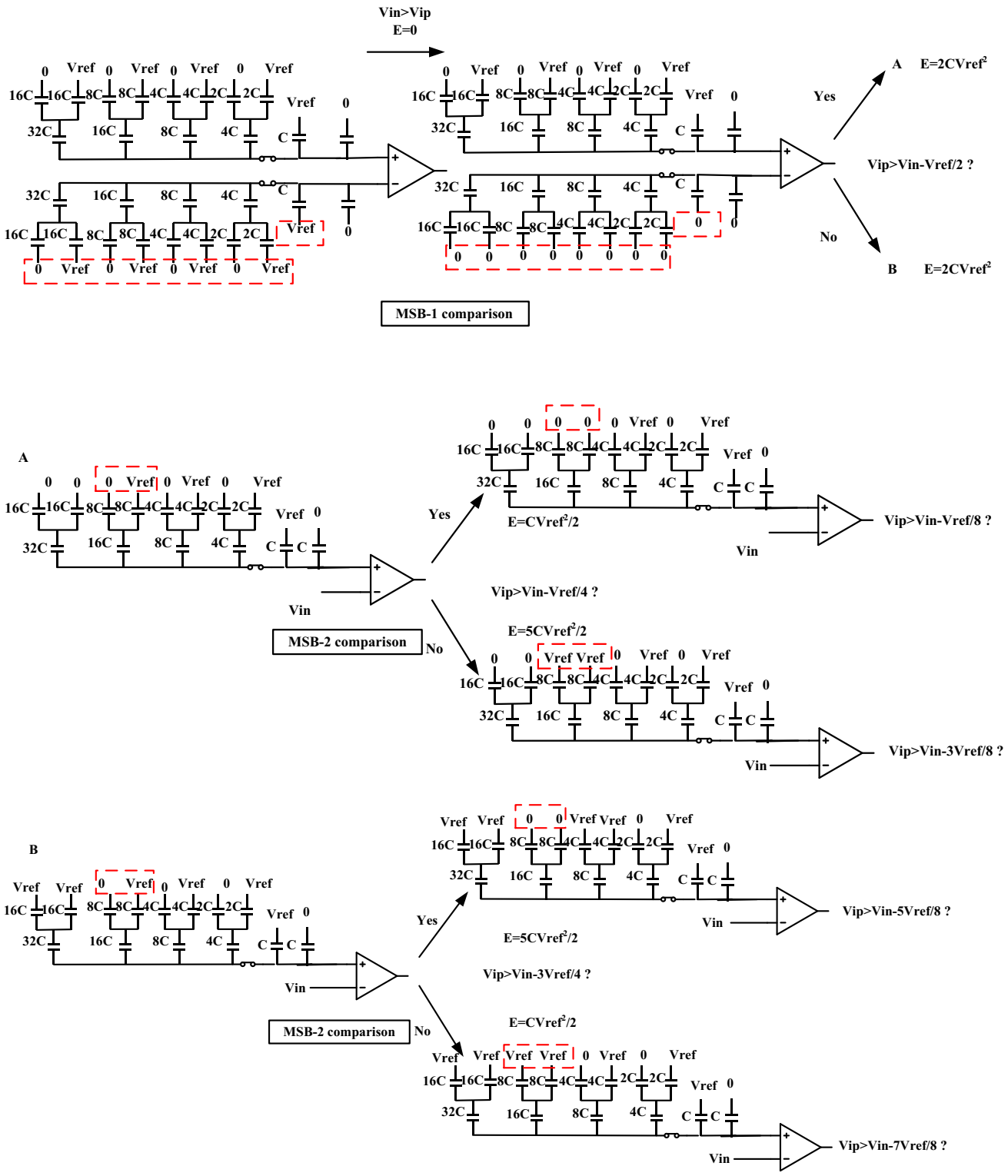



**Fig. 3** The proposed SAR ADC switching scheme at MSBs

efficiency papers published recently didn't take the influence of multi-reference voltages on linearity into account.

### 3.2.2 Power consumption

For the proposed goblet architecture, it can be calculated that both charge and discharge processes among $DAC_{ups}$

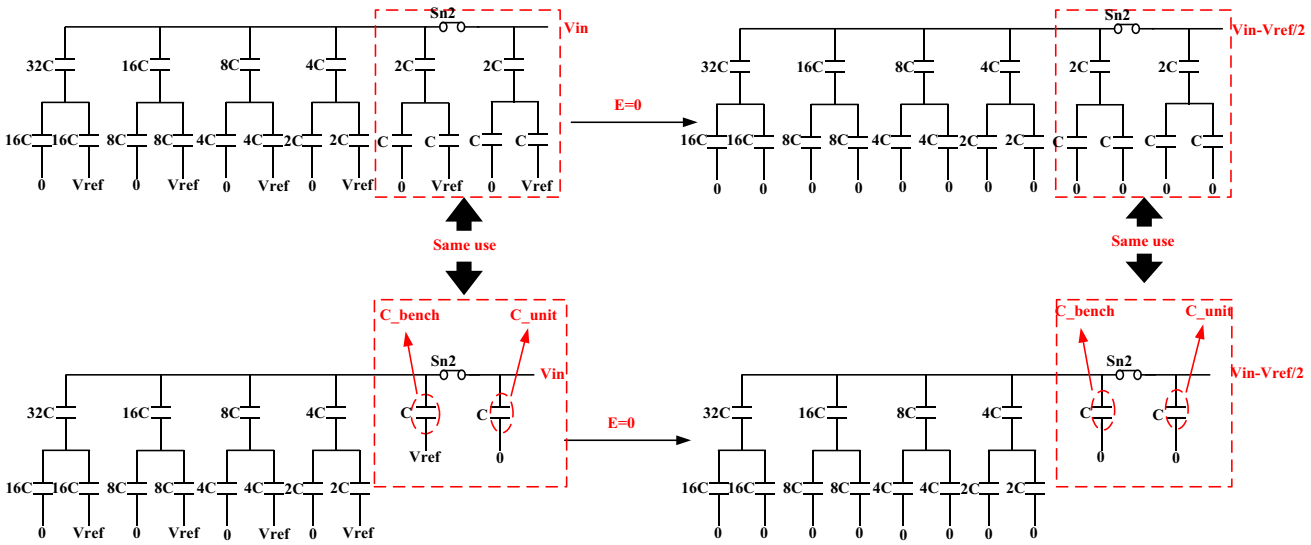



**Fig. 4** Switching method of the DAC array in NMSBs during MSB-1

consume zero energy because of the closed-loop charge recycling [9], thus the power terminal only needs to charge the bottom plate of $C_M$. As $C_L$ is set from gnd to Vref (or $C_R$ is set from Vref to gnd), the bottom plate of $C_M$ only changes Vref/2, which provides more energy saving.

### 3.2.3 Logic complexity

Note that the operation states "on" and "off" of the two reference voltages (Vref, 0) can be easily achieved by a nand gate cell. However, if $V_{cm}$ applied, more transistors are required to obtain the corresponding logic control. Which means more logic complexity and chip area. Therefore, the logic complexity of proposed switching scheme will be relieved.

## 4 Analysis of parasitic capacitances

In the proposed scheme, the parasitic capacitances cannot be ignored because of the series connection. Besides, there are supposed to be two different gain errors at the input terminal due to the utilization of the two step method. Figure 9 presents the parasitic capacitance in p-side in MSBs while Fig. 10 illustrates the parasitic capacitances in p-side during the second step, respectively. $C_{p1}$, $C_{p2}$ present the parasitic capacitances on the top plates of MSBs and LSBs, respectively. And the $C_{p3}$, $C_{p4}$ present parasitic capacitances on the top plates and bottom plates of the unit capacitor. If setting the $C_{L-1}$ from 0 to Vref, the voltage change in Ap should be (2).

$$V_{ip2} - V_{ip1} = \frac{C_{L-1}Vref}{C_{L-1}+C_{R-1}} * \frac{C_1}{C_1+C_2+C_3} * \frac{C_{L-1}+C_{R-1}}{C_{L-1}+C_{R-1}+C_{pr1}} * \frac{C_1+C_2+C_3}{C_1+C_2+C_3+C_{p1}} \tag{2}$$

From (2), we can find the *Gain error* in the first step as

$$Gain1 = \frac{C_1+C_2+C_3}{C_1+C_2+C_3+C_{p1}} * \frac{C_{L-1}+C_{R-1}}{C_{L-1}+C_{R-1}+C_{pr1}}$$

Similarly, when the voltage of $C_{L-5}$ flows from 0 to Vref, the voltage change in Bp can be obtained as:

$$V_{Bp2} - V_{Bp1} = \frac{C_{L-5}(Vref-0)}{C_{L-5}+C_{R-5}} * \frac{C_5}{C_5+C_6} * \left( \frac{C_5+C_6}{C_5} * \frac{C'_5}{C'_5+C'_6+C_{eq}+C_{p4}} * \frac{C_{L-5}+C_{R-5}}{C_{L-5}+C_{R-5}+C_{pr2}} \right) \tag{3}$$

The *Gain error* in second step can be acquired from (3) as

$$Gain2 = \frac{C_5+C_6}{C_5} * \frac{C'_5}{C'_5+C'_6+C_{eq}+C_{p4}} * \frac{C_{L-5}+C_{R-5}}{C_{L-5}+C_{R-5}+C_{pr2}} * \frac{C\_unit}{C\_unit+C_{p2}} \tag{4}$$

If the value of parasitic capacitances on the top plates is linear to the total value of DAC arrays, defaulting the ratio as $\gamma$, we can get

$C_{p1} = \gamma(C_1+C_2+C_3)$, $C_{p4} = \gamma(C_5+C_6)$, $C_{p2} = \gamma C\_unit$, $C_{pr1} = \gamma(C_{L-1}+C_{R-1})$, $C_{pr2} = \gamma(C_{L-5}+C_{R-5})$, $C_{pr3} = \gamma(C_{L-6}+C_{R-6})$

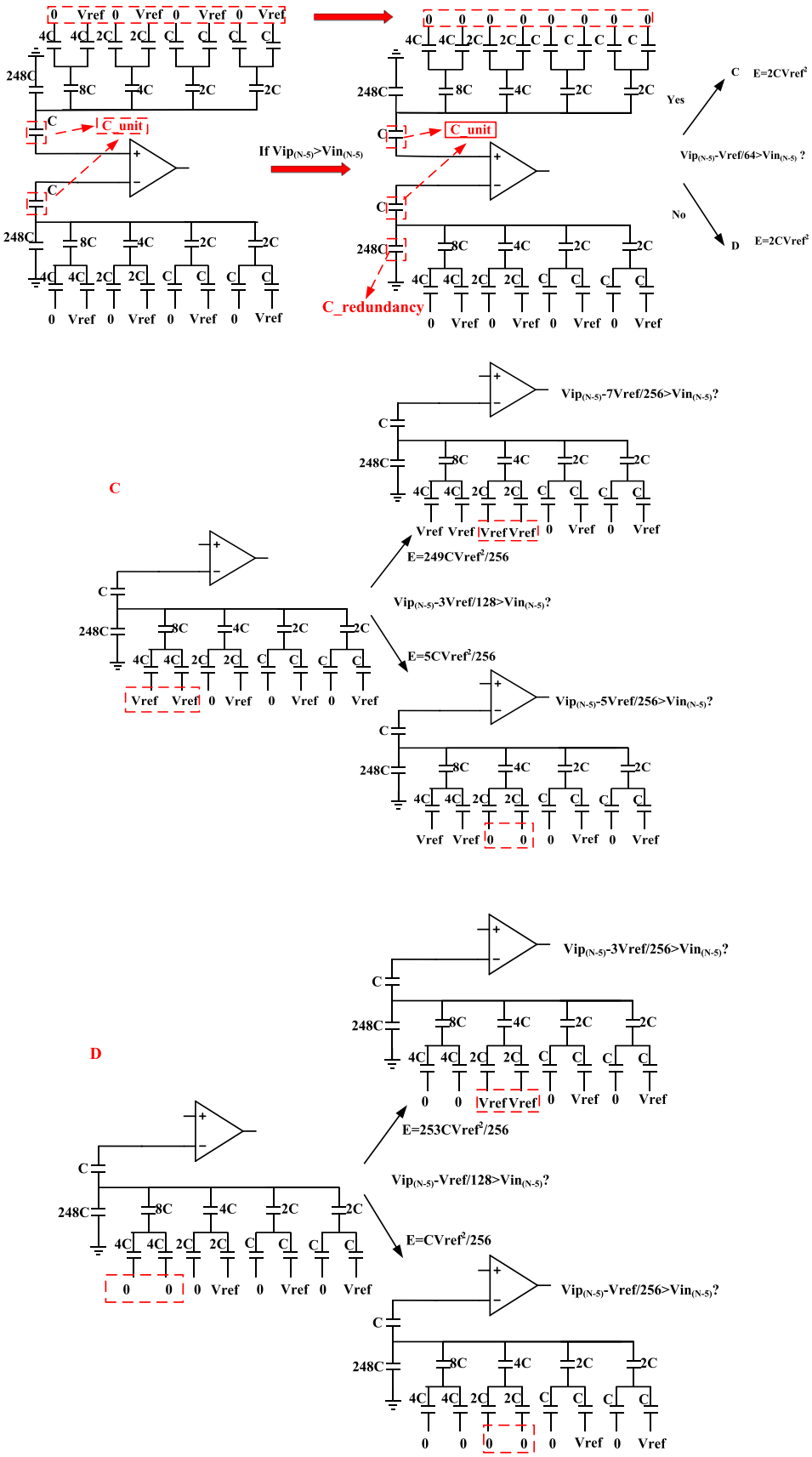



**Fig. 5** The proposed SAR ADC switching scheme at LSBs

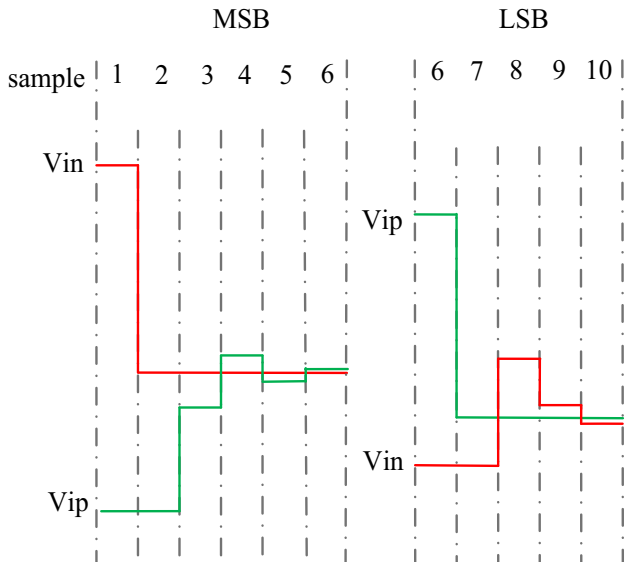



**Fig. 6** Waveform of the comparator inputs

The final expression of Gain1 and Gain2 after simplification is:

$$Gain1 = \frac{C_1 + C_2 + C_3}{C_1 + C_2 + C_3 + \gamma(C_1 + C_2 + C_3)} * \frac{C_{L-1} + C_{R-1}}{C_{L-1} + C_{R-1} + \gamma(C_{L-1} + C_{R-1})} = \frac{1}{(1+\gamma)^2} \quad (5)$$

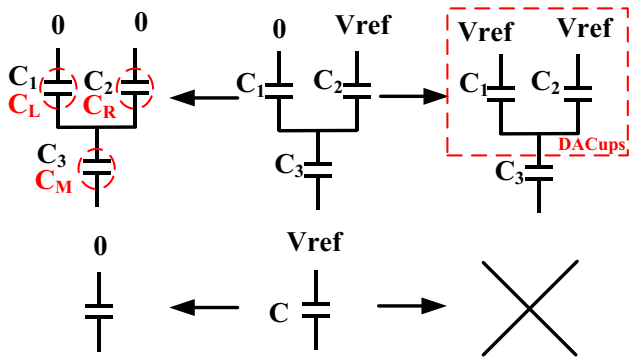



**Fig. 8** Goblet architecture capacitor

$$Gain2 \approx \frac{C_5 + C_6}{C_5} * \frac{(2\gamma+1)C_5}{(C_5 + C_6)(2\gamma+1) + (\gamma+1)\gamma(C_5 + C_6)} * \frac{C\_unit}{C\_unit + \gamma C\_unit} * \frac{C_{L-5} + C_{R-5}}{C_{L-5} + C_{R-5} + \gamma(C_{L-5} + C_{R-5})} \quad (6)$$

In (6), note that

$$C_{eq} = \frac{C\_unit C_{p2}}{C\_unit + C_{p2}} + C_{p3} < C\_unit + C_{p3} << C_5 + C_6$$

Thus

$$Gain2 \approx \frac{2\gamma+1}{\gamma^2 + 3\gamma + 1} * \frac{1}{(1+\gamma)^2}$$

The analysis shows that owing to the parasitic capacitances, there will be two different Gain errors in the MSBs' and LSBs' bits cycle. Usually, the value of $\gamma$ floats from 0.01 to 0.03 according to different process bias. Table 1 shows the value of Gain errors against $\gamma$. Note that the input signal has no error when Gain equals 1, it can be

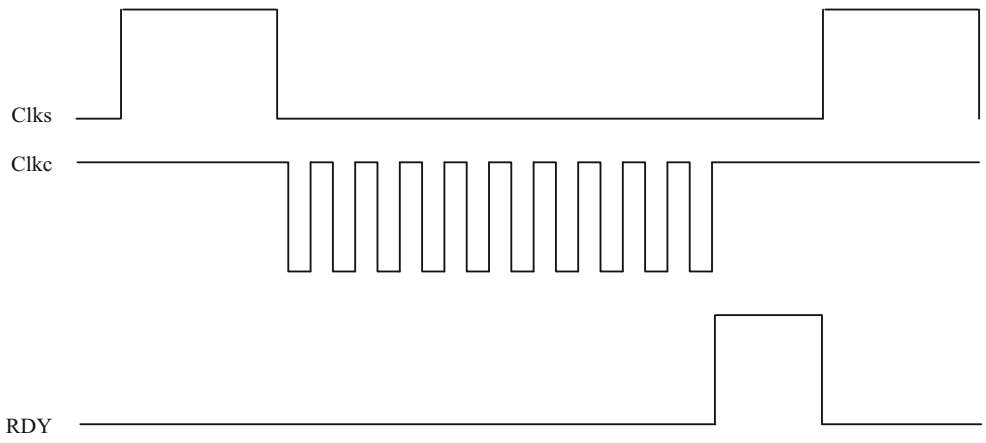



**Fig. 7** Timing waveforms of the clock signals for the SAR ADC operation

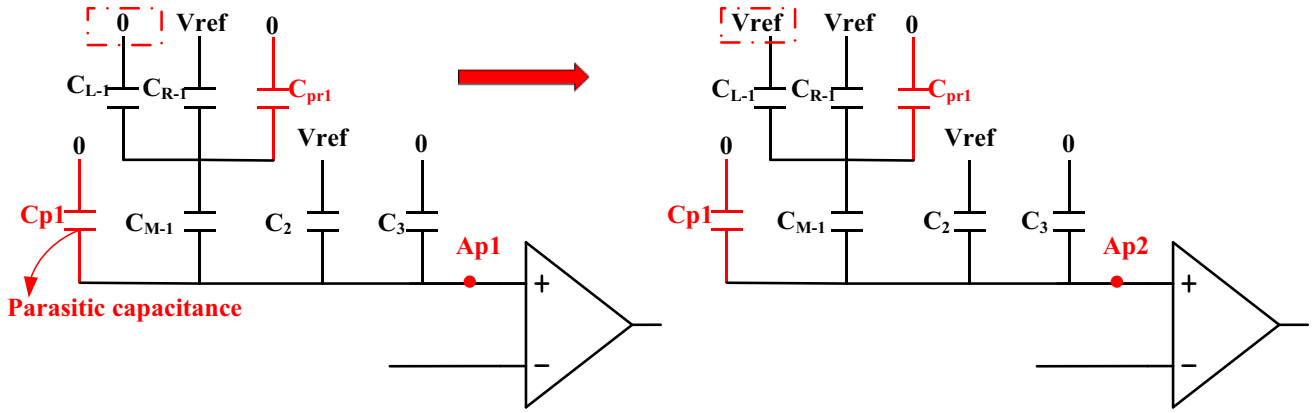



**Fig. 9** Parasitic capacitances in MSBs

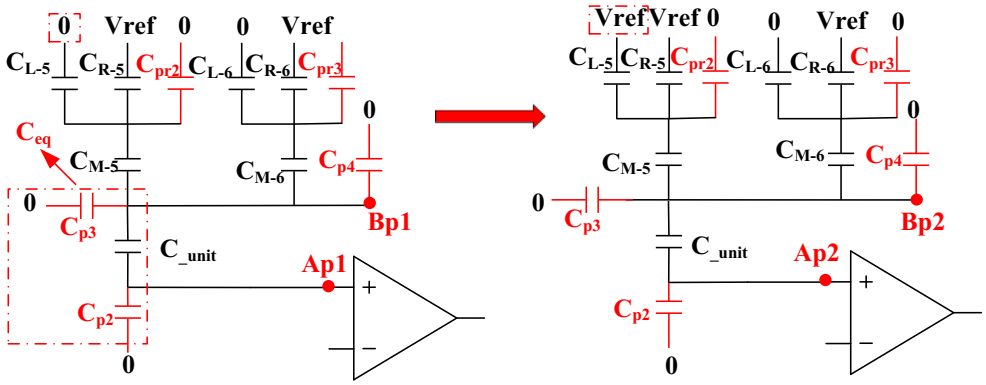



**Fig. 10** Parasitic capacitances in LSBs

**Table 1** Gain error against γ

| Gain error | γ | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0.01 | 0.012 | 0.014 | 0.016 | 0.018 | 0.020 | 0.022 | 0.024 | 0.026 | 0.028 | 0.030 |
| Gain1 | 0.980 | 0.976 | 0.973 | 0.969 | 0.965 | 0.961 | 0.957 | 0.954 | 0.950 | 0.946 | 0.943 |
| Gain2 | 0.971 | 0.965 | 0.959 | 0.954 | 0.948 | 0.943 | 0.937 | 0.932 | 0.926 | 0.921 | 0.916 |

observed that both Gain1 and Gain2 have minimal impact on the accuracy of inputs when γ less than 0.018.

## 5 Energy analysis

### 5.1 Reset energy

Recently published papers such as Osipov and Paul [3] and Baek and Lee [8] have been proved to have good performance in energy saving. However, power terminal still needs to charge the bottom plates of the DAC array when a complete comparison cycle finished which [3, 8] didn't mention.

From Table 2, which presents principal characteristics of different switching schemes, we can find that the average switching energy of the proposed scheme for a 10-bit SAR ADC is 6.573Cvref$^2$, less than [1–6]. While if reset energy being considered, Xie et al. [5] and two-step [7] seem to perform better with zero reset energy, but the dissipation consumed by the circuits which generate the third voltage must be taken into account. Figure 11 shows the energy consumption without reset energy of different schemes against output code.

### 5.2 Optimal value of M

In order to find the optimal value of M, the behaviour simulation of different switching architecture for a 10-bits SAR ADC has been performed. Table 3 shows the different characteristics of proposed scheme about its cap-area, linearity, and switching energy. It can be observed that

**Table 2** Principal characteristics of different switching schemes

| Switching scheme | Switching energy | Energy saving | Reset energy | Total energy | Reference voltage |
|---|---|---|---|---|---|
| Conventional | 1363.3 | Reference | 0 | 1363.3 | Vref, 0 |
| Vcm-based [1] | 170.17 | 87.54% | 0 | 170.17 | Vref, Vcm, 0 |
| Monotonic [2] | 255.5 | 81.2% | 0 | 255.5 | Vref, 0 |
| Osipov and Paul [3] | 8.63 | 99.36% | 111.75 | 120.38 | Vref, Vcm, 0 |
| LSB split [4] | 10.8 | 99.2% | 48.12 | 58.92 | Vref, Vcm, 0 |
| Xie et al. [5] | 10.54 | 99.23% | 0 | 10.54 | Vre, Vcm, 0 |
| Wu and Wu [6] | 21.3 | 98.4% | 64 | 85.3 | Vref, 0 |
| Two-step [7] | 3.44 | 99.75% | 0 | 3.44 | Vref, Vcm, 0 |
| Baek and Lee [8] | 1.91 | 99.86% | 74.58 | 76.49 | Vref, Vcm, 0 |
| Proposed | 6.573 | 99.52% | 24.10 | 30.673 | Vref, 0 |

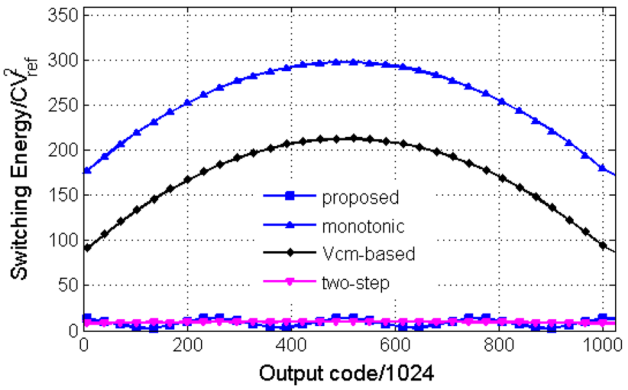



**Fig. 11** Switching energy against output code

when M > 5, the linearity tends to be unstable, which will lead to errors such as code missing, Below 6, choosing M = 3 can get a modifying in linearity, but the capacitor area and the total energy consumption are undesirable. Thus, M is chosen to 4 with the lowest energy consumption, an acceptable linearity and relatively small area for capacitor.

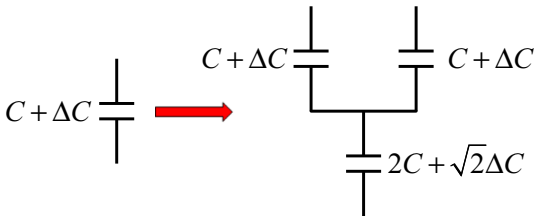



**Fig. 12** Mismatch of the goblet structure

## 6 Linearity

It is always the capacitors mismatch that determinate the minimum value of the unit capacitance. Assume that the unit capacitor takes a nominal value of Cu with standard deviation of σu which equals 0.01(σu(ΔC/C) = 0.01). Since the proposed switching scheme adopts the goblet architecture, the linearity of the SAR ADC can get a modicum of improvement. Provided a unit capacitor with a nominal value C and an error of ΔC, after using goblet structure (Fig. 12), the error of the unit capacitor can be described as:

$$C_{C-2C\_error} = \frac{(C+\Delta C + C + \Delta C) * (2C + \sqrt{2}\Delta C)}{(C+\Delta C + C + \Delta C + 2C + \sqrt{2}\Delta C)} - C = \frac{(2+\sqrt{2})C\Delta C + 2\sqrt{2}\Delta C^2}{4C + (2+\sqrt{2})\Delta C} \tag{7}$$

**Table 3** Principal characteristics of proposed switching scheme with M 3 ∼ 7

| M | Capacitors area | Max (INL-RMS) | Switching energy | Reset energy | Total energy |
|---|---|---|---|---|---|
| 3 | 836 | 0.466 | 10.92 | 33.82 | 44.74 |
| 4 | 804 | 0.546 | 6.573 | 24.09 | 30.66 |
| 5 | 724 | 0.799 | 5.854 | 26.54 | 32.394 |
| 6 | 756 | 0.820 | 8.292 | 42 | 50.292 |
| 7 | 916 | 0.957 | 14.67 | 76.68 | 91.35 |

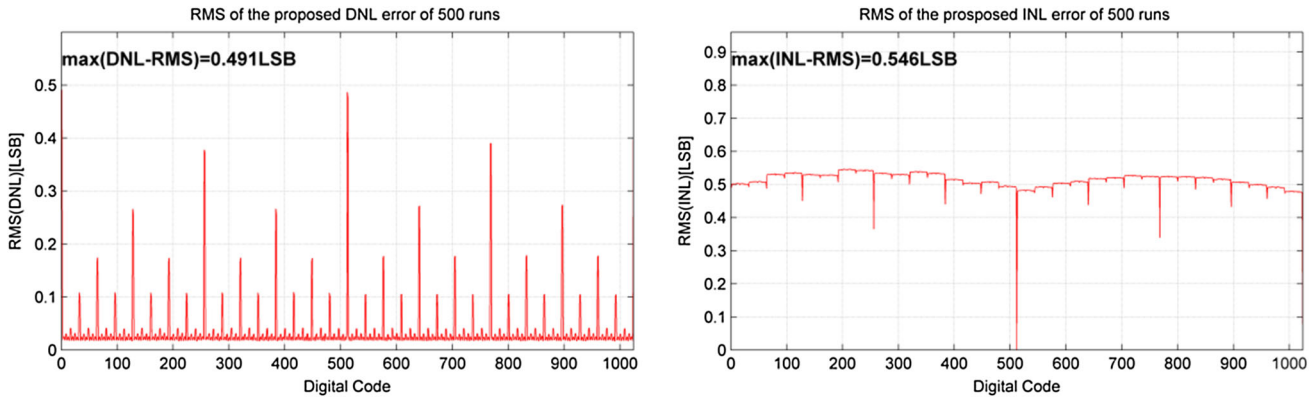



**Fig. 13** Linearity simulation result of proposed scheme

Because $\Delta C \ll C$, the the $\Delta C^2$ in the formula can be neglected, then divide both top and bottom with C, we can get $C_{goblet\_error} \approx (2 + \sqrt{2})\Delta C/4$, which is lower than $\Delta C$. The simulation results of 500 Monte Carlo runs of 10-bit SAR ADC with the proposed switching scheme is shown in Fig. 13.

## 7 Conclusion

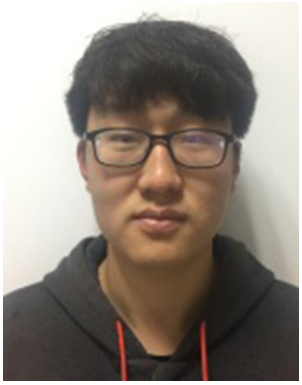
In this letter, an energy-efficient switching scheme with two reference voltages has been presented. Splitting all the capacitors into the goblet structure and reusing of the unit capacitor, the proposed switching scheme achieves an energy saving by 99.52% at 10-bit level. Even considering the reset energy, the proposed scheme performs better than recently published schemes. Simultaneously, the goblet structure also allows to benefit from using only two reference voltage which significantly reduces power and dependence on the requirements for stability or accuracy of the third voltage. In summary, the proposed scheme achieves a trade-off between energy-saving and the quantity of reference voltages.

**Funding** Funding was provided by National Natural Science Foundation of China (Grant Nos. 61504104, 61322405) and Natural Science Foundation of Zhejiang Province (Grant No. LQ15F040003).

## References

1. Zhu, Y., Chan, H., Chio, U. F., Sin, S. W., Seng-Pan, U., Rui, P. M., et al. (2010). A 10-bit 100-ms/s reference-free SAR ADC in 90 nm CMOS. *IEEE Journal of Solid-State Circuits, 45*(6), 1111–1121.
2. Liu, C. C., Chang, S. J., Huang, G. Y., & Lin, Y. Z. (2010). A 10-bit 50-ms/s SAR ADC with a monotonic capacitor switching procedure. *IEEE Journal of Solid-State Circuits, 45*(4), 731–740.
3. Osipov, D., & Paul, S. (2016). Two advanced energy-back SAR ADC architectures with 99.21 and 99.31% reduction in switching energy. *Analog Integrated Circuits and Signal Processing, 87*(1), 81–91.
4. Bahzard, G., & Ebrahim, A. (2017). LSB split capacitor SAR ADC with 99.2% switching energy reduction. *Analog Integrated Circuits and Signal Processing, 93*(1), 375–382.
5. Xie, L., Su, J., & Wen, G. (2015). Energy-efficient capacitor-splitting DAC scheme with high accuracy for SAR ADCs. *Electronics Letters, 51*(6), 460–462.
6. Wu, A., & Wu, J. (2017). Energy-efficient switching scheme for ultra low voltage SAR ADC. *Analog Integrated Circuits and Signal Processing, 90*(2), 507–511.
7. Ding, A., & Zhu, Z. (2015). High efficiency two-step capacitor switching scheme for SAR ADC. *Analog Integrated Circuits and Signal Processing, 86*(1), 127–131.
8. Baek, S. U., & Lee, M. (2018). Energy-efficient switching scheme for SAR ADC using zero-energy dual capacitor switching. *Analog Integrated Circuits and Signal Processing, 94*(2), 317–322.
9. Hu, Y., Liu, A. B., & Wu, Z. (2016). Closed-loop charge recycling switching scheme for SAR ADC. *Electronics Letters, 53*(2), 66–68.
10. Zhao, J., Mei, N., Zhang, Z., & Meng, L. (2018). Vaq-based tri-level switching scheme for SAR ADC. *Electronics Letters, 53*(2), 66–68.

**Shubin Liu** received the B.S. and Ph.D. degree in microelectronics from Xidian University, Xi'an, China, in 2007 and 2014, respectively. His current interests include high-resolution high-speed data converters, SAR ADC and mixed-signal VLSIs.



**Haolin Han** is now currently working toward the M.S. degree at the school of microelectronics, Xidian University, Xi'an, China. His research interests include nanoscale SAR ADC and low voltage low power analog integrated circuits design.

**Ruixue Ding** received the B.S., M.S., and Ph.D. degrees in microelectronics and solid-state electronics from Xidian University, Xi'an, China, in 2003, 2006, and 2011, respectively. He is currently an Associate Professor with the School of Microelectronics, Xidian University. His current research interests include mixed-signal integrated circuits design and high-performance 3-D integrated circuits.

**Zhangming Zhu** received the B.S., M.S. and Ph.D. degree in microelectronics from Xidian University, Xi'an, China, in 2000, 2003, and 2004, respectively. He is currently a professor with the school of microelectronics, Xidian University, Xi'an, China. His research interests include low power mixed-signal integrated circuits, SAR ADC, high speed ADC/DAC, green-power power ICs, and 3D-ICs based on the TSV.