



A novel ALL-digital low power delay lines based time difference amplifier for coarse-fine TDC

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Abstract

In most of digital systems, which require to have high level of resolution, time for digital converter is among the most significant blocks. Time difference amplifier (TDA) is utilized in time to digital converter in order to increase the level of accuracy. In this article, an all-digital TDA is suggested. The proposed TDA consumes delay lines with variation delay for amplifying. The proposed circuit is designed and simulated in 65 nm CMOS technology and obtain gain of six and chip areas about 0.002 mm². The maximum calculated addition error is about 5%. The TDA harnesses 0.74 mW power under 1.1 V supply voltage.

Keywords TDA · TDC · Delay line · Low power · Time amplifying

1 Introduction

Time measurement is a very essential method for engineering and science researches. Time to digital converter (TDC) is a circuit that can determine the time and convert it to digital code. TDC has numerous applications, such as phase failure detection in the design of PLLs [1–4]. The use of TDCs instead of phase comparator in PLL structure leads to removal of analog parts such as charge pump and loop filter. As a result, power consumption, stability against noise and compressibility are improved. In addition, TDC is used in the structure of time-based analog to digital converters [5, 6]. In this type of analog to digital converters, analog input voltage is turned into a time interval, and then the time interval is converted to a digital code through TDC. In time of flight (TOF), positron emission tomography (PET) [7, 8], the TDC measures the time duration where gamma rays are accumulated in an annihilation event and finally the digital code is produced by the TDC. Also in laser TOF distance

measurement [9–11], the time duration between sending of laser pulse and receiving it is computed by TDCs, therefore the distance from the intended target can be calculated. Moreover, TDCs are used in fluorescence lifetime imaging microscopy (FILM) structures [12, 13] that are applicable in biological, biophysical and biochemical structures for functional imaging and environmental monitoring.

Delay line based [14–18] and multi-stage groups [19, 20] are two important kinds of TDCs. Two significant TDCs, flash and vernier structures consume the delay line. In flash TDC, one delay line and in vernier TDC two delay lines and a comparator, produce the digital code based on the time difference between inputs. To optimize these structures, various techniques have been employed recently, articles such as, two-dimensions Vernier TDC [4], 3-D Vernier space TDC [9], Vernier ring TDC [3] and gated-Vernier TDC [7]. Such circuits, besides the high conversion time, have restricted dynamic range and low resolution. The other kinds of TDCs are the multi-stage TDCs that usually include two stages: coarse stage with low resolution and high dynamic range and fine stage for achieving better accuracy. Furthermore, this TDC has a high dynamic range. In the multi-stage TDC, the TDA can be applied so as to ameliorate the resolution. The residue pulse of the coarse stage can be amplified with TDA and then it is applied to the fine stage.

The conceptual block diagram of TDA is shown in Fig. 1. The input pulses have time difference Δt between

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rising edges, which is amplified by gain factor of TDA (N), and output signals with time difference of $N * \Delta t$ are then, generated. It should be noted that the residue of time difference in coarse stage is augmented with the gain of TDA. Maximum Gain of TDA is $(DR\ Fine)/(Resolution\ coarse)$. Since the amplified signal, which is the output of the TDA, is conducted into the fine stage, the dynamic range of fine stage should be wide enough to cover the amplified signal. Therefore, the maximum gain of the TDA depends on the dynamic range of the fine stage. On the other hand, by enhancing the gain of TDA, the linearity of TDC will be decreased. TDAs have been presented in sundry types of structures. Charge domain TDA [20–22], is a kind of TDA, which first changes the time difference to the charge and then reinforces the charge amplitude and the amplified amplitudes is altered into the voltage by the capacitor. Finally, this voltage is converted to the time difference by the comparator. Figure 2 shows one charge domain TDA circuit. In this TDA, the phase detector (PD) is utilized so

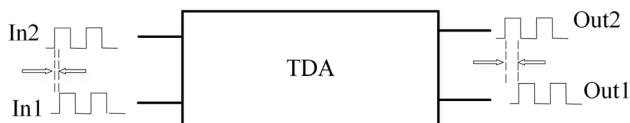


Fig. 1 Block diagram of TDA

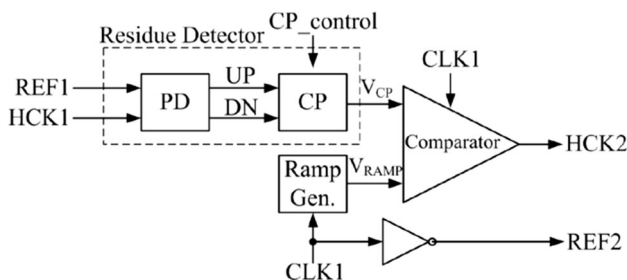
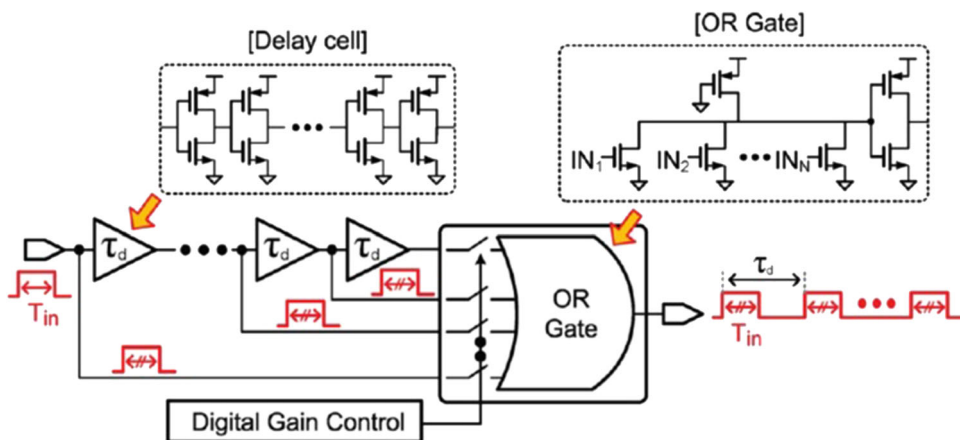


Fig. 2 Schematics of charge domain TDA [20]

Fig. 3 Schematics of pulse train TDA [19]



as to recognize previous TDC stage residue. Then the charge pump (CP) is used to exchange the time residue into voltage. Comparator, comparing the output voltage of CP with ramp signal and then, generate the amplified output. The other kind of TDA is illustrated in Fig. 3. In such TDA, the input time difference pulses are inserted with each other by considering the delay between them [19]. Then the output is applied to the delay cells of fine stage as the control input. The amplifying is done only at $\pm 1/2$ LSB, and at the other points the operation of amplifying is hampered. Latch based TDA is the other type of TDA, which has been presented based on latch is shown in Fig. 4 [23, 24]. The nodes A and B are initially pre-charged to when two inputs are low. The output of the TA is determined by the discharging times of A and B when rising transitions of the inputs are requested. The discharging is performed by two variance paths, by M1 and M3, and a dependent path, by M2 and M4. Not only does not this TDA have sufficient resolution, but also it has limited linear range. Consequently, it requires the calibration. DLL-based TDA [25], which is shown in Fig. 5. Since DLL can only deal with periodic clock signals, two same oscillators were used. Constant delay line is controlled with DLL1 and variable delay line is controlled with DLL2. The PD of DLL2 compares the phase difference between the first delay cell in variable delay line and constant delay line

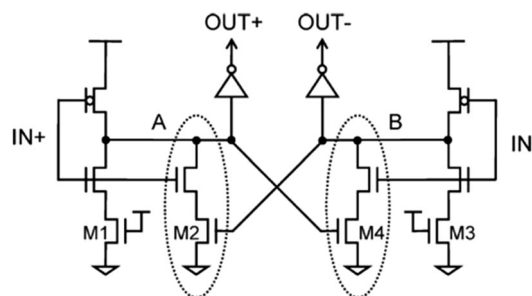
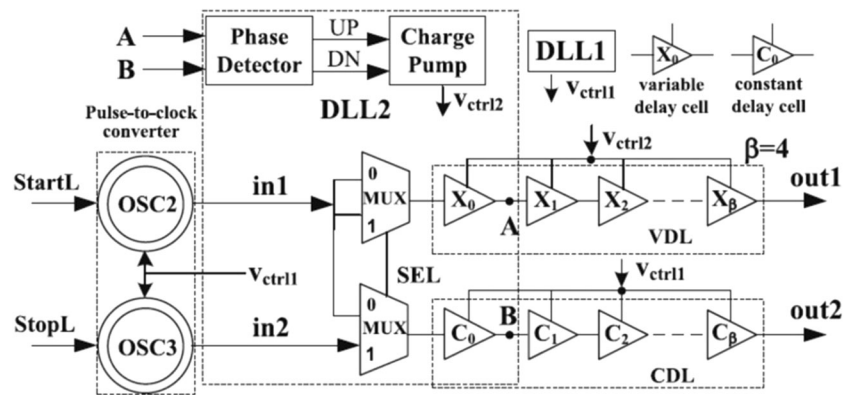


Fig. 4 Schematics of latch based TDA [24]

Fig. 5 Schematics of DLL-based TDA [25]



and CP change out puts of PD to control voltage for variable delay line. The gain of TDA is calculated with the number of delay cells.

In this paper, a novel all-digital TDA is recommended. The proposed TDA uses the delay lines for amplifying. The gain of TDA can be adjusted based on delay of the delay lines. The paper is organized in the following parts. Section II describes architecture and the structure of the proposed circuit. Section III presents simulation results and comparisons with recently published TDAs. The paper is concluded in Section IV.

2 Delay lines based time difference amplifier

The total structure of the proposed delay lines based TDA is shown in Fig. 6. As it is completely obvious in Fig. 6, the circuit consists three delay lines. The first and second delay lines are connected to the stop signal, while the third delay line is connected to the start signal. The created delay by the second and third delay lines are calculated based on (1) and (2), respectively. The D_{b2} is related to the delay of one buffer in second delay line, D_{b3} shows delay of one buffer in third delay line and N is refer to the number of stages. The outputs for delay difference of these two delay lines in each stage are equal to $D_{b2}-D_{b3}$ (the delay of D_{b3} is more than D_{b2}). The total delay difference of these two delay lines (Δt_{n1}) is achieved by (3). Based on the fact that the start signal comes sooner than the stop ones, and D_{b3} delay is more than D_{b2} delay, after each stage the time interval between these two signals is reduced, and finally after N stages the two signals will reach together.

The stop output of the TDA is elected from the first delay line, whereas the start output of the TDA is an input start signal. The output of the first line after N stages is showed in (4) that in each stage the delay, which equals to the delay of the one buffer, D_{b1} adds to the start signal. When the stop and start signals reach together through

delay lines 2 and 3 after N stages, the output of delay line 1 and start signal conceive as final output at N th stage. As a matter of fact, the start and stop signals have the delay difference (Δt_{n2}) throughout delay line 1 and start signal, which is based on (5). As it is expressed in (3), the start and stop signals with together after N stages from the second and third delay lines. By measuring N from of (3), and then, considering the time that two start and stop signals have zero time interval and utilizing it at (5), the total delay difference is calculated like (6). Finally, the total gain of the TDA is obtained based on (7). As a result of this equation, the total gain of the circuit is directly proportional to the ratio of delay of the first delay line to the delay difference of the second and third delay lines. By altering this ratio, the gain of the TDA can be varied.

$$t_{stopn1} = t_{stopin} + (N \times D_{b2}) \tag{1}$$

$$t_{startn1} = t_{startin} + (N \times D_{b3}) \tag{2}$$

$$\Delta t_{n1} = t_{stopn1} - t_{startn1} = \Delta t_{in} + N(D_{b2} - D_{b3}) \tag{3}$$

$$t_{stopn2} = t_{stopin} + (N \times D_{b1}) \tag{4}$$

$$\Delta t_{n2} = t_{stopn2} - t_{start} = \Delta t_{in} + N(D_{b1}) \tag{5}$$

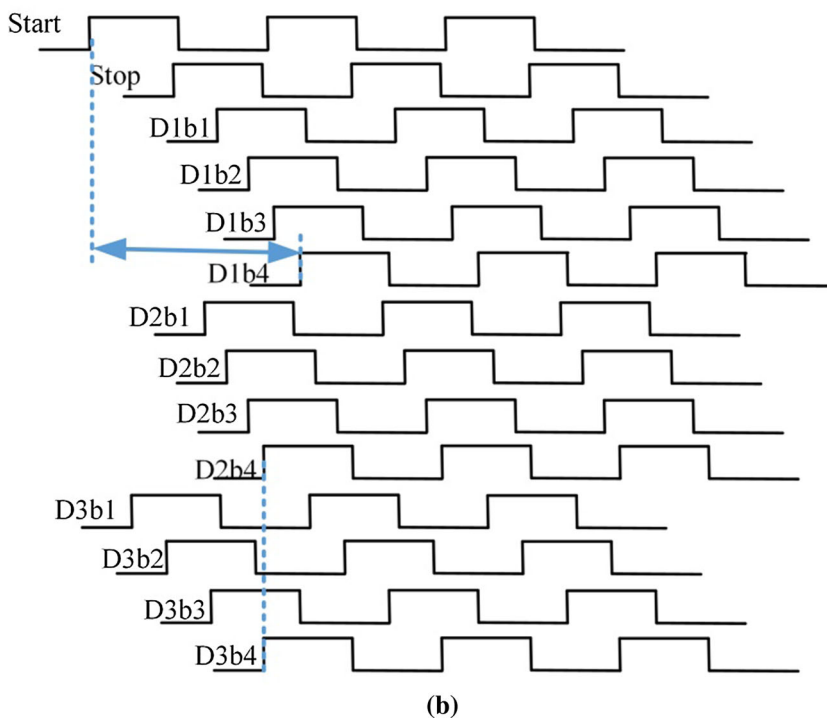
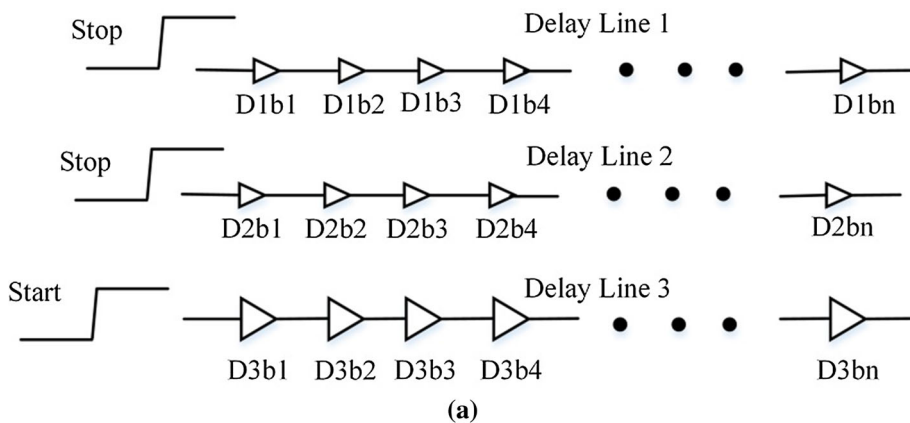
$$\Delta t_{n2} = \Delta t_{in} + \frac{\Delta t_{in}(D_{b1})}{D_{b2} - D_{b3}} \tag{6}$$

$$Gain = \frac{\Delta t_{n2}}{\Delta t_{in}} = 1 + \frac{D_{b1}}{D_{b2} - D_{b3}} \tag{7}$$

The wave forms of the suggested TDA are presented in Fig. 6(b). As it is entirely evident, when the interval time of the second and third delay line signals becomes zero, the high level of time difference between the start signal and first delay line output like the TDA outputs still exists.

The architecture of the recommended delay line based on TDA is shown in Fig. 7. According to Fig. 7, the TDA consists of the delay lines, comparator and selection block. The proposed circuit has three delay lines that the second and third ones diminished the interval time of the start and stop input signals. The outputs of each stage from these two delay lines are applied to the comparator in order to clarify

Fig. 6 **a** Structure of the proposed delay lines based TDA, **b** wave forms



the time that the difference between start and stop signals become zero. The outputs of the comparators are applied to the selection block as the control signals. The selecting block chooses the stop signal of the TDA from the first delay line. Thus, the outputs of each stage from the first delay lines are picked as the selection blocks input and the comparator outputs are applied to the selection block as the control signals. The circuit, which is shown in Fig. 8(a), is harnessed as the comparator. The procedure of this circuit is described in the following parts: at the rising edge of the stop signal, the start signal is sampled. The output Q (Q_n) equals to 1 (0), respectively, unit the start signal has lower delay than the stop signal. When the interval time equals to zero or when the start signal has more delay than the stop signal, the output Q (Q_n) becomes 0 (1), respectively. The wave forms are presented in Fig. 8(b), which shows the

operation of the comparator circuit. The selection block is presented in Fig. 9. The outputs are produced by the comparators are exerted to the selection block as the same as the control signals. The output of each delay cell is contemplated like the input of the selection blocks (the firth delay line for the stop signal). When the start signal passes the stop signal of the second and third delay lines, the output Q of the comparator becomes zero. Thus, at the stage that the comparator output changes from one to zero, its comparator becomes zero. Thus, at the stage that the comparator output changes from one to zero, its relative input of the first delay line transmits to the output of the selection block like the final stop output (the transistors n2 and p2 turn on and transistor n4 turns off). If the outputs of the two consecutive comparators do not alter from one to zero, the output of the transmission gate, which is related to

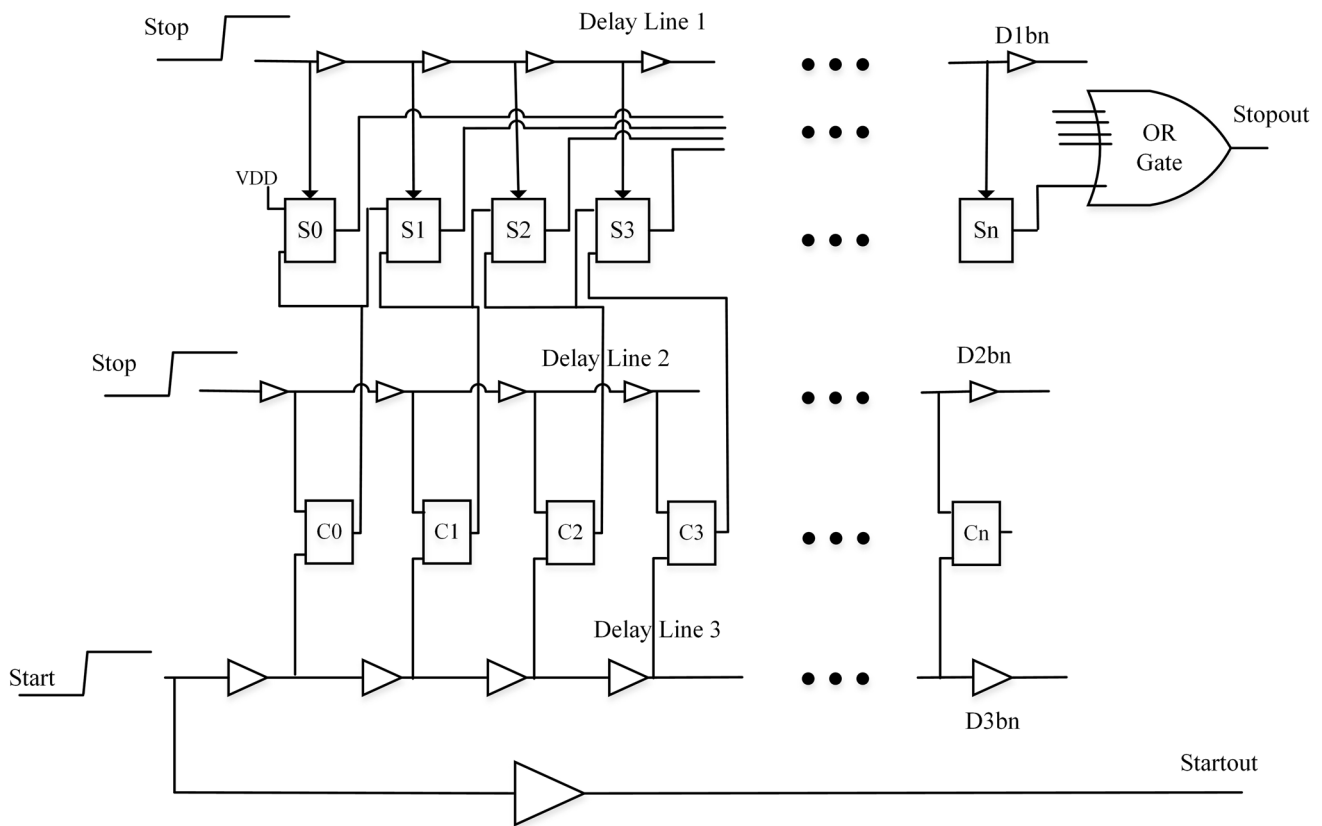


Fig. 7 The proposed delay line based TDA

this stage, will become zero (transistor n4 turns on). At the end, all outputs of selection block add together with or gate. At the ideal case, for the zero input, zero value is set at the output and for the input between zero and 1 LSBs (DB3–DB2), the output has the value between zero and 1 LSBs. To shed more light on this matter, the input that is applied to the circuit is transferred to the output when the input has the worth between 1 LSBs, and 2 LSBs the output change from 1 LSBf (DB1) + 1 LSBs to 1 LSBf + 2 LSBs. In this case, the gain error will be highly increased at the end of this range. As a result, the initial difference, which is employed to the circuit, equals to 1/2 LSBf. Lower than 1 LSBs the output signal is not amplified and the time difference of the inputs is exactly transferred to the output. Therefore, the gain error is enhanced at this section. Usually, the residue of the coarse stage, which is between 0 and 1 LSBc (1 LSB of coarse stage) is injected to the fine stage. For reducing the error of the TDA, 1 LSBc + Residue of the coarse stage is applied to the fine stage as the input. In this situation, the interval time has the worth between 1 LSBc and 2 LSBc; thus, the error of the TDA earn will be attenuated. The maximum percentage of the TDA gain error is calculated from (8). According to the fact that the coarse stage resolution of the proposed circuit equals to 59 ps, the gain of the circuit is conceived as 6. All

in all, the maximum percentage of the gain error is 2.8% in compare with the ideal case. Notwithstanding, the buffers offset, which causes from the buffers deviates the operation of the circuit from the ideal case, and then creates the gain deviation.

$$Max\ Gain\ Error = \frac{\pm \frac{1}{2}(Db_1)}{6\Delta tin} \times 100 \tag{8}$$

The output interval time versus the input interval time of the proposed TDA is presented in Fig. 10(a). According to Fig. 10(a), the input is exerted to the TDA by increasing its interval time to 1 ps. In Fig. 10(b), the addition error for this condition is assessed that the maximum gain error of the proposed circuit equals to 5%. As a result of Eq. (8), the maximum gain error at the desire situation is achieved about 2.8%, however thanks to the non-ideality of the buffers operation, the gain error percentage is increasing at the delay line. According to what is presented in (8), when the pulse width becomes expanded, the gain error percentage will be reduced. Nonetheless, unlike (8), Fig. 10(b) illustrates the increment of gain error with the raising of the pulse width. This error growth in Fig. 10(b) comes from the non-ideality of buffers in delay lines that transmits to the next stages and enhances the gain error of the last stages.

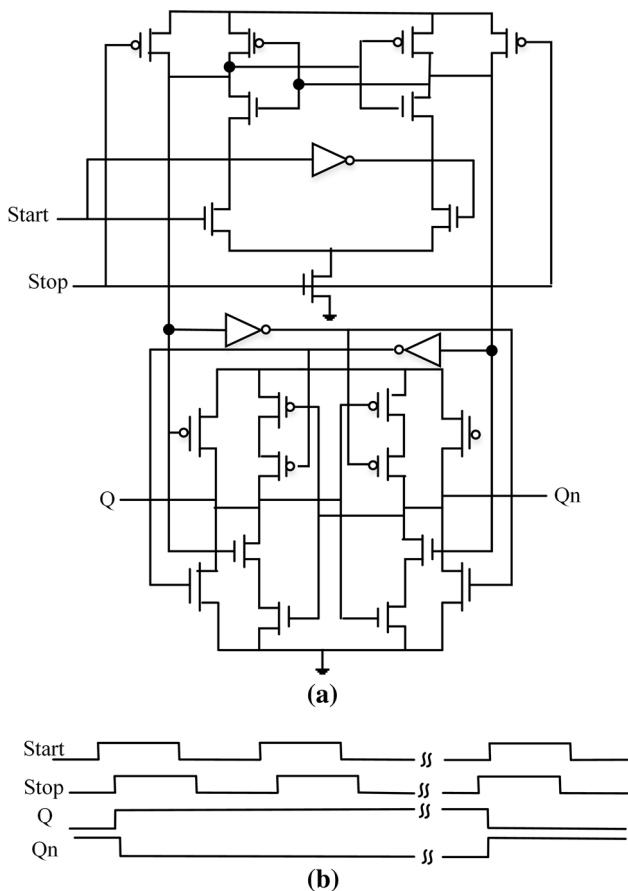


Fig. 8 a Comparator, b wave forms

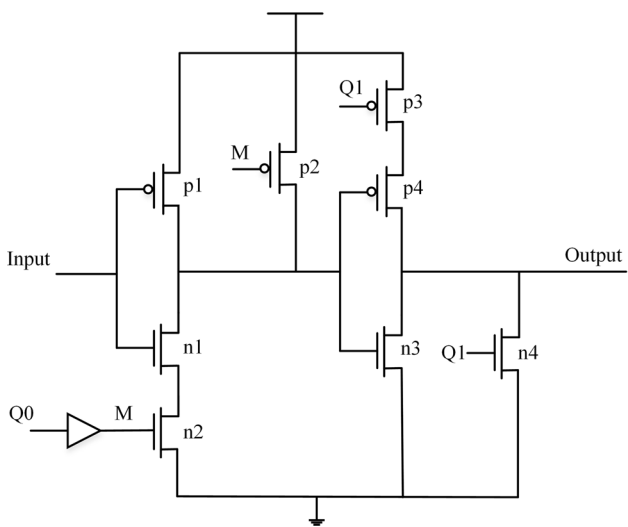


Fig. 9 Selection block

The proposed TDA contains 30 stages. Since the TDA input equals to 1 LSBc + Residue, the interval time between start and stop signals of the second and third delay lines does not equal to zero during the 15 stages.

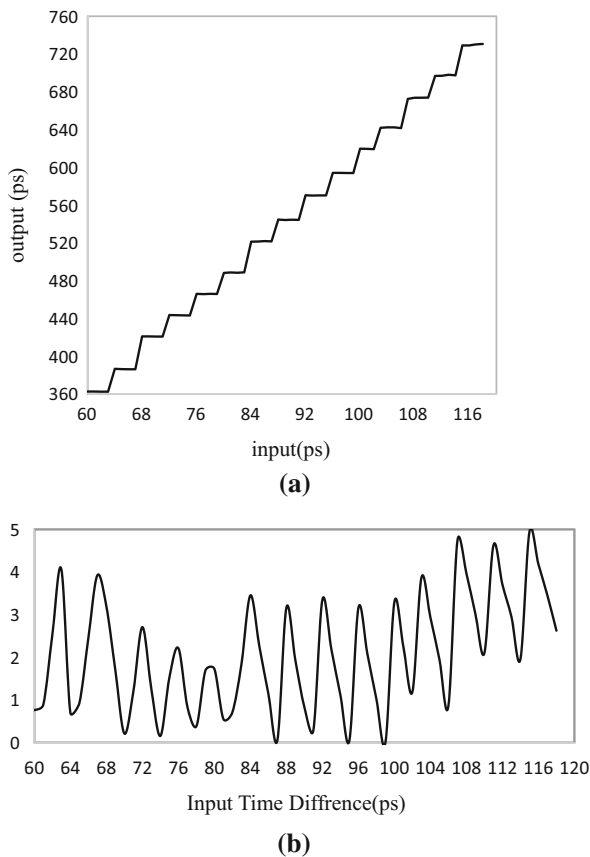


Fig. 10 a The output time interval versus the input time interval of the proposed TDA, b the gain error

Consequently, the comparators are eliminated at the first 15 stages in order to reduce the power consumption and area.

3 Simulation results

The proposed TDA was simulated in 65 nm supplementary metal-oxide semiconductor (CMOS) technology. The outcomes are presented in this paper are based on post layout simulations in the Cadence Virtuoso package using Hspice simulator. The area of the suggested TDA is only $78.9 \mu\text{m} \times 25.80 \mu\text{m}$ owing to Fig. 11, which shows the layout of the proposed TDA. The TDA consumes 0.74 mW under 1.1-V supply voltage. The post layout simulation exhibits the proposed TDA, which has 118 ps dynamic range and gain of six. Non-ideal environment with process, voltage and temperature (PVT) variations will further degrade the accuracy and linearity. To test the stability of the TDA to procedures variations, corners analysis was performed. Figure 12(a) exposes the gain error in fast PMOS and NMOS process. According to the fact that the delay is reduced in this progressions corner, the delay of the delay lines is diminished, which leads to the decrement

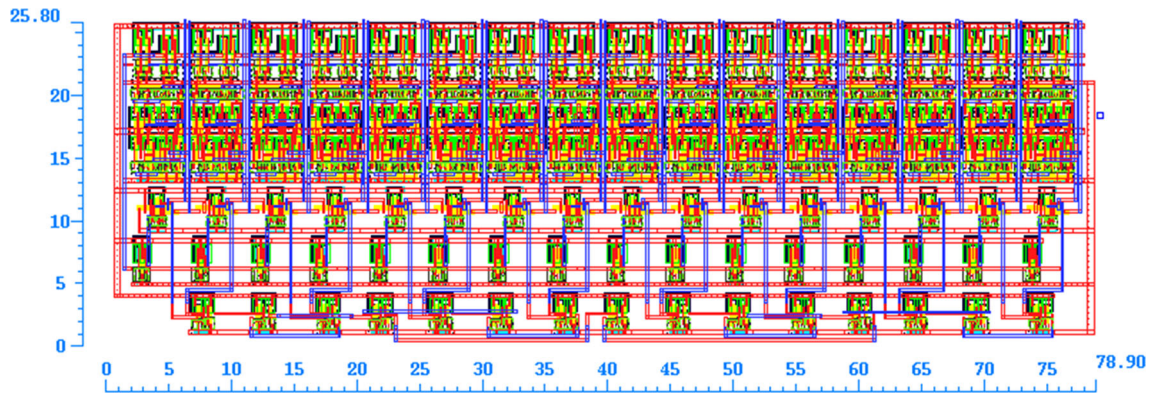


Fig. 11 The layout of the proposed TDA

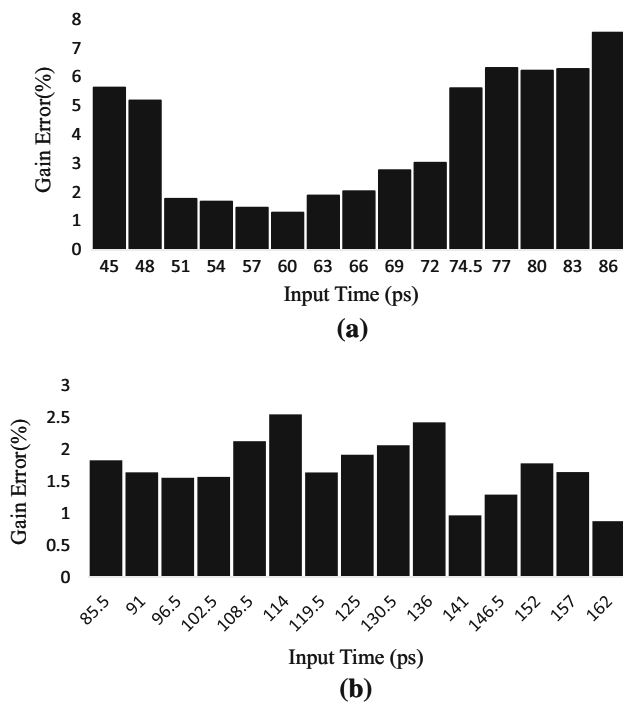


Fig. 12 a Gain error in FF process b gain error in SS process

of the dynamic range. It should be noted that the error of the previous stages accumulates and consequently increases the gain error of the last stages and the maximum gain error is 8%.

Figure 12(b) represents the gain error in slow PMOS and NMOS process (SS). In this process corner, the delay of delay lines is increased, which culminates in the increment of dynamic range. Even though the accumulation of the prior stages errors augments the total error, the increment of pulse width reduces the gain error percentage as it is stated in (8). Therefore, the gain error percentage in this process corner is decreased and maximum gain error is equal to 2.6%.

To estimate the temperature sensitivity, the gain error according to the input time difference was calculated through simulation at temperature in $-40\text{ }^{\circ}\text{C}$ and $+80\text{ }^{\circ}\text{C}$ under 1.1 V supply voltage. Figure 13(a) presents the gain error at $-40\text{ }^{\circ}\text{C}$ and Fig. 13(b) presents the gain error at $+80\text{ }^{\circ}\text{C}$ temperatures. Thanks to this figure, it can be concluded that the lessening of temperature creates the reduction of buffers delay in delay lines, which culminates in the increment of gain error at preceding stages. In the final stages, the collected error from the previous stages enhances the delay and the reduction of temperature decreases the delay; thus, the gain error will decline. Increase temperature to $80\text{ }^{\circ}\text{C}$ causes the last stages have large gain error since both enlarging temperature and

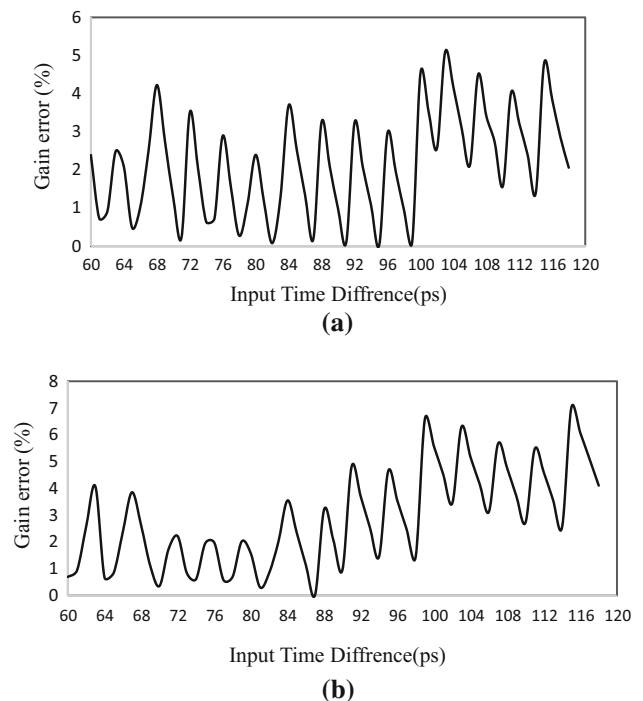
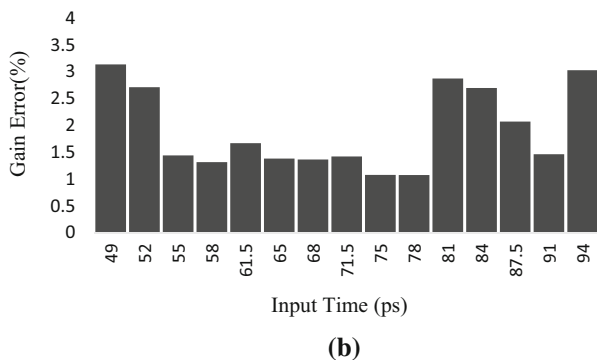
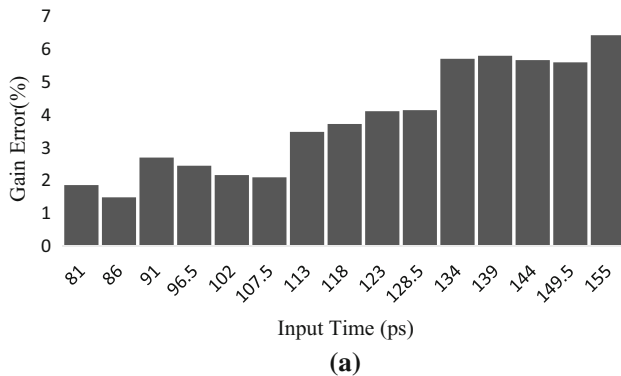


Fig. 13 a Gain error in $-40\text{ }^{\circ}\text{C}$ b gain error in $+80\text{ }^{\circ}\text{C}$

Table 1 Comparison TDA

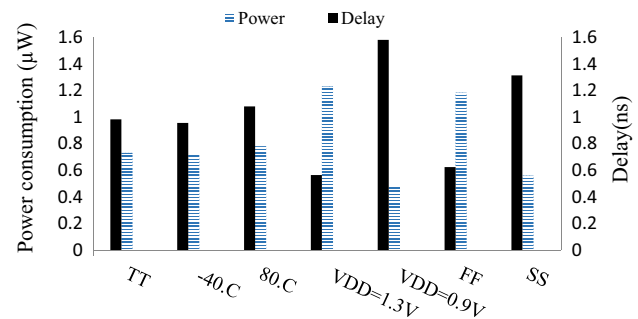
	Reference [25]	Reference [24]	Reference [20]	This work
Gain	4	2	80	6
Max gain error	8%	8%	4.1%	5%
Input range	1.5 ns	100 ps	225 ps	118 ps
Power consumption	–	–	1.7 mW	0.74 mW
Area	–	–	0.559 mm ²	0.74 mW
Supply voltage	–	1.8 V	1.8 V	0.002 mm ²
Technology	0.35 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	65 nm CMOS

**Fig. 14** a Gain error in 0.9 V VDD b gain error in 1.3 V VDD

accumulated error from the previous stages produces delay rise; therefore, the gain error will boost.

To assess the sensitivity of TDA to supply voltage the circuit is resembled under 0.9 V and 1.3 V supply voltages. Figure 14(a) represents the gain error under 0.9 V supply voltage at room temperature (27 °C). The reducing of the supply voltage increases the delay of the delay lines and consequently enhances the dynamic range. Based on these supply voltages, the total error of the last stages is boosted due to the gathered gain error of the previous stages. Figure 14(b) represents the gain error under 1.3 V supply voltage at room temperature (27 °C). The increasing of the supply voltage improves the pace of the circuit and consequently reduces the delay of the delay lines.

Table 1 compares the function of the proposed TDA with the other similar tasks. The suggested TDA has

**Fig. 15** Power consumption and delay

0.74mW power consumption under 1.1 V supply voltage. Figure 15 presents the power dissipation and circuit delay at process corners versus, various temperature and supply voltages. According to Fig. 15 the power waste is enhanced by the reduction of temperature and increase of supply voltage. In addition, the power dissipation is boosted for FF process corner. The power consumption is diminished by enhancing of temperature and decreasing of supply voltage and SS procedure corner. The delays for assorted situations are presented in Fig. 15. At FF progression corner under 1.3 V supply voltage and – 40 °C temperature, the delay is decreased, while at SS method corner and 80 °C temperature under 0.9 V supply voltage, the delay is augmented.

4 Conclusion

TDA is utilized for enhancing the resolution in TDC. An all-digital TDA based on delay lines has been recommended in this investigation. The proposed TDA harnesses three delay lines with various delays for create amplified output. The proposed TDA simulated in 65 nm CMOS procedure has a minus chip size of 0.002 mm² and generates gain of six with maximum gain error, which is about 5%. Under 1.1 V supply voltage, the circuit consumes 0.74 mW.

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