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MOS-only polyphase filter with small chip area

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Abstract
In this paper, it is aimed to realize a systematic approach for the realization of the MOS only complex polyphase filters which occupy small chip area. For this purpose, we used a technique based on adding cross-coupled transistors realizing local positive feedback, which, in turn, increases filter time constants. Thanks to this method, a substantial reduction in the filter chip area is achieved without having to use bulky on chip capacitors. The usefullness of the approach is validated by comparing the layouts of the designed CMOS circuit with the conventional RC polyphase filter. Post-layout simulation results using SPECTRE in CADENCE design environment are provided to verify feasibility of the proposed complex filter.

Keywords Analog CMOS circuit design · Analog filters · Complex filters · Communication circuits

1 Introduction

Heterodyne and low IF receivers suffer from the image problem, in which an image signal superimposes the desired signal, degrading the overall system performance. Low-IF transceivers suffer from the presence of image signals, caused by the down-conversion operation realized by a complex mixing. Unfortunately, the conventional real filters have not the capability for removing these undesired signals due to their symmetrical response around dc. The complex filters have been introduced to overcome this problem [1]. This kind of filters are constructed from two-path networks, where a pair of signals with equal amplitudes and quadrature phases (I and Q channels) are applied at their inputs. Complex signal processing is formally described in the literature (see [1–3] and the references cited therein).

RC Polyphase filter which can be considered as a complex filter is used in the low-IF wireless receiver to filter out the image signal [2, 3]. However, from IC realization point of view, RC Polyphase filters has some important drawbacks. The time constants of these filters can not be set accurately due to tolerances of the passive components in integrated circuit environment. On the other hand, these filters are designed to suppress image signals at low frequencies, thus requires large capacitors which occupy large chip area [4–13].

From the other side, MOS-only active filters which do not employ the on-chip bulky capacitors has attracted some interest recently [14–18]. This kind of filters offer some important advantages from IC realization point of view such as [19–21]:

1. MOS transistor provides higher capacitance density compared to conventional metal-plate capacitors.
2. MOS-only filters operate well at high-frequency region, owing to the fact that gate capacitances, the largest intrinsic device capacitor are considered during the design of the filters.
3. electronic tuning property of the important filter parameters, since the time constants are function of device transconductances which are controlled by biasing currents.

On the other hand, MOS-only active filters suffer from an inherent low frequency limitation. For achieving low frequency of operation, a design technique is applied to the MOS-only polyphase filter. Thus the obtained modified filter achieves the operating towards lower frequency region.

In this paper, the design of a MOS-only polyphase filter using cross-coupled MOS transistor pairs is presented [22, 23]. In this way, the operating frequency of the

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modified filter is decreased without using any bulky on chip capacitors. In order to reveal the advantages of the proposed circuit in terms of the chip area occupied, layouts of the classical passive polyphase filter and the proposed MOS-only polyphase filters are obtained [24]. It is found that, the proposed filter achive an area saving of 72%. Finally, in order to demonstrate the usefullness of the theoretical approach, simulation results are obtained using Spectre simulator in Cadence design environment.

2 Image problem and the use of polyphase filters for image rejection

The superheterodyne radio receiver is an important type of architecture widely used in various communications applications. One important issue associated with the superheterodyne radio is the image problem.

The image problem is illustrated in Fig. 1. This issue arises from the fact that two different signals can be translated to the same intermediate frequency region of the receiver. To achieve this issue, the receiver should provide some amount of image rejection. The image rejection of a receiver is specified as the ratio between the wanted and image signals expressed in decibels (dB) at the intermediate frequency.

The image interference problem becomes very challenging for low-IF receivers.

A possible solution is to use a complex polyphase filter. The conventional polyphase filter realized using passive elements is given in Fig. 2.

Assuming that the complex transfer function is defined as,

$$H(\omega) = \frac{I_{out} + jQ_{out}}{I_{in} + jQ_{in}}$$

the analysis of the circuit in Fig. 2 yields

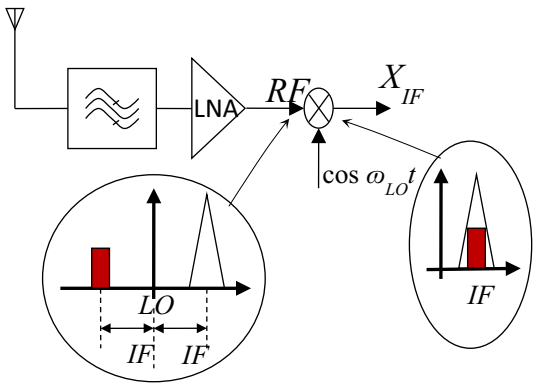


Fig. 1 Image problem in conventional RF receivers

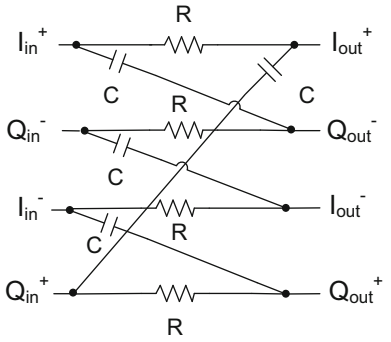


Fig. 2 First-order RC polyphase filter

$$H(\omega) = \frac{1 + \omega RC}{1 + j\omega RC} \tag{1}$$

Note that the filter provides unsymmetrical characteristics, i.e. $H(\omega) \neq H(-\omega)$.

Thus, the filter magnitude can be expressed as follows:

$$|H(\omega)|^2 = 1 + \frac{2\omega RC}{1 + (\omega RC)^2} \tag{2}$$

which shows that for positive frequencies, its magnitude remains between 0 and 3 dB, while for negative frequencies, the magnitude function has a zero at $\omega = -1/RC$. Therefore, the circuit in Fig. 2 can be used as an image reject filter.

3 Realization of MOS-only polyphase filter

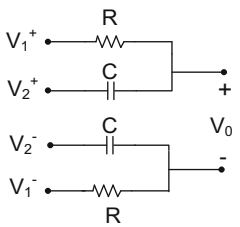
3.1 Synthesis procedure

The basic topology used as the basic block of the polyphase filter is shown in Fig. 3. The passive polyphase circuit mentioned above consists of two parts, the phase and the quadrature phase. The active-only equivalent of the passive polyphase filter can be obtained by using the subcircuits shown in Fig. 3.

The transfer function of the passive subcircuit is determined as follows:

$$V_0 = \frac{1}{1 + sRC}\left(V_1^+ - V_1^-\right) + \frac{sRC}{1 + sRC}\left(V_2^+ - V_2^-\right) \tag{3}$$

Fig. 3 Basic RC subcircuit



Note that in case of $V_1^+ - V_1^- = V_{in}$ and $V_2^+ - V_2^- = -jV_{in}$, i.e. quadrature signals are applied to the filter, we obtain the function in (1). This also shows that: The desired signal with positive frequency falls in the filter's passband while the image signal at negative frequency is suppressed.

The proposed general allpass topology is given in Fig. 4(b). The circuit (small-signal) transfer function is given by:

$$\frac{V_{out}}{V_{in}} = 1 - \frac{g_{m1}}{Y} \tag{4}$$

In order to realize the MOS-only polyphase filter, the circuit simulating parallel RC impedance is to be obtained. The MOS-only simulator of parallel RC circuit is shown in Fig. 5.

As it can be seen from the circuits, the equivalent MOS-only circuit of the parallel RC impedance is to be obtained. It is easy to verify that these active-only circuit realizes the desired function with: $R = 1/g_{m2}$, $C = C_{gs2}$.

In order to realize MOS-only equivalent of the passive RC subcircuit, it is proposed a MOS-only polyphase filter which realizes highpass and lowpass type characteristics simultaneously. These circuits are shown in Fig. 6.

As it can be seen from the circuit, the low pass and high pass filter functions are also achieved. Hence the passive subcircuit in Fig. 3 is implemented as MOS-only circuit. This circuit realize the transfer function as follows:

$$V_{out} = \left(1 - \frac{g_{m1}/C_{gs}}{s + g_{m2}/C_{gs}}\right) V_2^+ - \frac{g_{m3}/C_{gs}}{s + g_{m2}/C_{gs}} V_1^- \tag{5}$$

Note that, proposed MOS-only circuit realizing the RC subcircuit is given in differential mode; hence the circuit also enjoys all the advantages of differential-mode of operation.

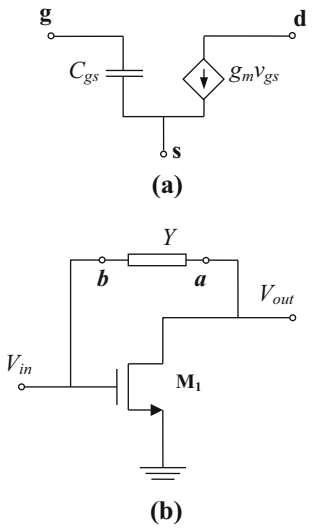


Fig. 4 **a** Simplified small-signal device model used in the filter synthesis. **b** General polyphase filter topology [25]

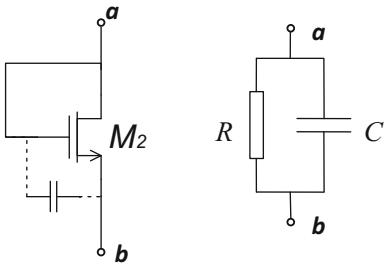


Fig. 5 Simulator of a parallel RC circuit [25]

The MOS small-signal model and the subcircuits shown in Fig. 6 are used in the synthesis prosedure of the proposed active-only polyphase filter. The small-signal transfer function is obtained by:

$$V_0 = \frac{g_{m3}/g_{m2}}{1 + sC_{gs}/g_{m2}}\left(V_1^+ - V_1^-\right) + \left(1 - \frac{g_{m1}/g_{m2}}{1 + sC_{gs}/g_{m2}}\right)\left(V_2^+ - V_2^-\right) \tag{6}$$

where C_{gs} is the intrinsic gate capacitance and g_{m2} is the small-signal transconductance of the transistors. Provided that all transistors' transconductances are equal, the expressions in (3) and (6) are identical and the MOS-only circuit in Fig. 7 simulates the RC subcircuit in Fig. 3.

3.2 Effects of parasitics

So far, in order to simplify the design of the filters, we have considered the simplified MOSFET model in Fig. 4(a), while the effects of the other parasitics are not taken into account.

When the parasitic capacitances of the MOS transistor are considered, the transfer function of the circuit is reobtained. The overlap (C_{gd}) capacitances are negligible since they are very small compared to other parasitic capacitances, and the effect of the bulk capacitors (C_{db} and C_{sb}) is taken into account during the systhesis procedure.

Hence the transfer function is obtained as follows:

$$V_{out} = \left(1 - \frac{g_{m1}/(C_{gs} + C_p)}{s + (g_{m2} + g_o)/(C_{gs} + C_p)}\right) V_2^+ - \frac{g_{m3}/(C_{gs} + C_p)}{s + (g_{m2} + g_o)/(C_{gs} + C_p)} V_1^-$$
$$C_p = (C_{db1} + C_{sb1} + C_{db3} + C_{sb3}) \text{ and } g_o = g_{ds1} + g_{ds3}. \tag{7}$$

Note that by predistorting the values of the capacitor C_{gs} and transconductance g_{m2}, the effects of the parasitics can be reduced.

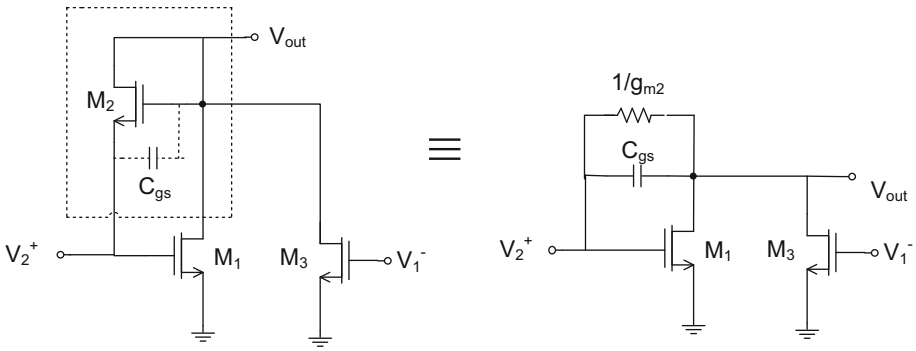


Fig. 6 MOS-only simulator of high-pass and low-pass characteristic

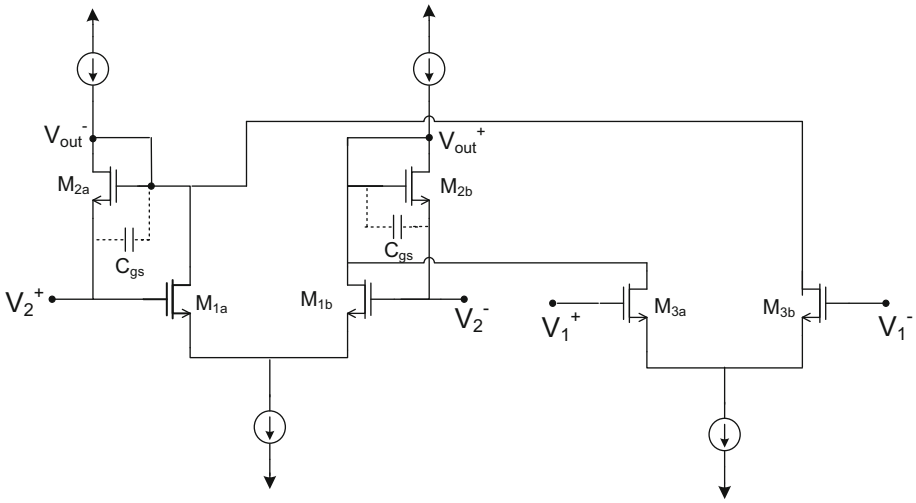


Fig. 7 Proposed MOS-only circuit realizing the RC subcircuit in Fig. 3

3.3 Implementation of image-reject polyphase filter

In order to compose the active only equivalent circuit of the RC subcircuit shown in Fig. 3, the possible procedure is described in Fig. 8. As it can be seen clearly from this figure, the active-only polyphase filter can be obtained accordingly by interconnecting two of the subcircuits in Fig. 7.

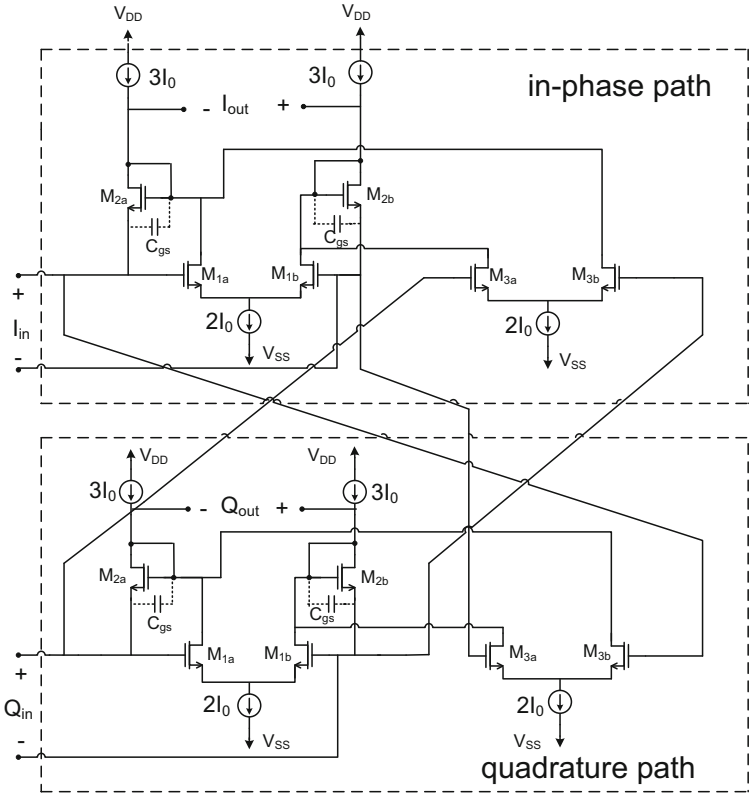
It is clear that, the center frequency of the complex bandpass filter is obtained such as: $\omega_0 = g_{m2}/C_{gs}$. It can be seen that, a filter with all key parameters are electronically adjustable. It should be note that, the lack of passive capacity and resistance elements in the circuit design has significantly reduced the area covered by the filter.

In the circuit, all biasing currents are 7.5 μA except for the tail currents which are 5 μA and using these parameter values, the center frequency is measured as 12.8 MHz. The dimensions of MOS transistors in the circuit are shown in Table 1.

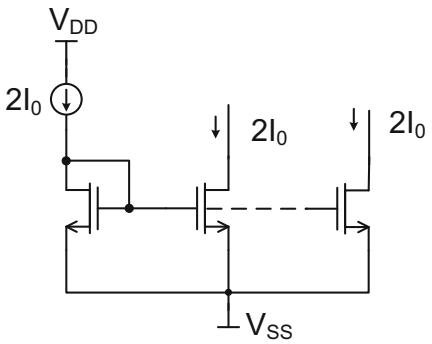
With these biasing conditions, the value of parasitic gate-source capacitances and transconductances of the transistors were calculated as $C_{gs2} = 600$ fF and $g_{m2} = 50$ μA/V. Using these values in the expression in Eq. (6), the center frequency is calculated as $f_o = 13.2$ MHz. On the other hand, from the characteristics given in Fig. 9, the filter center frequency is calculated as 12.8 MHz, which agrees well with the value derived from theoretical expressions.

In addition to that, in application where necessary image rejection ratio is required, the designed first-order polyphase filter can be used in cascade configuration to realize second order polyphase filter.

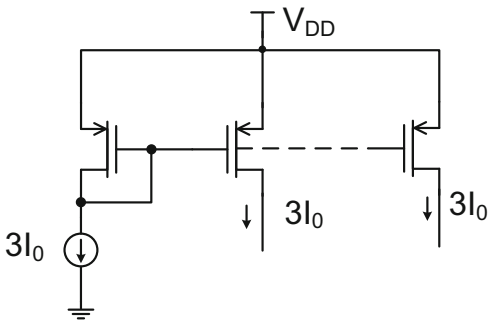
As it can be seen from the Fig. 10, in accordance with theoretical value the image reject ratio is found to be approximately 60 dB. On the other hand, the magnitude is about 6 dB at positive frequencies.



(a)



(b)



(c)

Fig. 8 **a** Implementation of the MOS-only polyphase filter realizing the RC subcircuit in Fig. 3. **b** Realization of NMOS current mirrors. **c** Realization of PMOS current mirrors

Table 1 Dimensions of MOS transistors

$M_{1a,b}$	12 μm/1 μm
$M_{2a,b}$	48 μm/4 μm
$M_{3a,b}$	12 μm/1 μm
All NMOS in Fig. 8(b)	12 μm/1 μm
All PMOS in Fig. 8(c)	30 μm/1 μm

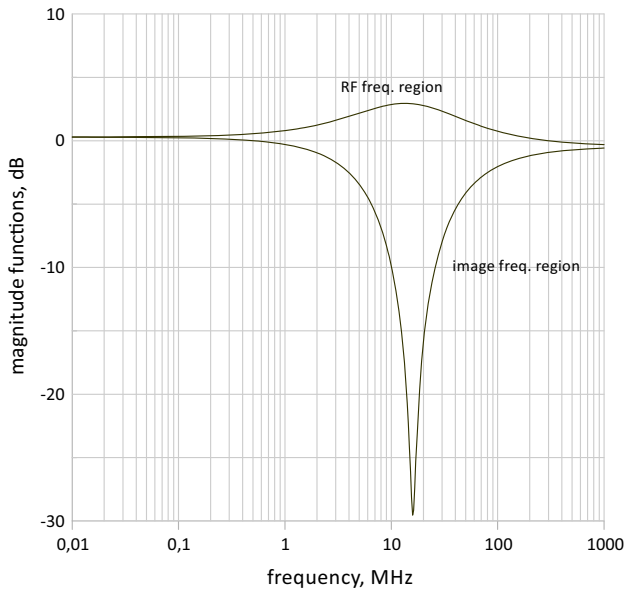


Fig. 9 Simulation result of first order MOS-only polyphase filter

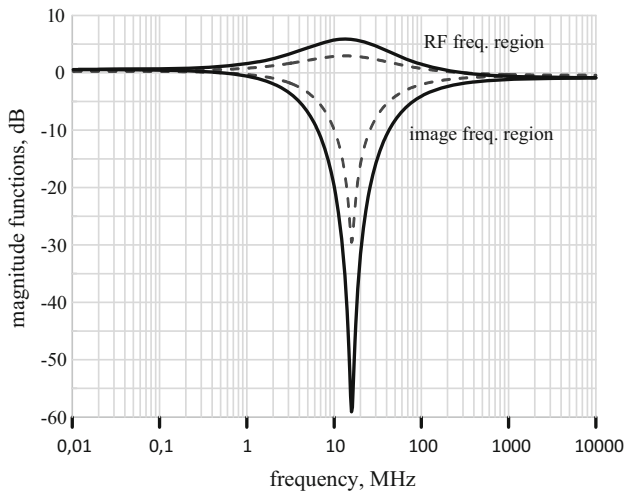


Fig. 10 Magnitude characteristics of first order (dashed line) and second order (solid line) MOS-only polyphase filters

4 Proposed technique based on adding cross-coupled transistor pairs for low frequency MOS-only filter

In low IF circuits, the low frequency RC circuit occupies too much space on the chip. Since capacitance and resistance are not used in MOS-only circuits, this kind of filters provides substantial area advantage in contrast to the passive RC circuits.

On the other hand, for achieving low natural frequencies, either the value of g_m, i.e. MOS biasing current should be decreased or the value of C_{gs} should be increased. However, MOS biasing current can not be decreased below a specific value at which the transistor enters the subthreshold regions where filter suffers from large distortion due to the governing transistor's exponential nonlinearity. On the other hand, to increase the value of C_{gs} implies the use of large devices that increase the chip area occupied by the circuits.

In order to overcome this problem, it is used a technique which is based on adding a cross coupled MOS transistor pairs, M_{jp} and M_{jn}. Provided that $(W/L)_{jp} = K(W/L)_{ip}$ and $(W/L)_{jn} = K(W/L)_{in}$, or equivalently $gm_{ip} = gm_{in} = Kgm_{jp} = Kgm_{jn}$, the filter's new pole is obtained as $\hat{f}_p = f_p(1-K)$ where the value of K is nonnegative and less than unity. As it can be seen from Fig. 11, this shows that by applying this technique, the filter's pole frequency is reduced by a factor of $1-K$.

It is considered the filter shown in Fig. 8 to indicate the usefulness of the idea. Assuming that all MOS transistors operate in saturation region, transconductances from the body effect, gate drain overlap capacitances, C_{gd} and parasitic junction capacitances C_{sb} and C_{db} of the devices are neglected. The modified circuit is obtained as shown in Fig. 12 according to the technique described above.

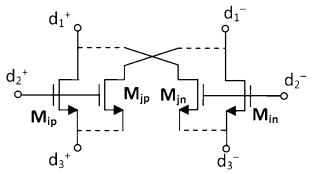


Fig. 11 The cross coupled MOS transistor technique for realizing low frequency filters [23]

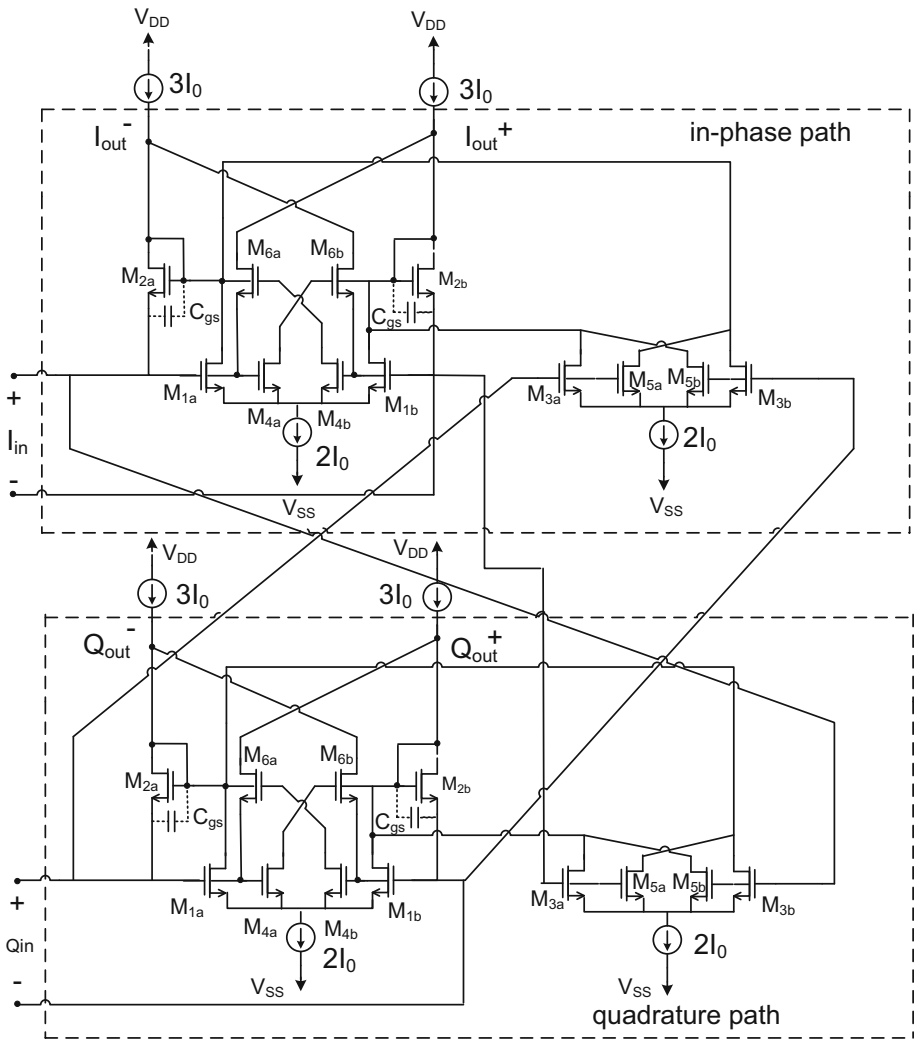


Fig. 12 MOS-only polyphase filter obtained according to the proposed technique

Routine analysis of the circuit yields the following transfer function:

$$V_0 = \frac{g_{m3}(1-K)}{g_{m2}(1-K)+sC_{gs}(1+K)}\left(V_1^+ - V_1^-\right) + \left(1 - \frac{g_{m1}(1-K)}{g_{m2}(1-K)+sC_{gs}(1+K)}\right)\left(V_2^+ - V_2^-\right) \tag{8}$$

where $K = g_{m6}/g_{m2} = g_{m4}/g_{m1} = g_{m5}/g_{m3}$. In the new case, the filter pole frequency is now given by:

$$\omega_0 = \frac{g_{m2}(1-K)}{C_{gs2}(1+K)} \tag{9}$$

It should be noted that the filter frequency is actually modified by a factor of $(1–K)/(1 + K)$. This is due to fact that gate capacitances of the cross-coupled transistors appear in parallel with the existing gate capacitors and increase the total capacitance in the circuit. In order to test the feasibility of the proposed technique, it is obtained simulation result of the modified filter in Fig. 13 by choosing $K = 0.75$.

5 Post-layout simulation results

In order to show the feasibility of the modified filter, the layouts of the circuits were drawn and their areas occupied on the chip were calculated. The filters were simulated using Spectre simulation tool in Cadence design environment using the parameters of AMS 0.35 μm CMOS pro-

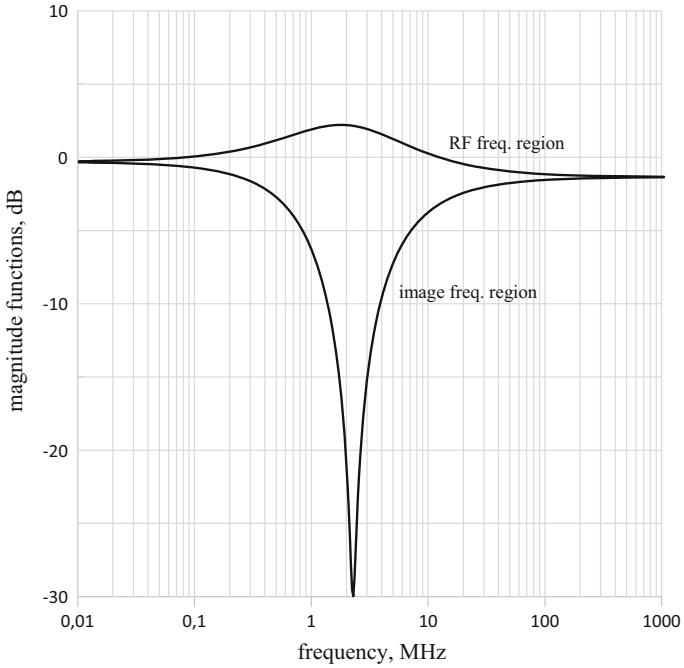


Fig. 13 Magnitude characteristics of the modified filters showing that the natural frequency is 1.8 MHz without using any bulky on-chip capacitors ($K = 0.75$)

cess. The initial and modified filters shown in Figs. 8 and 12 were biased with ± 1.65 V DC power supply and all the current sources were realized using simple CMOS current mirrors.

In the modified circuit, the factor K is set to be 0.75 by adjusting the transistor dimension ratios and the center frequency is measured as 1.8 MHz. The circuit area is measured as 9184 μm^2. In order to show the advantages of the active filter compared to the filter realized using any bulky on-chip capacitors, the circuit is redesigned using on-chip capacitors with the same center frequency of 1.8 MHz. The chip area occupied by the integrated circuit is determined as 32,490 μm^2 at this time. It is much larger than the above active only filters. This comparison shows the benefits of the active only filters and the proposed method. From the filters' layouts, it is found that an area saving of 72% is achieved using the proposed technique. The layouts of the circuits are shown in Fig. 14(a, b).

Note that a number of MOS-only filters have been presented in the literature. Among these, the one in the [18] is appealing due its very simple topology. In order compare the proposed complex filter with this circuit, we have used a figure of merit. Note that the proposed complex filter processes two channels, i.e. in-phase and quadrature phase channels, while the filter in the reference is meant to process a single channel. In a possible complex filtering application, two of the filters given in the reference should be used. Therefore, it is more appropriate to compare the proposed circuit based on a figure of merit normalized to the number of channel.

Therefore, the figure of merit is proposed here as

$$FOM = \frac{chip - area \times power - dissipation}{channel \times filter - order^2}$$

Note that with this chip area and power dissipation are both evaluated as per pole and per channel. According to the above equation, FoM values are obtained respectively for the proposed complex filter and the filter in [18] as 91 [$(\mu m)^2$ mW] and 301 [$(\mu m)^2$ mW].

As can be seen from these results, the proposed complex filter circuit is much more advantageous in terms of area.

6 Conclusions

In this paper, a MOS-only polyphase filter having a simple topology with electronically adjustable filter parameters is presented. In order to verify the usefulness and feasibilities of the circuit, Cadence Spectre simulation results are provided. The proposed MOS-only polyphase circuit suffer from an inherent low frequency limitation. In order to address this issue, the modification techniqe allowing the derivation of MOS-only filter which allows extension of the operating frequency towards lower frequency region is used. This technique based on using cross-coupled MOS transistor pairs. Detailed simulations results of the filters modified according to the this technique are also provided in order to verify the usefulness of the theoretical approach.

Finally, in order to demonstrate the usefullness of the approaches, first order polyphase filter pole frequency as

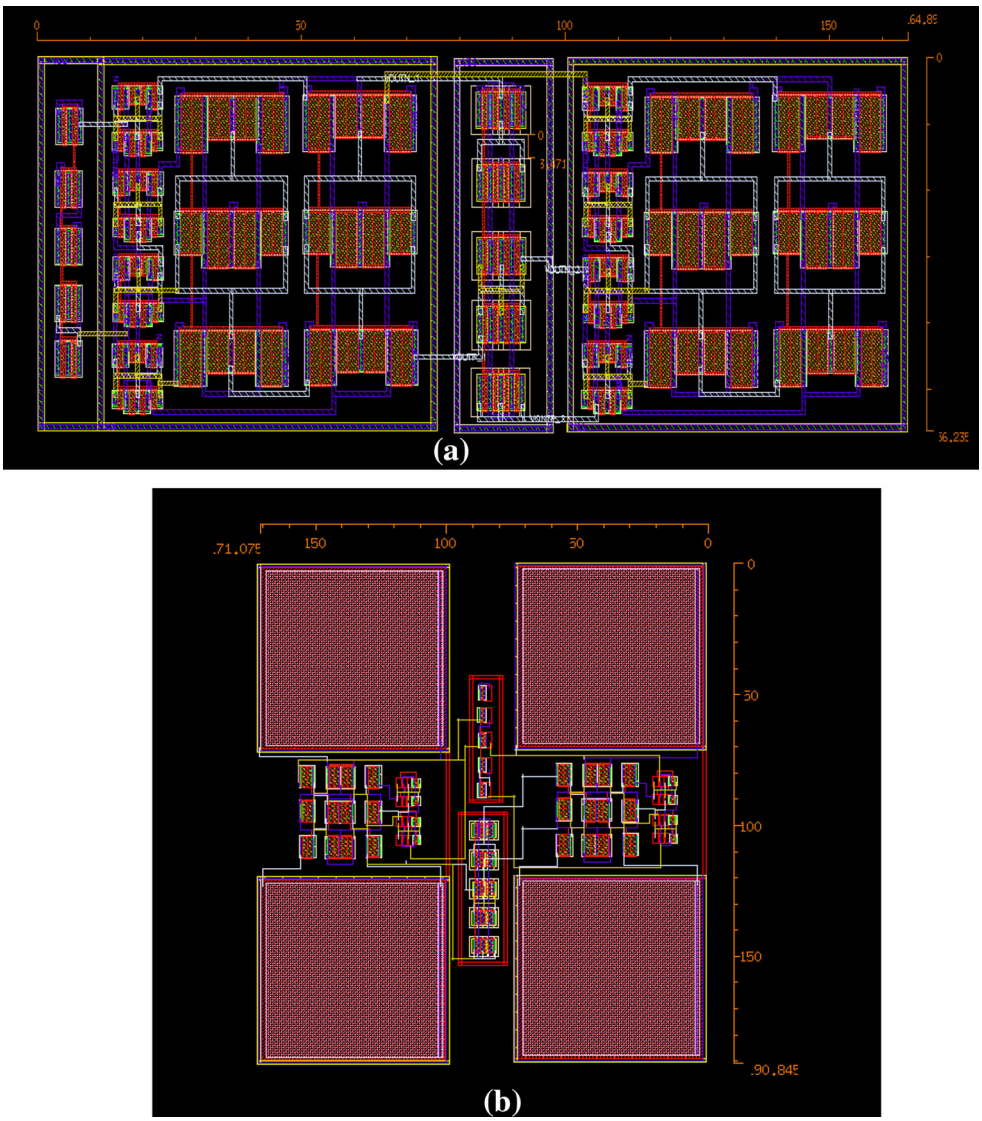


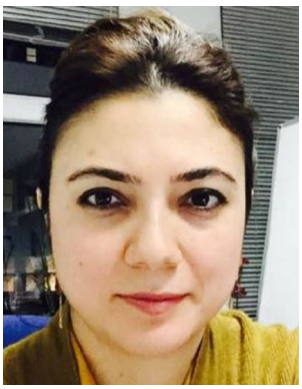
Fig. 14 **a** The layout of modified circuit based on adding cross-coupled transistor pairs (f_0 = 1.8 MHz), **b** the layout of the circuit redesigned using on-chip capacitors (f_0 = 1.8 MHz)

low as 1.8 MHz is obtained by using the cross coupled MOS-transistor technique. The layouts of the filters were drawn and their areas occupied on the chip were calculated. The filters were simulated using Spectre simulation tool in Cadence design environment using the parameters of AMS 0.35 μm CMOS process.

References

1. Wenin, J. (1994). IC's for digital cellular communication. In *Proceedings of the. ESSCIRC, Ulm* (pp. 1–10).
2. Sedra, A., Snelgrove, W., & Allen, R. (1995). Complex analog bandpass filter designed by linearly shifting real lowpass prototypes. In *Proceedings of the IEEE international symposium on circuits and systems* (pp. 1223–1226).
3. Minnis, B., & Moore, P. (2002). Non-complex signal processing in a low-IF receiver. *IEE Proceeding-Circuits, Devices and Systems, 149,* 322–330.
4. Behbahani, F., Kishigami, Y., Leete, J., & Abidi, A. A. (2001). CMOS mixers and polyphase filters for large image rejection. *IEEE Journal of Solid State Circuits, 36,* 873–887.
5. Behbahani, F., Leete, J., Kishigami, Y., Roithmeier, A., Hoshino, K., & Abidi, A. A. (2000). A 2.4 GHz low-IF receiver for wideband WLAN in 0.6 μm CMOS architecture and front-end. *IEEE Journal of Solid State Circuits, 35,* 1908–1916.
6. Galal, S. H., Ragaie, H. F., & Tawfik, M. S. (2000). RC sequence asymmetric polyphase networks for RF integrated transceivers. *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 47,* 18–27.
7. Haddad, F., Zaid, L., & Frioui, O. (2000). *Polyphase filter design methodology for wireless communication applications*. London: INTECH Open Access Publisher.
8. Emira, A., & Sanchez-Sinencio, E. (2003). A pseudo differential complex filter for Bluetooth with frequency tuning. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 50,* 742–754.
9. Laoudias, C., & Psychalinos, C. (2010). Low-voltage Bluetooth/ZigBee complex filter using current mirrors. In *Proceedings of the ISCAS* (pp. 1268–1271).

10. Abuelmaatti, A., & Abuelmaatti M. T. (2005). A new active polyphase filter for image rejection using second generation current conveyors. In *Proceedingds of the 9th international conference on circ*uits (pp. 1–4).
11. Alzaher, H., & Tasadduq, N. (2009). A CMOS low power current-mode polyphase filter. In *Proceedings of the IEEE ınternational symposium on low power electronics design* (pp. 75–79).
12. Un, M. (2004). Implementation of polyphase filter section with CFAs. *Frequenz, 58,* 221–224.
13. Sagbas, M. (2011). Design of CDBA-based active polyphase filter for low—IF receiver applications. *Turkish Journal of Electrical Engineering and compurt Science, 19,* 565–574.
14. Thanachayanont, A. (2002). CMOS transistor-only active inductor or IF/RF applications. In *Proceedings of the IEEE International conference on Industrial Technology* (Vol. 2, pp. 1209–1212).
15. Karsilayan, A., & Schaumann, R. (2000). A high-frequency high-Q CMOS active inductor with DC bias control. In *Proceedings of the 43rd IEEE midwest symposium on circuits and systems* (Vol. 1, pp. 486–489).
16. Metin, B., Arslan, E., Herencsar N., & Cicekoglu, O. (2011). Voltage-mode MOS-only all-pass filter. In *Proceedings of the ınternational conference on telecommunications and signal processing* (pp. 317–318).
17. Arslan, E., Metin, B., Kuntman, H., & Cicekoglu, O. (2013). MOS-only second order current-mode LP/BP filter. *Analog Integrated Circuits and Signal Processing, 74,* 105–109.
18. Safari, L., Minaei, S., & Metin, B. (2014). A low power current controllable single-input three-output current-mode filter using MOS transistors only. *AEU International Journal of Electronics and Communications, 68,* 1205–1213.
19. Yuce, E., & Minaei, S. (2010). A novel phase shifter using two NMOS transistors and passive elements. *Analog Integrated Circuits and Signal Processing, 62,* 77–81.
20. Minaei, S., & Yuce, E. (2012). High input impedance NMOS-based phase shifter with minimum number of passive elements. *Circuits, Systems and Signal Processing, 31,* 51–60.
21. Razavi, B. (2012). *RF microelectronics* (2nd ed.). Upper Saddle River: Prentice Hall.
22. Yıldız, H. A., Toker, A., Kılınç, S., & Ozoguz, S. (2016). Low frequency active only filters with small chip area. *Analog Integrated Circuits and Signal Processing, 89*(3), 739–747.
23. Yıldız, H. A., Toker, A., Elwakil, A. S., & Özoğuz, S. (2014). MOS-only allpass filters with extended operating frequency range. *Analog Integrated Circuits and Signal Processing, 81*(1), 17–22.
24. Yıldız, H. A. (2015). MOS-only polyphase filter. In *Proceedings of the 10th international conference on electrical and electronics engineering (ELECO'2017), Bursa, Turkey* (pp. 1226–1229).
25. Yıldız, H. A., Özoğuz, S., Toker, A., & Çiçekoğlu, O. (2013). MOS-only allpass filters with extended operating frequency range. *Circuits, Systems and Signal Processing (CSSP), 32*(3), 1455–1465.



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