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MIXED SIGNAL LETTER

Energy-efficient switching scheme based on floating technique for SAR ADC

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Abstract
A high energy-efficiency capacitor switching scheme for successive approximation register (SAR) analog-to-digital converters is proposed in the paper. During the design procedure, the charge characteristic of the floating capacitor and the technique of splitting capacitor ensure zero energy consumption of switching operation. With the reset energy of capacitor arrays taken into account, the proposed switching scheme can achieve 100% less switching energy over the conventional switching scheme. Furthermore, this work also achieves about 50% area reduction with only two reference voltages. The behavioral simulation of the proposed SAR was performed, the maximum differential nonlinearity and maximum integral nonlinearity are 0.451 and 0.452 LSB respectively.

Keywords SAR ADC · Floating · Splitting capacitor · Reference voltages

1 Introduction

Nowadays successive-approximation register (SAR) analog-to-digital converters (ADC) are widely used in many research institutions due to its inherent low energy consumption characteristic. Typically, the total power dissipation of SAR ADC mainly derives from three parts: capacitor array, comparator and digital circuits. However, the capacitor array switching power dominates the total energy [1–3]. Therefore, many published switching schemes are used to reduce the energy dissipation. Compared with the conventional SAR switching scheme, the method of Tri-level [1] has achieved 96.9% energy reduction, others as the V_{cm}-based monotonic scheme [2] (VMS), Trade-off method [3], Tong [4] and Advanced energy-back [5] can achieve 97.66, 98.05, 98.83 and 99.4% respectively. However, the reset energy consumption was not considered in most of published works and the drawbacks of more than two reference voltages are ignored, neither. Based on the analysis and discussion in [5], the reset energy is a major part of the total energy dissipation. In this letter, the proposed energy-efficient switching scheme of SAR ADC not only takes the energy of switching scheme into consideration, but also the reset energy which has been introduced in [6]. Thus, the proposed switching scheme can achieve 100% less switching energy. Moreover, the C–2C structure is applied to improve the performance of linearity, here. Therefore, the proposed architecture and switching scheme has a significant improvement in energy consumption, area and linearity.

2 Proposed switching scheme

The floating technique is used to reduce the switching energy in [7]. Here we propose a single-ended switching transformation with floating technique, which reduce about half of the area and simplify the digital control complexity in comparison cycles. The proposed 10-bit DAC array has been shown in Fig. 1. The capacitor array contains two sides: p-side cap-array (capacitance array connecting the higher voltage potential side of the comparator) and n-side cap-array. Each side can be divided into two parts: C_{up} and C_{down}, which are exactly same. And each of them consists of a binary capacitor array, in which the large capacitor is

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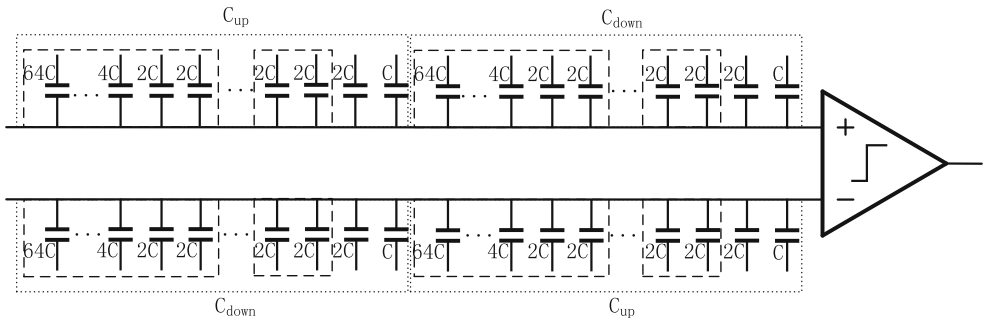


Fig. 1 Proposed 10-bit DAC capacitor array

split as follows: 4C = 2C + 2C, 8C = 4C + 2C + 2C, … $2^{N}C = 2^{N-1}C + \cdots + 4C + 2C + 2C$.

Resulting from the floating capacitor technique, the top plate voltage is different from the traditional switching scheme. As shown in Fig. 2(a), the first step is the initial sampling condition, while the conversion from the second step to the third step will be discussed in detail. If the bottom plate voltage of the C_{down}'s unit capacitor varies from floating to gnd, and the bottom plate voltage of the C_{up} stops floating and keep gnd. The voltage variation of the top plates can be described as follow:

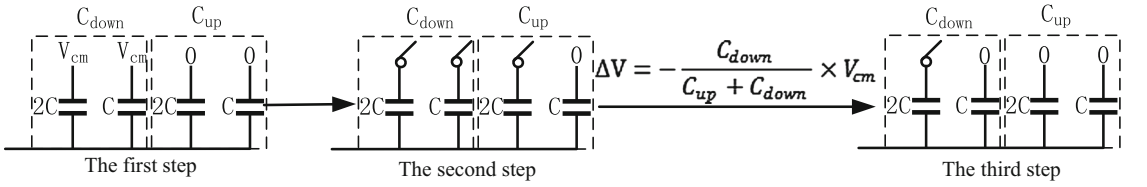
$$\Delta V = -\frac{C_{down}}{C_{up}+C_{down}} \times V_{cm} = -\frac{C}{3C+C} \times V_{cm} = -\frac{1}{8}V_{ref} \tag{1}$$

Note that only the non-floating capacitances are taken into account. Similarly, the voltage variation of the top plates in Fig. 2(b) can be given as:

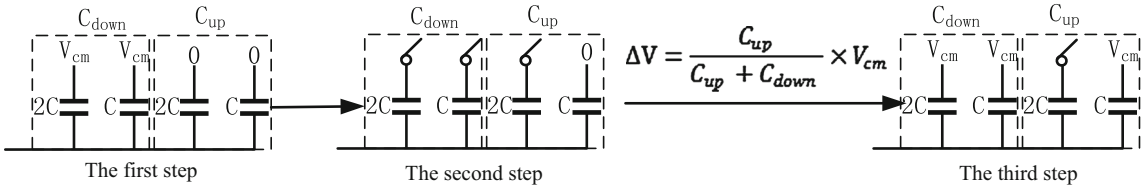
$$\Delta V = \frac{C_{up}}{C_{up}+C_{down}} \times V_{cm} = \frac{C}{C+3C} \times V_{cm} = \frac{1}{8}V_{ref} \tag{2}$$

As shown in Fig. 3, a 4-bit SAR ADC are used to explain the operational principle of the proposed switching scheme. Figure 4 shows the waveform of the proposed switching scheme. Considering the conversion between $V_{ip} > V_{in}$ and $V_{ip} < V_{in}$ are exactly the same, only the conversion of $V_{ip} > V_{in}$ is discussed in detail in the paper.

In the sampling phase, the top-plates of the capacitors directly sample the input signal, the bottom plate voltage of C_{up} connects gnd and C_{down} connects V_{cm}. After sampling, both bottom plate voltages of unit capacitors of C_{up} hold gnd, and other capacitors are floating, then the first comparison can be obtained directly. After that, as shown in Fig. 3, D_1 (D_n is the n-th output of the comparator) = 1, the bottom plate voltage of C_{up} for the n-side cap-array stops floating and sets to V_{cm}, therefore the second comparison can be obtained. Then the remaining voltage changes will happen to the p-side cap-array. If D_2 is 1, the floating unit capacitance of p-side cap-array sets to gnd; if D_2 is 0, the bottom plate voltage of two unit capacitances of p-side cap-array sets to V_{cm}, as a result we can get the third comparison result. If the case is A and D_3 = 1, the bottom plate voltage of the second smallest capacitor for C_{down} stops floating and sets to gnd; if D_3 = 0, the bottom plate voltage of the second smallest capacitor of C_{up} stops floating and sets to gnd. If the case is B and D_3 = 1, the bottom plate voltage of the second smallest capacitor for



(a) Calculation of the main change of C_{down}



(b) Calculation of the main change of C_{up}

Fig. 2 Illustration of the voltage calculation. **a** Calculation of the main change of C_{down}, **b** calculation of the main change of C_{up}

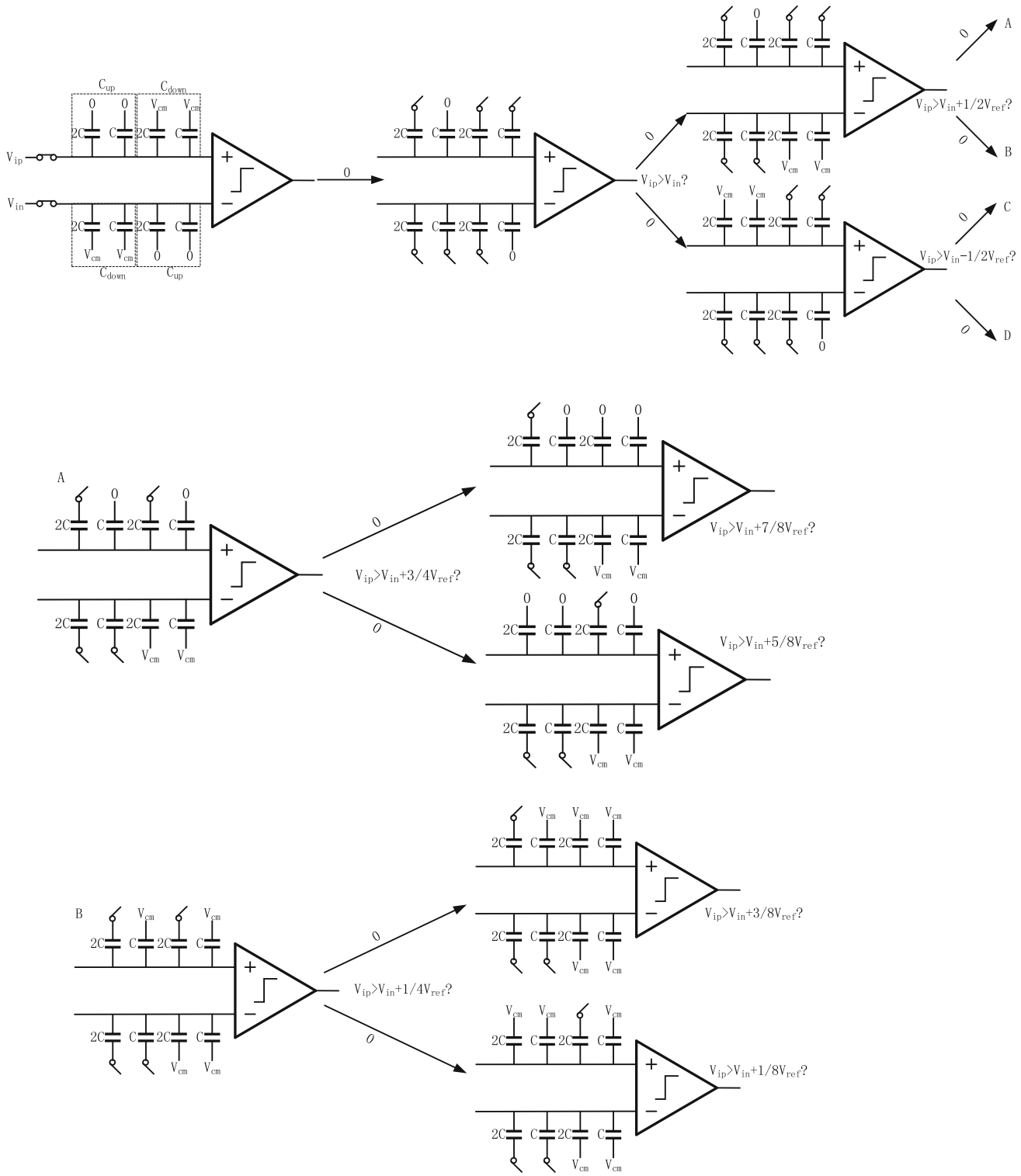


Fig. 3 Proposed capacitor switching scheme of 4-bit DAC

C_{down} stops floating and sets to V_{cm}; if $D_3 = 0$, the bottom plate voltage of the second smallest capacitor for C_{up} stops floating and sets to V_{cm}. Therefore the forth comparison can be obtained, and remained comparisons are similar to it.

As shown in Fig. 5(a), supposing the initial voltage of the top and bottom plates are V_{top}, V_{bottom} respectively. During the switching operation, the bottom plate voltages of floating capacitances changes with the fluctuation of

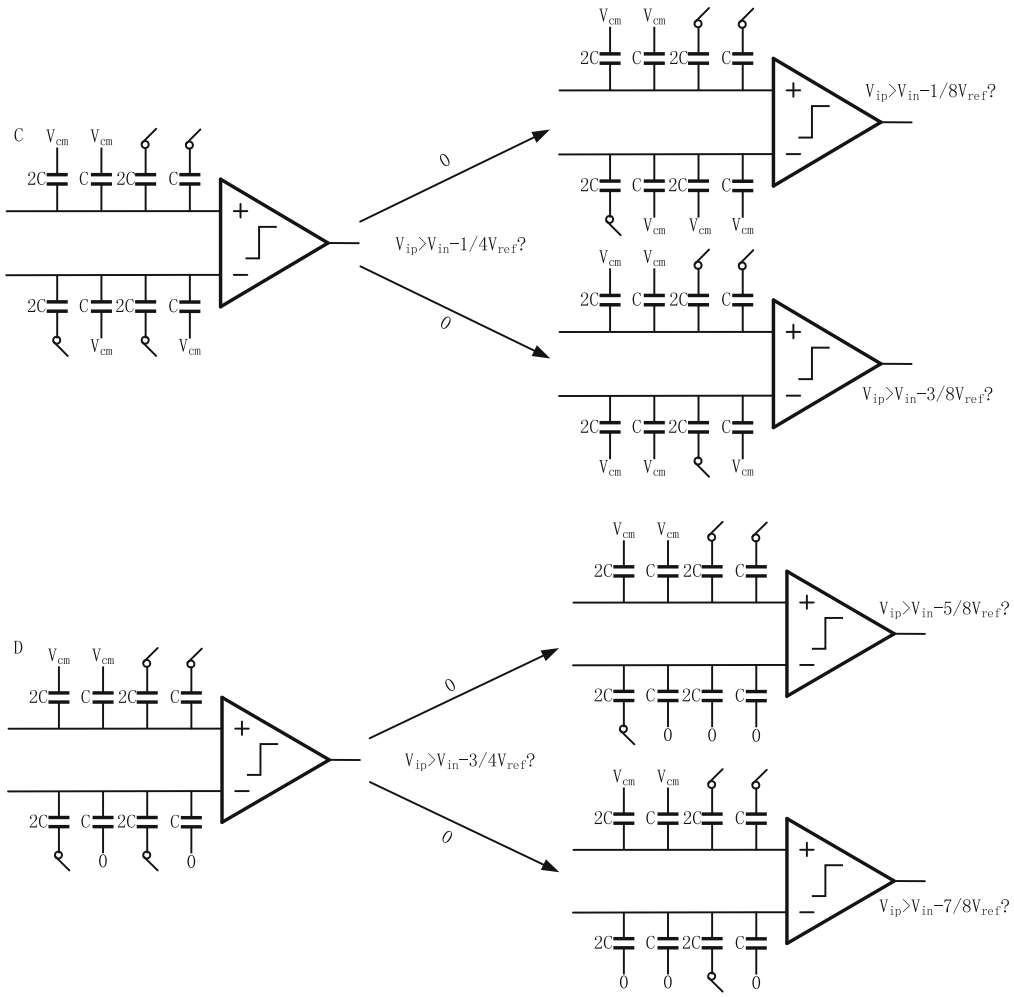


Fig. 3 continued

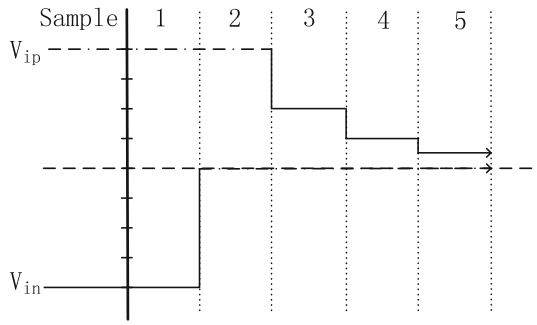


Fig. 4 Waveform of the proposed technique

voltages of the top part. The charge on the top plate of the C1 keep unchanged and it can be calculated as:

$$\begin{aligned} \mathrm{Q} &= \mathrm{C} \times \left[\left(V_{top} \pm \Delta \mathrm{V} \right) - \left(V_{bottom} \pm \Delta \mathrm{V} \right) \right] \\ &= 2 \times \mathrm{C}_u \times \left(V_{top} - V_{bottom} \right) \end{aligned} \tag{3}$$

where $\Delta \mathrm{V}$ is the voltage variation of the top plate. Resulting from (1), the voltage of the top plate in

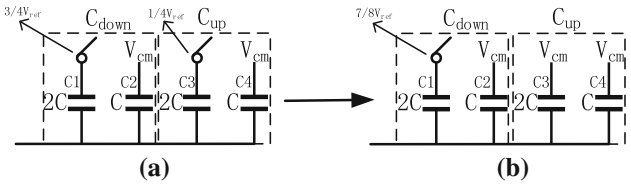


Fig. 5 Illustration of the energy consumption

Fig. 5(b) is $V_{top}+ 1/8V_{ref}$. It is clear that the charge of C1 is still unchanged, and C3's charge is transferred to C2 and C4 respectively. The energy calculation can be derived as:

$$\begin{aligned} E_{energy} &= -V_{cm} \times 2\mathrm{C}_u \times \frac{1}{8} V_{ref} + (-V_{cm}) \times 2\mathrm{C}_u \\ &\quad \times \left(\frac{1}{8} V_{ref} - \frac{1}{4} V_{ref} \right) \\ &= 0 \end{aligned} \tag{4}$$

Note that the above formula can be extended to the entire conversion process. Apart from the first conversion process and floating capacitors, two situations need to be considered: Firstly, the bottom plates of the whole capacitors are set to gnd, and the other all capacitors' bottom plates are set to V_{cm}. For the first case, it is clear that its power consumption is 0. For the second case, its energy consumption can be expressed as:

$$\begin{aligned} E_{energy} &= -V_{cm} \times 2^n C_u \times \left(\pm \frac{1}{2^{n+2}} V_{ref} \right) + (-V_{cm}) \\ &\quad \times 2^n C_u \times \left(\pm \frac{1}{2^{n+2}} V_{ref} \mp \frac{1}{2^{n+1}} V_{ref} \right) \\ &= 0 \end{aligned} \tag{5}$$

where $n = N - 2$ (N is the number of conversions) and $n \geq 2$, if $n = 1$, the conversion process obviously does not require any power consumption. In summary, there will be no power consumption in the entire conversion process.

3 Resetting switching scheme

Figure 6 shows the reset operation in this work. One side of the capacitor array is that C_{up} connects V_{cm} and C_{down} is floating, then all the capacitors of this side connect to V_{cm}, and the other side connects to gnd. Then the $C_{up}(C_{down})$ of p-side cap-array swaps with the $C_{down}(C_{up})$ of n-side cap-array, and the four identical capacitor arrays sample the input signal respectively. Once the sampling is completed, the original C_{down} of the cap-array will combine together. C_{up} is the same as C_{down} and it consume no power. The related method has introduced in [6].

Based on the behavior simulation result of switching energy, the inherent charge transfer characteristics of capacitors are served for the proposed switching scheme, it is clear that 100% total energy consumption has been saved over the traditional switching scheme.

4 Switching energy

The behavioral simulation of the proposed method and other 10-bit SAR's methods were performed in MATLAB. Figure 7 shows the switching energy comparison of 10-bit SAR ADC. Table 1 shows the comparison of switching technique for 10-bit SAR. The proposed switching scheme has no switching energy and reset energy, so it achieves 100% energy saving. Compared with other switching schemes, the proposed switching scheme only uses two reference voltages, while the switching schemes of Tri-level [1], VMS [2] and Trade-off [3] shown in Table 1, adopt three reference voltages.

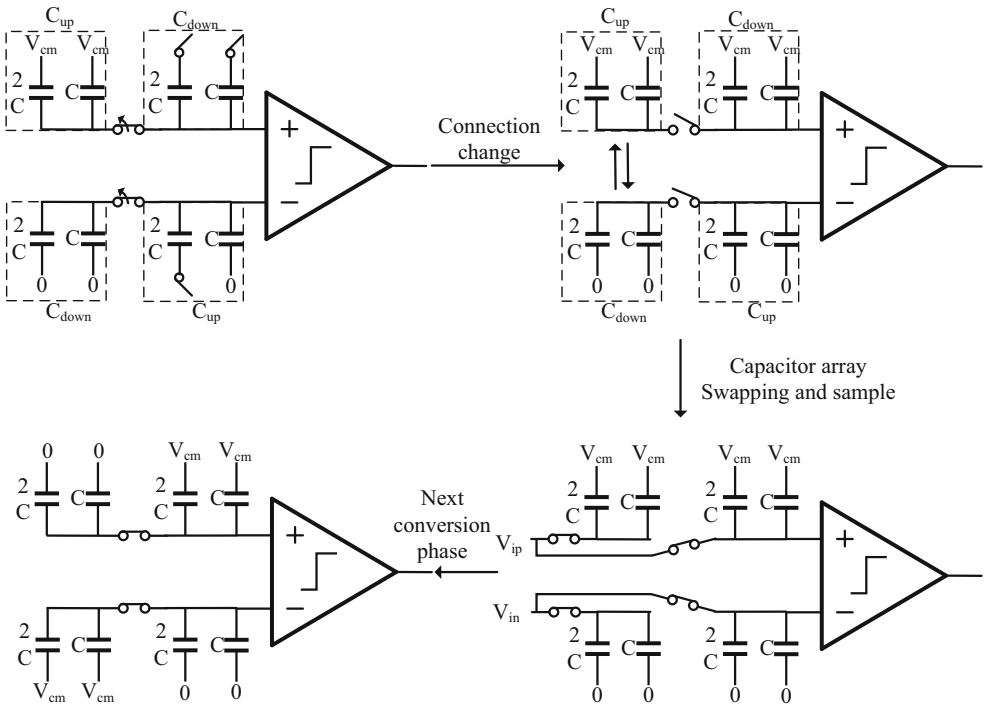


Fig. 6 Illustration of the reset switching

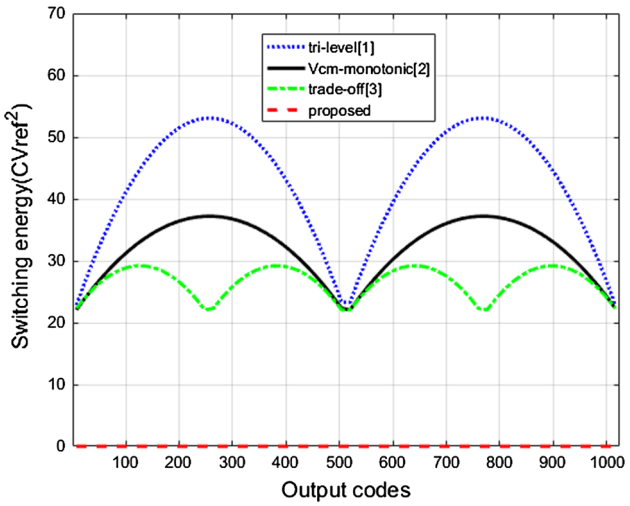


Fig. 7 Switching energy against output code

5 DNL and INL

There is no denying the fact that the mismatch of capacitors has effect on the switching scheme which is based on floating. Figure 8 shows the DNL and INL versus output code of the proposed switching scheme. The unit capacitance obeys Gaussian distribution in this simulation. The result of the simulation is 500 times Monte Carlo operations of 10-bit SAR ADC which adopts the proposed scheme. Assuming that the unit capacitance is C_u, the deviation is $0.01(\sigma(\Delta C/C_u = 0.01))$. The reason for the largest error is the maximum deviation of the first two unit capacitances during the first two conversions, e.g. $C1 = C_u*(1 + 0.01)$, $C2 = C_u*(1 - 0.01)$. The RMS maximum DNL and the RMS maximum INL are 0.801 and 0.899 LSB respectively. The result is not as good as expected, so it should be improved. Figure 9 shows the improvements in the proposed switching circuit. We just need to change the structure of unit capacitance during the first two conversions into the structure in Fig. 9. Then the mismatch can be much lower than above.

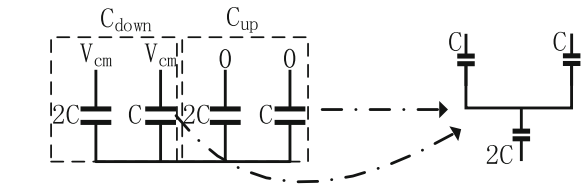


Fig. 9 Improvements to the proposed switching circuit

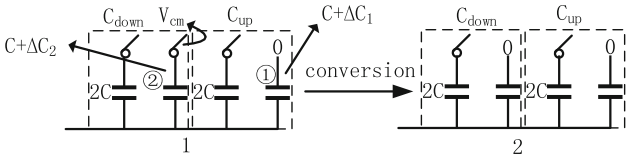


Fig. 10 Deviation of the unit capacitances

Table 1 Comparison of switching technique for 10-bit SAR

Switching method	Switching energy (CV^2_{ref})	Energy saving (%)	Reference voltage	Reset energy consumption
Convention	1363.3	Reference	V_{ref}, gnd	No
Tri-level [1]	42.4	96.9	V_{ref}, V_{cm}, gnd	No
VMS [2]	31.88	97.66	V_{ref}, V_{cm}, gnd	No
Trade-off [3]	26.54	98.05	V_{ref}, V_{cm}, gnd	No
Advanced energy-back [5]	10.66	99.2	V_{ref}, V_{cm}, gnd	Yes
Proposed	0	100	V_{cm}, gnd	No

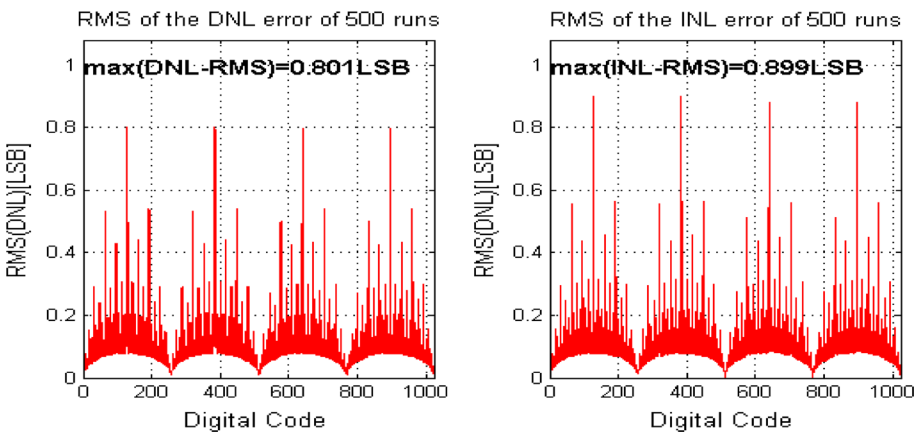


Fig. 8 DNL and INL versus output code of the proposed scheme

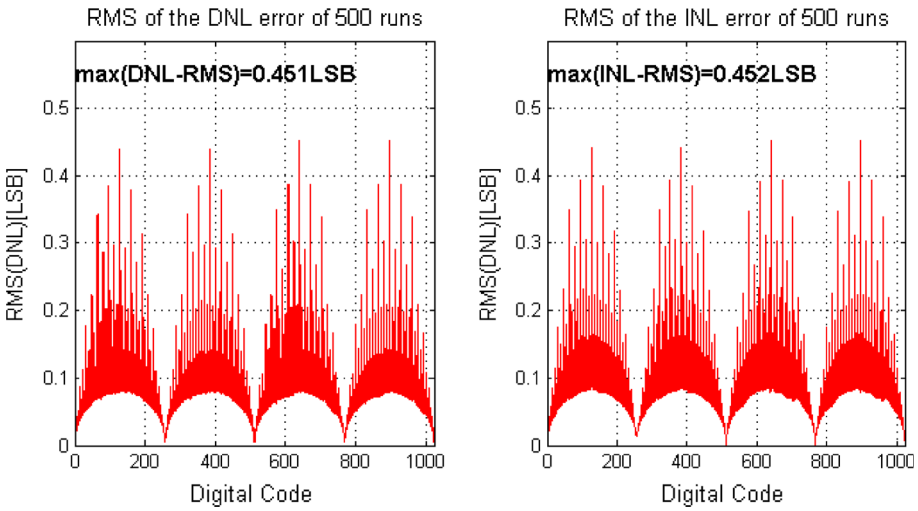


Fig. 11 DNL and INL versus output code of the improved switching scheme

Figure 10 shows the deviation of the unit capacitances, it is caused by a variety of undesirable factors. When the conversion goes from 1 to 2, the change of the top plate voltage is $-\frac{C+\Delta C_1}{2C+\Delta C_1+\Delta C_2} \times V_{cm}$, and the ideal changing is $-\frac{C}{2C} \times V_{cm} = -\frac{1}{4} V_{ref}$. The structure of C–2C can alleviate this problem. There is a special case that when $\Delta C_1 = \Delta C_{max}$ and $\Delta C_2 = -\Delta C_{max}$, it will lead to serious non-linear problems. When all the capacitances, which is used to substitute the unit capacitance ① in Fig. 10, increase their relative maximum value ($C_{C-2C} = C + \Delta C_{max}$, $2C_{C-2C} = 2C + 2\Delta C_{max}$) and all the capacitances which replace the unit capacitance ② decrease their relative maximum value ($C_{C-2C} = C - \Delta C_{max}, 2C_{C-2C} = 2C - 2\Delta C_{max}$), this case will occur. Obviously, the structure of C–2C greatly reduces the RMS maximum DNL and the RMS maximum INL.

Figure 11 shows the DNL and INL versus output code of the improved switching scheme. It is clear that the improved circuit has a great role on DNL and INL. The RMS maximum DNL and the RMS maximum INL are 0.451 and 0.452 LSB respectively. Compared with the original circuit, the RMS maximum DNL and the RMS maximum INL are decreased by 0.35 and 0.447 LSB respectively.

6 Conclusion

Because the method based on the capacitance floating to reduce the energy dissipation has been used in many published works, an energy-efficient switching scheme for SAR ADC is proposed in the paper. Compared with the traditional switching scheme, the novel switching scheme achieves 100% less switching energy. The proposed switching scheme is a single-ended conversion and after the second comparison, its total voltage change is based on V_{cm}. So it achieves about 50% area reduction than the conventional architecture. In addition, the switching scheme proposed in the paper uses only two references and has no reset energy. The RMS of maximum DNL and the RMS of maximum INL are 0.451 and 0.452 LSB respectively.

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