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Current inverting metamutator, its implementation with a new single active device and applications

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Abstract
A new kind of metamutator, namely "Current Inverting Metamutator", its realizations using different types of active blocks and some of its applications like voltage-mode universal biquadratic filter with three input and one output terminals are presented. The proposed circuits can realize all standard filters, namely, low-pass, band-pass, high-pass, notch and all-pass without passive component matching conditions. The proposed circuit offers the features of using grounded capacitors and orthogonal controllability of angular frequency and quality factor. Then a novel realization of metamutator with one active device, additive and differential IC (AD-IC) is proposed and implemented with twelve transistors only. The metamutator with AD-IC has the advantages: (1) of creating new realizations of memristors, capacitance multipliers, inductor simulators, frequency dependent negative resistors which can be used to make IC active filters, (2) less is the number (only one) of active devices, less is the amount of disparity, (3) no need to match passive component values.

Keywords Metamutator · Memristors · Analog circuit design · Universal filter · FDNR

1 Introduction

In 1971 memristor and a 2-port mutator, with a very complex circuit structure, for transforming nonlinear circuit elements to memristor was introduced in [1]. Recently different circuit structures for 2-port mutators have been introduced for obtaining Memstors (a generic name covering memristors, meminductors, memcapacitors) from nonlinear resistors or, converting one type of memstor to another [1–7].

The idea of a new class of multifunctional 4-ports was first introduced in [8] and then named metamutator, because of its ability of transforming many kinds of circuit elements to each other among other applications. These 4-port metamutators can be used for realizing mutators, quadrature oscillators, inverters, trans-admittance, trans-impedance amplifiers and gyrators by properly terminating some of its ports. Different kinds of circuit structures for metamutators have been introduced in [8–12]. Because of the port description matrix (1) and the negative sign in the voltage relation of two of its ports, it was named as Voltage Inverting Metamutator (VIM).

Recently, different kinds of filters and multifunctional filters with diverse realizations have been introduced by several researchers and manufacturers [13–16]. Universal filters are able to realize different types of filters low-pass (LP), high-pass (HP), band-pass (BP), band-stop (BS) and all-pass (AP) simultaneously. They are widely used in electronic measurements, communications and neural networks. The voltage-mode active filters with high input impedance are useful because by cascading several filters of this type, higher order filters can be realized [24, 25].

According to the number of input and output ports, filters can be classified into three categories: (1) single-input, multiple-output (SIMO) [26, 27], (2) multiple-input, single-output (MISO) [28] and (3) multiple-input, multiple-output (MIMO) type [29]. Similarly different realizations of a variety of impedance simulators, gyrators, frequency dependent negative resistors (FDNR) simulators are being considered by several companies and authors [17–21]. In

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[19] a FDNR simulator with two DO-CCIIs, three resistors and one capacitor, in [20, 23] a FDNR using two current backward transconductance amplifiers (CBTAs) and several passive components is presented. A FDNR simulator with two voltage differencing current conveyors (VDCCs), a single grounded resistor and two grounded capacitors is proposed in [22]. With two or more active devices in their structure, most of these circuits necessitate component matching. Also, because of many active devices present, existing parasitic elements and non-ideal gain effects create severe problems; less number of active devices causes less amount of disparity.

With the first part of the paper the newly introduced metamutator, named as current inverting metamutator (CIM) due to its port description matrix (2) and the negative sign in the current relation of two of its ports, is being presented in Sect. 2. Three CIM circuit realizations will be offered in Sect. 3. Application of CIM as universal filter is proposed in Sect. 4 with its simulation results in Sect. 5.

In the second part of the paper a new metamutator circuit with only one new active device, additive and differential-integrated circuit (AD-IC) realized only with twelve transistors, will be proposed; its port description matrix and circuit structure with twelve transistors using TSMC 0.25 µm CMOS process parameters will be given in Sect. 6. Theoretical analysis of the inductor simulator, capacitance multiplier, and FDNR will be presented in Sect. 7. The layout, the post-layout simulation results obtained using TSMC 0.25 µm process parameters with ± 1.25 V supplies confirming the claimed applications, including memristor's signature, will be exhibited in Sect. 8. In the circuits introduced here, as only one active device and few passive components are being used, there is no need of matching components and functionality. Finally, Sect. 9 will conclude the paper.

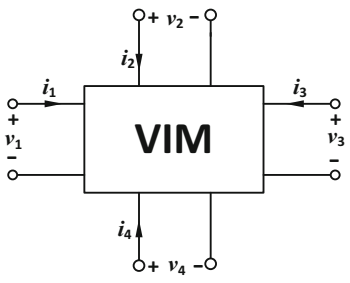

Fig. 1 Block diagram of VIM [8, 9]

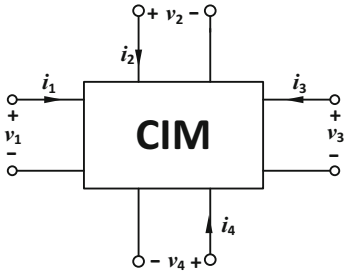

Fig. 2 Block diagram of CIM

2 VIM and CIM

The 4-port block diagrams of VIM and CIM are shown in Figs. 1 and 2 and their port descriptions are defined via the equalities (1) and (2) respectively. Although identity matrix shows in both expressions in VIM a port voltage is being inverted whereas, in CIM a port current is inverted. As care must be exercised in the implementation phase as to which variable follows the other in (1) and (2), variables have been indexed with letters k, l, m, n taking different values from the set {1, 2, 3, 4} as required by the application.

$$\begin{bmatrix} i_k \\ i_l \\ v_m \\ v_n \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_m \\ i_n \\ v_l \\ -v_k \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} i_k \\ i_l \\ v_m \\ v_n \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_m \\ -i_n \\ v_l \\ v_k \end{bmatrix} \tag{2}$$

3 Proposed realizations of CIM

3.1 Realization with one CFOA and one CCII+

In this section, three new CIM structures using two off the shelf active devices are being proposed. The circuit structure of the first one for $l = 1$, $n = 2$, $k = 3$, $m = 4$ is shown

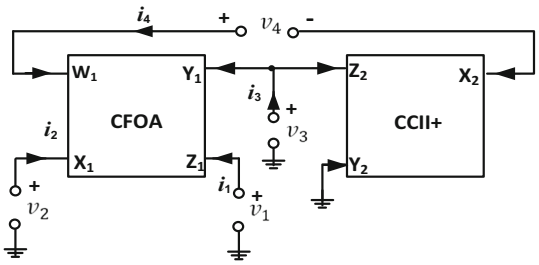

Fig. 3 Metamutator using CFOA and CCII+

in Fig. 3, using one current feedback operational amplifier (CFOA) and one second-generation plus type current conveyor (CCII+) are being employed, which are defined respectively by (3) and (4).

$$\begin{bmatrix} i_z \\ v_x \\ v_w \\ i_y \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_x \\ v_y \\ v_z \\ i_w \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{4}$$

After some algebraic manipulations using KCL and KVL the port relation matrix describing the circuit in Fig. 3 becomes as given with expression (2).

3.2 Realization with two DOCCIIs

As shown in Fig. 4, the second CIM is designed by using two dual output second generation current conveyors (DOCCII) with port definition matrix shown in (5). The structure of this metamutator is extracted from [4].

$$\begin{bmatrix} i_{z+} \\ i_{z-} \\ v_x \\ i_y \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ v_y \\ v_z \end{bmatrix} \tag{5}$$

After some algebraic manipulations the port relation matrix between currents and voltages of the circuit in Fig. 4 becomes as given with expression (2) thus identifying a CIM.

3.3 Realization with two CFOAs

The third CIM is designed using two CFOA defined by (3), as shown in Fig. 5. It can easily be verified that the 4-port satisfies the CIM port description as given by (2).

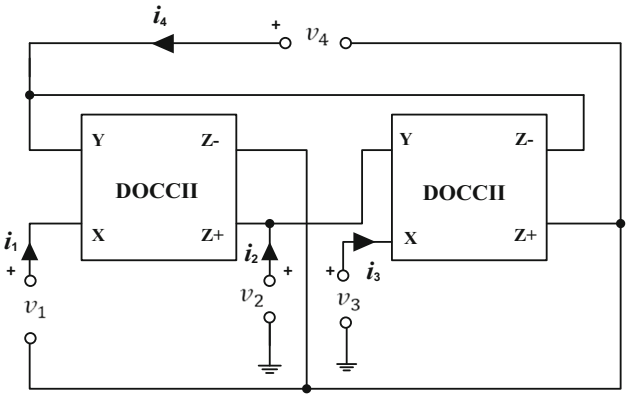

Fig. 4 Metamutator with two DOCCIIs

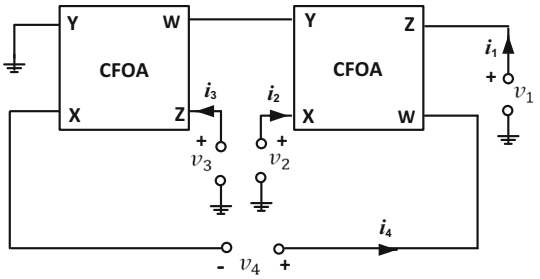

Fig. 5 Metamutator realized with two CFOAs

4 Application of CIM as universal filter

In [30–38] several multi input VM universal biquadratic filters were introduced and different kinds of filters can be realized by properly selections of input voltage terminals in these circuits. However, these circuits suffer from one or more of the following problems:

1. In [33, 34, 36–38] the necessity of passive component matching conditions,
2. In [30–32, 35] lack of orthogonal controllability of the resonance angular frequency (ω_0) and quality factor (Q),
3. In [34, 36, 37] use of many passive components.

Application of CIM as a voltage mode (VM) universal filter is presented in this section. As an example, the CIM circuit with one CFOA and one CCII+ is selected. Using Table 1 to connect properly elements to ports of CIM in Fig. 3, different realizations of a multifunctional filter will be obtained. For example, applying realization #1 the circuit will become as shown in Fig. 6.

From (2) $v_2 = v_3$ and selecting the output as $v_3 = v_{\text{out}}$, KCL at port 2 of the circuit in Fig. 6 gives:

$$I_2 = sC_1(V_{S1} - V_{\text{out}}) + \frac{(V_{S2} - V_{\text{out}})}{R_1} \tag{6}$$

Using $i_1 = i_2$, $v_4 = v_1$ from (2), $i_1 = -\frac{v_1}{R_3}$, and $V_4 = -\frac{1}{sC_2} I_4$ in (6), gives:

$$I_4 = s^2 C_1 C_2 R_3 (V_{S1} - V_{\text{out}}) + \frac{sC_2 R_3}{R_1}(V_{S2} - V_{\text{out}}) \tag{7}$$

then using $i_3 = -i_4$ and $I_3 = (V_{S3} - V_{\text{out}})/R_2$ in (7) gives

Table 1 Multifunctional filter realizations

Realization	R_3	$(C_1 + v_{S1})//(R_1 + v_{S2})$	C_2	$R_2 + V_{s3}$
#1	Port 1	Port 2	Port 4	Port 3
#2	Port 4	Port 3	Port 1	Port 2
#3	Port 2	Port 1	Port 3	Port 4
#4	Port 3	Port 4	Port 2	Port 1

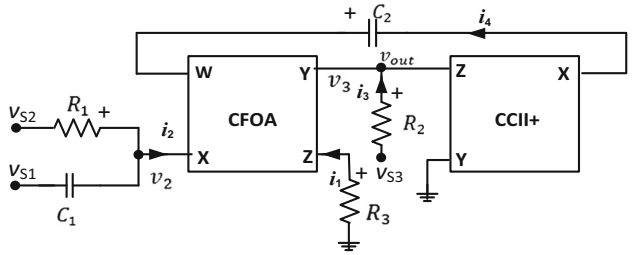

Fig. 6 Universal filter realization #1 with CCII+ and CFOA

$$\frac{(V_{S3}-V_{\text{out}})}{R_2}=s^2C_1C_2R_3(V_{\text{out}}-V_{S1})+\frac{sC_2R_3}{R_1}(V_{\text{out}}-V_{S2}) \tag{8}$$

Solving for V_{out} in terms of V_{S1}, V_{S2} and V_{S3} from (8) the output of the multifunctional filter is found as shown by (9), with the selection of different voltage sources resulting in different filter functions as shown in Table 2:

$$V_{\text{out}}(s)=\frac{s^2C_1C_2R_1R_2R_3V_{S1}+sC_2R_3R_2V_{S2}+R_1V_{S3}}{s^2C_1C_2R_1R_2R_3+sC_2R_3R_2+R_1} \tag{9}$$

So, the proposed CIM circuit can realize all filter functions with no requirements for matching conditions. The angular resonance frequency (ω_0) and the quality factor (Q) of all filter responses, given in Table 2, are:

$$\omega_0=\frac{1}{\sqrt{C_1C_2R_2R_3}} \tag{10}$$

$$Q=R_1\sqrt{\frac{C_1}{C_2R_2R_3}} \tag{11}$$

As shown by (10) and (11), the angular frequency can be controlled by R_2 and/or R_3 and the quality factor can be independently controlled by R_1. So the angular frequency and quality factor are orthogonally controllable. In the case of $C_1 = C_2 = C$ and $R_1 = R_2 = R_3 = R$ the angular frequency becomes $\omega_0 = \frac{1}{RC}$ and the quality factor is $Q = 1$. All of the filters have non-inverting unity gain and these results are also valid for other CIM circuits introduced in Sect. 3.

Taking into consideration of CIM non-idealities the port description matrix of CIM becomes,

Table 2 Different filters of realization #1

Selection	V_{S1}	V_{S2}	V_{S3}	Filter type
I	V_{in}	0	0	High-pass
II	0	0	V_{in}	Low-pass
III	0	V_{in}	0	Band-pass
IV	V_{in}	0	V_{in}	Band-notch
V	V_{in}	$-V_{\text{in}}$	V_{in}	All-pass

$$\begin{bmatrix} i_1 \\ i_3 \\ v_2 \\ v_4 \end{bmatrix}=\begin{bmatrix} \alpha_1 & 0 & 0 & 0 \\ 0 & -\alpha_2 & 0 & 0 \\ 0 & 0 & \beta_1 & 0 \\ 0 & 0 & 0 & \beta_2 \end{bmatrix}\begin{bmatrix} i_2 \\ i_4 \\ v_3 \\ v_1 \end{bmatrix} \tag{12}$$

where α_j and β_j are current and voltage frequency dependent non-ideal gains respectively and are equal to unity ideally. Furthermore,

$$\begin{cases} \alpha_j = 1-\varepsilon_{ij} \\ \beta_j = 1-\varepsilon_{vj} \end{cases} \quad j=1,2 \text{ and } \left(\left|\varepsilon_{ij}\right|,\left|\varepsilon_{vj}\right|\right) \ll 1$$

in which ε_{ij} and ε_{vj} are current and voltage tracking error coefficients with values close to zero. The non-ideal angular frequency ω_0, quality factor Q and bandwidth for all types of filters are obtained as,

$$\omega_0=\sqrt{\frac{G_2G_3}{\alpha_1\alpha_2\beta_1\beta_2C_1C_2}} \tag{13}$$

$$Q=\frac{1}{G_1}\sqrt{\frac{C_1G_2G_3}{\alpha_1\alpha_2\beta_1\beta_2C_2}} \tag{14}$$

$$\text{BW}=\frac{\omega_0}{Q}=\frac{G_1}{C_1} \tag{15}$$

Sensitivities of this filter, derived from (13) to (15), are:

$$S^{\omega_0}_{G_2,G_3}=-S^{\omega_0}_{\alpha_1,\alpha_2,\beta_1,\beta_2,C_1,C_2}=\frac{1}{2} \tag{16}$$

$$S^{Q}_{G_1}=-1,\quad S^{Q}_{G_2,G_3,C_1}=-S^{Q}_{\alpha_1,\alpha_2,\beta_1,\beta_2,C_2}=\frac{1}{2} \tag{17}$$

$$S^{\text{BW}}_{G_1}=-S^{\text{BW}}_{C_1}=1 \tag{18}$$

The absolute values of all passive and active element sensitivities are low and not larger than unity.

5 Simulation results of the universal filter

The simulation results of different types of filters shown in Fig. 6 are shown in Figs. 9 and 10. An AC voltage source with amplitude of 1 V is chosen for all of the voltage sources. For the characteristic frequency $f_0 = \omega_0/2\pi \cong 6.36$ MHz and the quality factor of filters $Q = 1$, the passive component values have been chosen as $C_1 = C_2 = 25$ pF, $R_1 = R_2 = R_3 = 1$ kΩ. For CFOA and CCII, 0.13 μm CMOS technology parameters have been used. The transistor level circuits are shown in Figs. 7 and 8, parameters being given in Tables 3 and 4 respectively; supply voltages are selected as ± 0.75 V, V_B = 0.24 V.

The transfer functions and simulation results of different types of filters are collected in Table 5 and Fig. 9, those of all-pass being in Fig. 10.

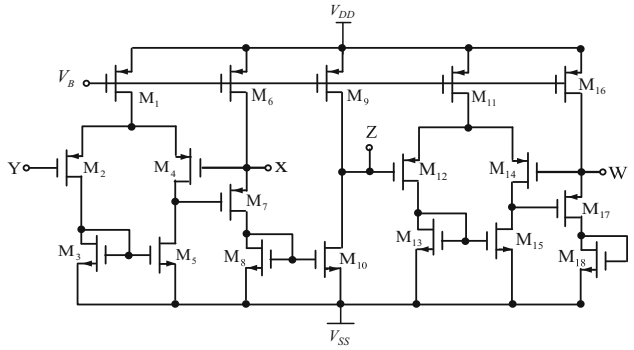

Fig. 7 Transistor level circuit of CFOA [22]

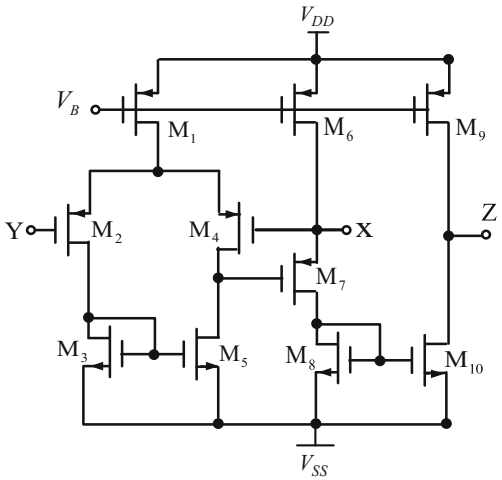

Fig. 8 Transistor level circuit of CCII [22]

Table 3 Transistor dimensions in CFOA

Transistor	*W/L* (μm)
M_1, M_2, M_4, M_6, M_9, M_{11}, M_{12}, M_{14}, M_{16}	41.6/0.52
M_7 and M_{17}	83.2/0.52
M_3, M_5, M_8, M_{10}, M_{13}, M_{15}, M_{18}	13/0.52

Table 4 Transistor dimensions in CCII

Transistor	*W/L* (μm)
M_1, M_2, M_4, M_6, M_9	41.6/0.52
M_7	83.2/0.52
M_3, M_5, M_8, M_{10}	13/0.52

Table 5 Transfer functions of different filters

	Filter function	Filter type
1	$\frac{V_{out}}{V_{in}}(s) = \frac{s^2C_1C_2R_3R_2}{s^2C_1C_2R_3R_2+s\frac{C_2R_3R_2}{R_1}+1}$	High-pass
2	$\frac{V_{out}}{V_{in}}(s) = \frac{1}{s^2C_1C_2R_3R_2+s\frac{C_2R_3R_2}{R_1}+1}$	Low-pass
3	$\frac{V_{out}}{V_{in}}(s) = \frac{s\frac{C_2R_3R_2}{R_1}}{s^2C_1C_2R_3R_2+s\frac{C_2R_3R_2}{R_1}+1}$	Band-pass
4	$\frac{V_{out}}{V_{in}}(s) = \frac{(s^2C_1C_2R_3R_2+1)}{s^2C_1C_2R_3R_2+s\frac{C_2R_3R_2}{R_1}+1}$	Band-notch
5	$\frac{V_{out}}{V_{in}}(s) = \frac{s^2C_1C_2R_3R_2-s\frac{C_2R_3R_2}{R_1}+1}{s^2C_1C_2R_3R_2+s\frac{C_2R_3R_2}{R_1}+1}$	All-pass

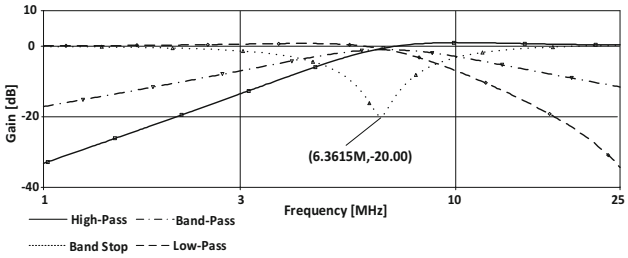

Fig. 9 Simulation results for high-pass, low-pass, band-pass and band-stop filters in Fig. 6

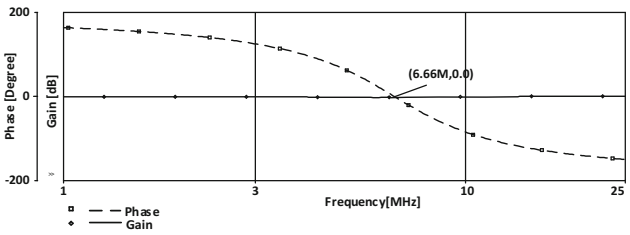

Fig. 10 Phase and gain of all-pass filter in Fig. 6

6 Metamutator with single active device AD-IC

The first metamutator was built using two separate adder and subtractor ICs in [8]. In this section a single 4-port IC named additive and differential IC (AD-IC) built only with twelve transistors will be proposed. The block diagram and port description matrix of AD-IC are shown in Figs. 11 and 19 respectively.

The 4-port metamutator can be constructed by properly interconnecting terminals of AD-IC as shown in Fig. 12. The port description matrix of this metamutator is the same as in (1) making it a VIM type metamutator, and the Table 4 in [8] illustrating several applications stands also true for this configuration.

$$\begin{bmatrix} v_{x1} \\ v_{x2} \\ i_{y1} \\ i_{y2} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{y1} \\ v_{y2} \\ i_{x1} \\ i_{x2} \end{bmatrix} \quad (19)$$

In the realization of AD-IC, TSMC 0.25 μm CMOS process parameters were used, with transistor dimensions as shown in Table 6 and its circuit in Fig. 13. The developed CMOS layout of AD-IC is given in Fig. 16.

7 Applications of metamutator with AD-IC

Many applications of metamutator were given in [8–12]. In this section three new applications: inductor simulator, capacitance multiplier and FDNR Simulator are being proposed using the metamutator built with AD-IC. The general structure of the configuration using the AD-IC metamutator with port impedances is shown in Fig. 14.

By connecting impedances to three of the ports, the impedance seen from the remaining 4th port is depicted in Table 7. When reading column i of Table 7 it should be understood that no element is connected to port i whereas impedances Z_j are connected to port j for $j \neq i$ and $i = 1, 2, 3, 4$.

Figure 14 illustrates the case $i = 1$. An interesting conclusion that can be deduced from Table 7 is that the metamutator allows the realization of grounded elements as well as floating ones. The simulation results of all applications will be given in the next section.

7.1 Application as inductor simulator

As coil realization of inductors on an integrated chip is highly undesirable many inductor simulator circuits have been proposed in the literature [39, 40]. In this section an application of metamutator as inductance simulator with minimum number of elements, AD-IC with 12 transistors, two resistors and single capacitor, is presented. According to Table 7 by connecting one capacitor and two resistors to three of the ports properly, an inductor will be achieved at the fourth port and the value of the inductance is equal to

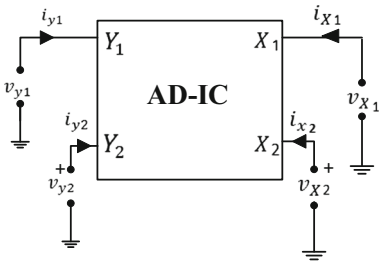

Fig. 11 Block diagram of AD-IC

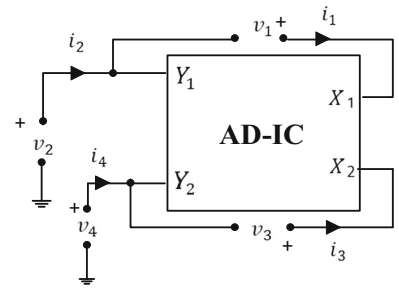

Fig. 12 Block diagram of metamutator with AD-IC

Table 6 Transistor dimensions in AD-IC

Transistors	W/L (μm)
M_1, M_2, M_5, M_6, M_7, M_8, M_9, M_{10}	1/0.5
M_3, M_4, M_{11}, M_{12}	30/0.5

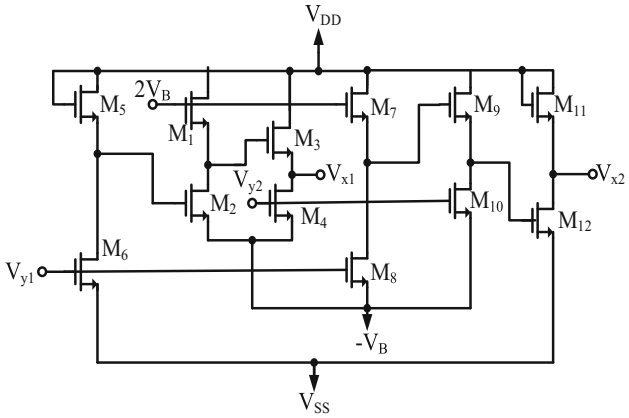

Fig. 13 Implementation of AD-IC with 12 MOS transistors

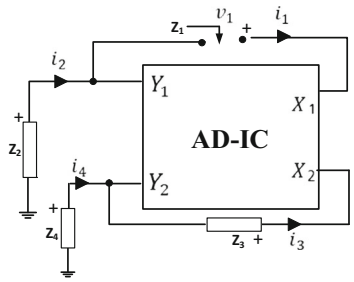

Fig. 14 Metamutator terminated with port impedances

Table 7 Equivalent impedance at the ports

Ports	Port 1	Port 2	Port 3	Port 4
Type	Floating	Grounded	Floating	Grounded
Z	$Z_{in} = \frac{Z_4}{Z_3} \cdot Z_2$	$Z_{in} = \frac{Z_3}{Z_4} \cdot Z_1$	$Z_{in} = \frac{Z_2}{Z_1} \cdot Z_4$	$Z_{in} = \frac{Z_1}{Z_2} \cdot Z_3$

the product of the values of capacitor and resistors. The different realizations are shown in Table 8.

7.2 Application as capacitance multiplier

According to Table 7 by replacing one capacitor and two resistors (or three capacitors) in three of the ports, a capacitor will be achieved at the fourth port for which the value of the so obtained capacitance is the value of the capacitor multiplied by the ratio of resistance (capacitance) values. Possible realizations are shown in Table 9.

7.3 Application as FDNR simulator

Low-pass filters have wide usage in radio frequency (RF) transceivers; in this process the much-used low-pass filter is called an anti-aliasing filter. By reducing the size and refining the performance of these filters, new improvements in communication are achieved. Figure 15 shows the position of the anti-aliasing filter in fully digital receivers.

As in general anti-aliasing filters (AAF) are third or higher order passive LC ladder filters using an inductor in these circuits requires a lot of space and reduces the performance. In order to reduce the size and improve the performance one can use the complex impedance scaling technique for designing a prototype of the LC ladder circuits. This technique, treated extensively by Bruton [41], is based on the fact that the filter transfer function will remain unchanged if the impedance of each element is divided by s. So the Inductor will be transformed into a resistor, the resistor will be transformed into a capacitor and the capacitor will be transformed into a FDNR.

By connecting two capacitors and one resistor to three of the ports, as detailed in Table 7, a grounded or floating FDNR will be achieved at the fourth port. The value of the FDNR and different realizations are shown in Table 10. It should be observed again that only twelve transistors and three passive elements are being used with no component matching requirements.

Table 8 Different realizations of Inductor

	Port 1	Port 2	Port 3	Port 4	Inductance value
#1	L_{eq}	R_2	C_3	R_4	$L_{eq} = C_3R_2R_4$
#2	R_1	L_{eq}	R_3	C_4	$L_{eq} = C_4R_1R_3$
#3	C_1	R_2	L_{eq}	R_4	$L_{eq} = C_1R_2R_4$
#4	R_1	C_2	R_3	L_{eq}	$L_{eq} = C_2R_1R_3$

Table 9 Capacitance multiplier realizations

	Port 1	Port 2	Port 3	Port 4	Capacitance value
#1	C_{eq}	C_2	R_3	R_4	$C_{eq} = C_2 \cdot R_4/R_3$
#2	C_{eq}	R_2	R_3	C_4	$C_{eq} = C_4 \cdot R_3/R_2$
#3	R_1	C_{eq}	C_3	R_4	$C_{eq} = C_3 \cdot R_4/R_1$
#4	C_1	C_{eq}	R_3	R_4	$C_{eq} = C_1 \cdot R_4/R_3$
#5	R_1	C_2	C_{eq}	R_4	$C_{eq} = C_2 \cdot R_1/R_4$
#6	R_1	R_2	C_{eq}	C_4	$C_{eq} = C_4 \cdot R_1/R_2$
#7	C_1	R_2	R_3	C_{eq}	$C_{eq} = C_1 \cdot R_2/R_3$
#8	R_1	R_2	C_3	C_{eq}	$C_{eq} = C_3 \cdot R_2/R_1$

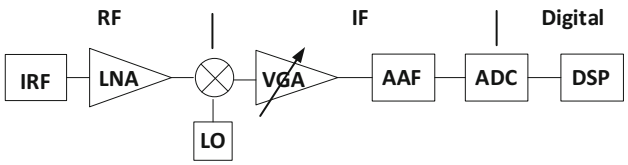

Fig. 15 Schematic of fully digital receiver [24]

8 Simulation results

The layout of the AD-IC circuit is shown in Fig. 16. The area of the AD-IC is approximately 60 × 22 μm^2. Post-layout simulations are performed using the netlist extracted from the layout with TSMC 0.25 μm process parameters. The supply voltage is taken as ± 1.25 V and V_B as 0.8 V. For increasing the dynamic range of the AD-IC circuits all NMOS transistors' substrates are connected to V_{SS} terminal. The dimensions of the transistors used for the circuit are given in Table 6. The equivalent parasitic capacitances C_L at the output ports are approximately 73 fF. For the purpose of providing a smaller output resistance the W/L ratios of the output node transistors M3, M4, M11 and M12 in Table 6 are chosen much bigger than the ratio of other transistors.

8.1 Memristor realization

The port description matrix of metamutator with single active device AD-IC is the same as the port description

Table 10 Different realizations of FDNR

	Port 1	Port 2	Port 3	Port 4	FDNR
#1	D_{eq}	C_2	R_3	C_4	$D_{eq} = 1/s^2C_2C_4R_3$
#2	C_1	D_{eq}	C_3	R_4	$D_{eq} = 1/s^2C_1C_3R_4$
#3	R_1	C_2	D_{eq}	C_4	$D_{eq} = 1/s^2C_4C_2R_1$
#4	C_1	R_2	C_3	D_{eq}	$D_{eq} = 1/s^2C_3C_1R_2$

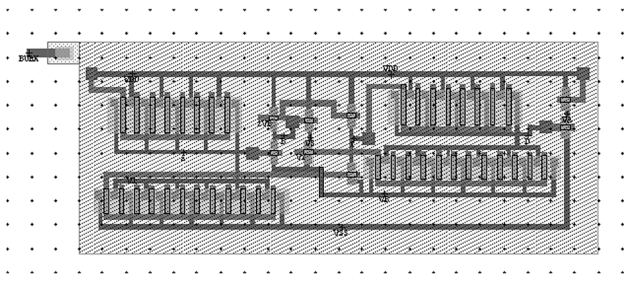

Fig. 16 Layout of the AD-IC circuit

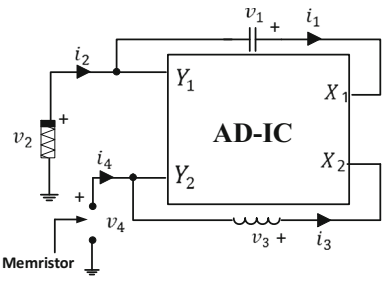

Fig. 17 Mutation of nonlinear resistor to memristor

matrix of metamutators with two active devices. In this case all applications obtained so far, can also be achieved by the AD-IC metamutator, as all the results are based on the port relationship given either by the expressions (1) or (2). For example, in case of terminating the ports 1, 2 and 3 by a capacitor, a nonlinear resistor and an inductor respectively, a grounded memristor will be achieved at the 4th port [8].

By applying a sinusoidal voltage source with amplitude of 2.5 V and frequency of 22 Hz at port 4 of the metamutator in Fig. 17, the current versus voltage and voltage versus current characteristics are obtained as shown in Fig. 18. For the nonlinear resistor the model introduced in [10] is being used. The supply voltages are chosen as $\pm$ 1.25 V and V_B as 0.5 V. The capacitor and inductor values were selected as 1 nF and 1 mH, respectively. The Lissajous curves show the signature of memristor at port 4.

8.2 Capacitance multiplier realization

According to Table 9 and applying realization #3 to the metamutator with AD-IC and connecting C_3, R_1 and R_4 to three of the ports of the metamutator, a capacitor with the value of KC_3 will be obtained at the second port with $K = R_4/R_1$. Moreover, the functionality and frequency response plots of the multiplied capacitor and that of an ideal capacitor are given in Fig. 19 for case #3 with R_1 = 1 kΩ, R_4 = 20 kΩ and C_4 = 5 pF, which yields the multiplied capacitance value of 100 pF.

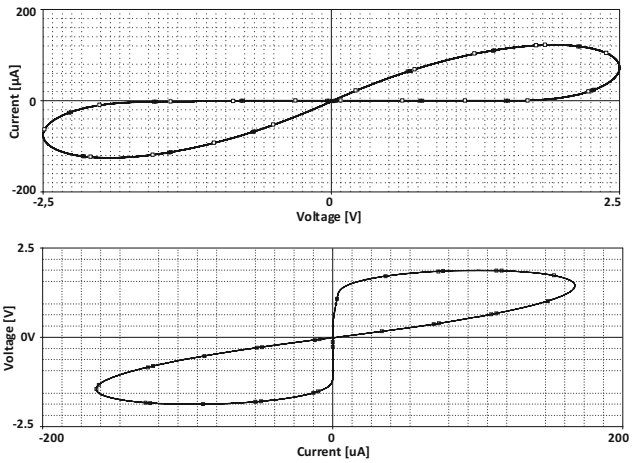

Fig. 18 $v - i$ Characteristics of memristor

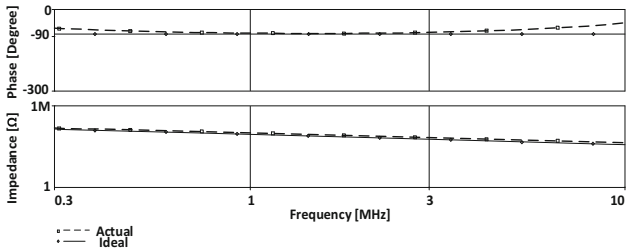

Fig. 19 |Impedance| and phase of the capacitor vs. frequency

In this case the metamutator was simulated using an AC voltage source with amplitude 0.3 V; for AD-IC, TSMC, 0.25 μm CMOS process parameters were used with transistor dimensions as shown in Table 6 and the circuit in Fig. 13. The supply voltages were chosen as $\pm$ 1.25 V and V_B as 0.8 V.

8.3 Inductor simulator realization

According to Table 8 and applying realization #2 to the metamutator with AD-IC and replacing C_4, R_1 and R_3 in three of the ports of the metamutator, an inductor will be obtained in the second port; Furthermore, the performance of the proposed inductance, the frequency response plots of the newly designed and ideal inductor are both given in Fig. 20 for $R_1 = R_3$ = 1 kΩ and C_4 = 25 pF, which corresponds to an inductance of 25 μH.

In this case the metamutator was simulated using an AC current source with amplitude of 1 mA. For AD-IC TSMC, 0.25 μm CMOS process parameters were used with transistor dimensions as shown in Table 6 and its circuit in Fig. 13. Supply voltages are chosen as $\pm$ 1.25 V, V_B = 0.8 V.

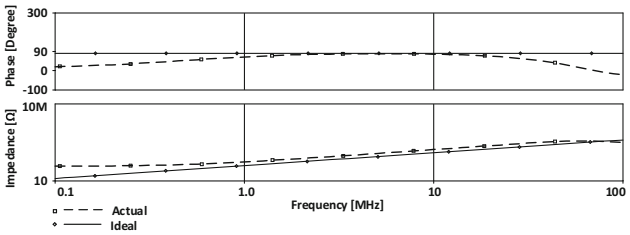

Fig. 20 Phase and limpedancel of the inductor vs. frequency

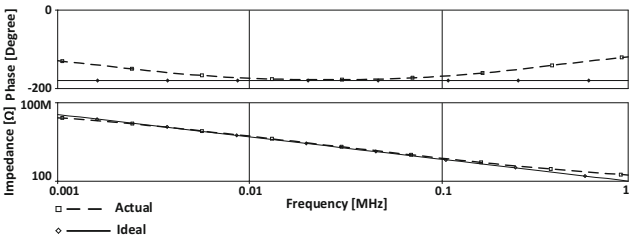

Fig. 21 Characteristics of FDNR in frequency domain

8.4 FDNR simulator realization

Applying realization #4 to the metamutator with AD-IC as given in Table 10 and connecting C_1, R_2 and C_3 to ports 1, 2 and 3 of the metamutator respectively, a FDNR will be observed from port 4. The simulation results are demonstrated in Fig. 21.

The metamutator with AD-IC was simulated using an AC voltage source with amplitude of 1 V. For AD-IC, TSMC 0.25 μm CMOS process parameters were used, with transistor dimensions as shown in Table 10 and its circuit in Fig. 13. The supply voltages are chosen as ± 1.25 V, V_B as 0.8 V. The values of C_1, C_3 and R_2 were selected as 0.1 nF, 0.2 nF and 100 kΩ, respectively.

9 Conclusion

It has been shown that metamutators, recently introduced 4-ports in [8, 12], can be classified into two categories as: voltage inverting VIM and current inverting CIM (presented in this paper). CIM is also capable to implement a variety of elements/systems like VIM and it has been given three IC realizations using two different IC devices. One of these new realizations has been applied to the simulation of a memristor by properly terminating three of the ports and verifying the memristor's signature.

Several new configurations, with properly terminated CIM ports, have been shown to be able to generate Universal Filters, a new application among many others presented in [8, 12]. All five filter types, band-, low-, high-, all-pass and band notch have been simulated with TSMC 0.13 μm parameters for one configuration and they have exhibited excellent frequency response.

Using AD-IC, introduced in this paper, as the only single active device and no passive elements, the metamutator has been given a new realization which was applied to capacitance scaling, memristor/inductor simulations and FDNR realization. Depending on the choice of the input port, these realizations can be made grounded or floating. All four applications have been simulated with TSMC 0.25 μm CMOS process parameters and shown to be in very good agreement with theoretical results.

Future work will concentrate on the comparison of VIM versus CIM, novel types of metamutators, their different realizations, tuning external elements to improve the behavior of these applications and further applications like linear oscillators, operational amplifiers etc. Filter building with FDNRs realized here and comparing the effect of using different kind of metamutators in the design of these filters will deserve special consideration. In another direction use of metamutators in nonlinear applications such as rectifiers, modulators will be looked upon.

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