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A hybrid CDAC-threshold configuring SAR ADC in 28nm FDSOI CMOS

Mustafa Kilic[1] · Themistoklis G. Mavrogordatos[2] · Yusuf Leblebici[1]

Abstract
In this paper, a 9-bit 1.3 GS/s single channel SAR ADC is presented. In conventional SAR ADCs, the capacitive DAC size grows exponentially with respect to converter resolution. This results in both signal bandwidth and conversion speed reduction. The proposed architecture implements binary search through a redundant capacitive DAC for the 5 first MSBs and through programmable comparator thresholds for the remaining 4 LSBs. The DAC capacitance at the front-end remains small enough to achieve high sampling rate with increased input bandwidth. Two asynchronously clocked alternate comparators are used additionally to improve conversion speed. The ADC is designed and simulated in 28 nm FD-SOI CMOS. It consumes 4.1 mW from a 1 V supply, while achieving a SNDR of 52.1 dB and a Figure-of-Merit of 11.4 fJ/conversion-step.

Keywords SAR ADC · High speed ADC · Threshold configuring · Asynchronous logic

1 Introduction

During the last two decades, the amount of data transferred worldwide has been dramatically increasing year by year. This was achieved by the development of communication networks of higher and higher capacity. Analog to Digital Converters (ADCs) are fundamental building blocks in such electronic systems since they convert the input analog signal to a digital one which will be subsequently digitally processed by the system. Performance requirements on ADCs are not only imposed in terms of speed, but also in terms of resolution, power consumption and bandwidth efficiency, as the complexity of modern applications is rapidly increasing.

Architectures such as the Flash and the Pipeline ADCs were suitable for high speed applications until recently. However the Flash architecture has low resolution while the pipeline requires accurate residue amplification between its stages. The introduction of nanometre-scale

Complementary Metal-Oxide Semiconductor (CMOS) processes have resulted in lower headroom voltage $V_{DD} - V_{th}$ for transistors with poorer intrinsic gain [1]. It follows that technology scaling favours mostly the performance of ADC architectures with few analog building blocks, such as the Successive Approximation Register (SAR) ADC which includes only the comparator as a purely analog building block. The significant performance benefits in terms of speed and power consumption of the digital logic block explain the rising interest in the engineering community for SAR ADCs operating at high speeds for medium to high resolution. Several design techniques have been proposed to enhance the speed performance of such SAR ADCs. Asynchronous clocking [2, 3], top plate sampling [4] or alternate comparators [5] have reduced the ADC conversion times considerably. Nevertheless, achieving high sampling rate becomes increasingly difficult for higher resolution SAR ADCs. The Digital to Analog Converter (DAC) total capacitance is doubling for each additional bit, leading to longer capacitor settling times. Lower sampling rate and lower input signal bandwidth are obtained as a consequence. Some solutions have been implemented to overcome the exponential growth of sampling capacitance of SAR ADCs. Fractional reference voltages are used in [5] for the last two bits, reducing the total capacitance by 4. But this requires the generation of two new reference voltages. An assisting 3-bit DAC

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computes rapidly MSBs in [6], providing enough time margin for the main DAC capacitance to settle during conversion cycles. Input bandwidth is reduced and power consumption is increased however due to the bigger main DAC and additional components. In [7], the input signal is sampled onto fixed capacitors that are not switched during the conversions. Comparator thresholds are modified instead to carry out binary search and determine the digital bits. This enables to have a sampling capacitance that is independent of the target resolution while increasing consequently the input bandwidth. However, the input range is kept small in order to ensure linearity of threshold variations with respect to the capacitive imbalance generated on comparator output nodes. Relatively low output resolution is thus obtained using a SAR architecture relying only on threshold configuring concept.

In this work, a hybrid architecture that combines a conventional Capacitive DAC (CDAC) and two asynchronously clocked threshold configuring comparators is presented. The resulting small DAC size provides a significant speed and bandwidth advantage, while the moderate resolution of the threshold configuring comparator (4-bit) allows for a higher target resolution. As a result, a 9-bit ADC achieving 1.3 GS/s sampling speed is implemented with this architecture. In Sect. 2, the architecture of the proposed design is presented. Section 3 goes deeper into details by exposing the circuit implementations and the calibration process. Simulation results are presented in Sect. 5 and 6 brings the conclusion.

2 Proposed architecture

The main building blocks of the proposed ADC and their respective interconnections are displayed on Fig. 1. The differential input signal is sampled using a high-speed and high-linearity bootstrapped switch, which is directly controlled by the external clock signal CK_{EXT}. The input signal is sampled at the top-plates of the CDAC. The V_{DACP} and V_{DACN} nodes of the CDAC are directly connected to the positive and negative inputs of the two comparators. The first five bits are obtained by performing binary search through the CDAC. Besides the clear area advantage, the resulting small CDAC size allows for fast and low-power switching as well as a high input bandwidth. Similarly to [5], two identical comparators are alternately clocked by signals CK_1 and CK_2 which are generated internally by the clock-generation block. The timing diagram of the related signals is shown in Fig. 2. The clock pulses are generated alternately so that one comparator is making a decision while the other is being reset. This design technique greatly enhances the conversion speed of the ADC. For the first 6 clock cycles, the DAC voltages V_{DACP} and V_{DACN} are settled using monotonic switching technique with split capacitors. The 6th clock cycle is a redundant bit. The voltage at the input of the comparators remains constant after the 6th comparison.

The two comparators are combined with a threshold control building block, which allows the ADC to implement the binary search algorithm by programming the input-referred threshold of the comparators. The last four bits are then obtained by programming the threshold of the comparators V_{th1} and V_{th2}. However, any mismatch in-between the two branches of the comparator can lead to an
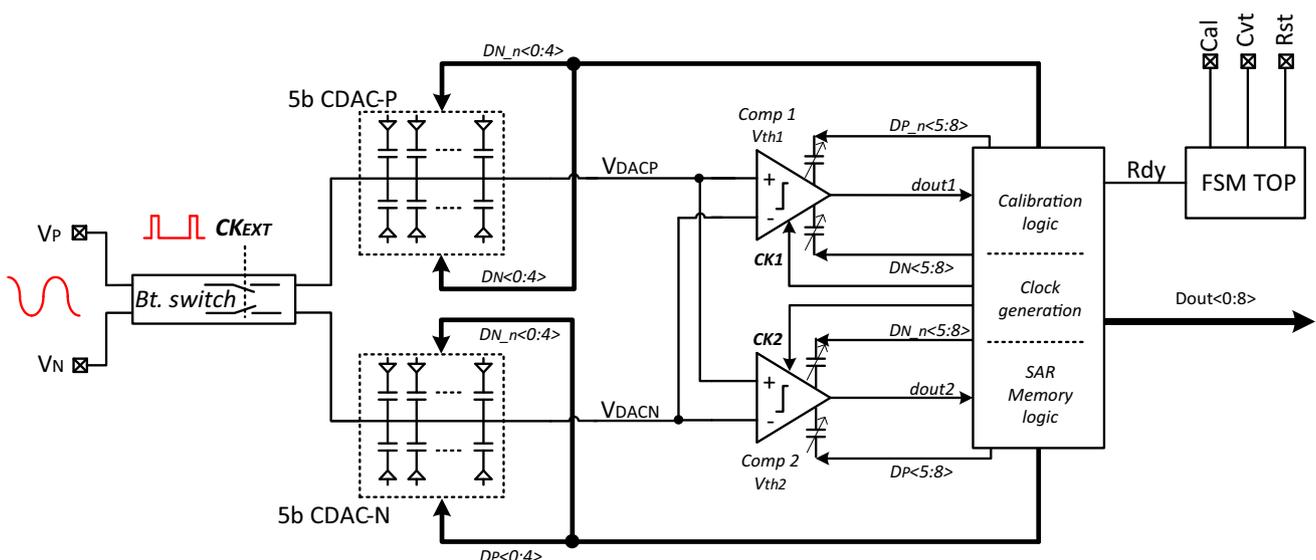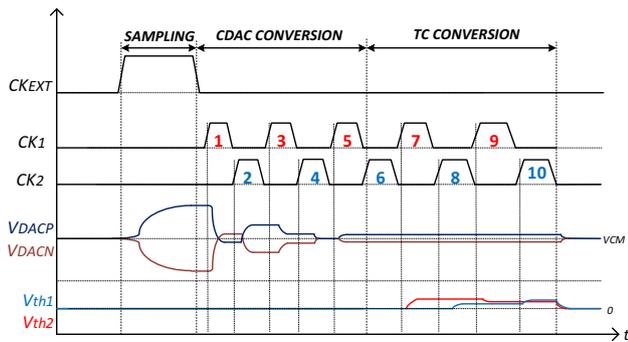

Fig. 1 Block diagram of the proposed ADC architecture

Fig. 2 Timing sequence of ADC operation

important initial offset, up to ± 40mV. Because of the amplification stage of the differential pair and the positive feedback latch, a small error can lead in a high offset difference. Using alternate comparators put the requirements of having zero-offset comparators. Since the digital bits are obtained alternately from one comparator and the other, offset mismatch between the two comparators will result in distortion and highly reduced performances. This is why a calibration circuit is implemented to correct the initial offset of the comparators.

The SAR memory logic block stores the decision outputs of the comparators and controls the CDAC and the threshold configuring mechanism. The output word for each sampled input consists of 10 comparison results. The first 5 bits are obtained from the CDAC. The last 4 bits are obtained from the comparator threshold control mechanism, which results in a 9 bit conversion at the end. There is no separate reset pulse at the end of the conversion. The CDAC and threshold control blocks are reset during the sampling phase in order to improve the overall conversion speed of the ADC. A basic Finite State Machine (FSM) controls the main operation of the ADC with respect to control pins Cal (for calibration) and Cvt (for conversion).

3 Circuit implementation

3.1 Top level FSM controller

A basic FSM is implemented to control and calibrate the ADC. Its corresponding diagram is presented in Fig. 3. After the initial reset from Rst signal, the machine is in **Idle** state. The Cal pin enables or disables the calibration of the threshold configuring comparators. If disabled, the machine goes into **Set Ready** state in which the Rdy flag is set to logic 1. This means that the ADC is ready to perform conversions. The machine goes to **Conversion** state when the Cvt signal goes high. The ADC starts operating as long as Cvt is logic 1 in this state. If calibration is enabled instead, the machine is set to **Calibration** state where
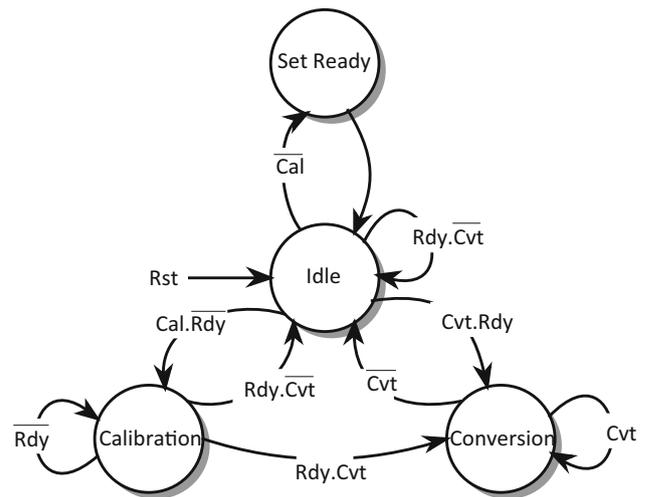

Fig. 3 Top level finite state machine

comparators are calibrated. The Rdy flag is pulled up at the end of the calibration. Regarding the logic state of Cvt signal, the machine goes either to **Conversion** mode directly, or returns to **Idle** state waiting for Cvt. In case of a new reset, Rdy is set back to logic 0.

3.2 Bootstrapped switch

The technique of bootstrapping presented in [8] is widely used nowadays in ADCs having more than 8 bit resolutions. Bootstrapped switches have been implemented as well in the proposed architecture since it presents a high linearity for a wide input range. The implemented circuit is presented in Fig. 4. It is the same design as in [8] but with a pMOS transistor M_{11} connected to V_{DD} and controlled by CK_{EXT}.

FDSOI technology allows body biasing of the transistors, changing considerably there threshold voltage. While sampling, the body voltage M_1 is forwardly biased to V_{DD}, reducing its threshold voltage and ON resistance. When sampling phase finishes, body voltage is backward biased,
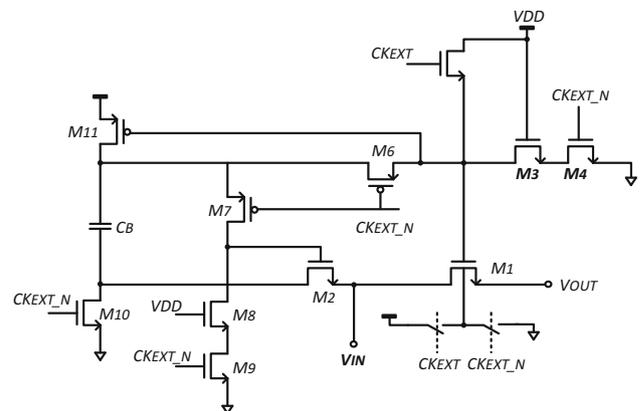

Fig. 4 Bootstrapped switch with dynamically biased body voltage

increasing the threshold voltage and reducing the charge leakage that could degrade SAR conversion accuracy. Although a negative voltage could have been applied as in [13] to maximize the threshold voltage, GND has been used in this case for simplicity.

3.3 Asynchronous clock generation

The clock generation mechanism implemented in this work is being referred to as asynchronous, because the internal comparator clock is not synchronized to an external clock. The nature of the binary search successive approximation algorithm dictates that the voltage at the inputs of the comparators is smaller than half the LSB voltage for only one out of ten comparisons. As a result, the duration of comparator clock pulses isn't restricted by worst-case decision time for all ten comparisons. The concept of generating clock pulses adjusted to the duration of each comparator decision was first introduced in [2] and has been proven to greatly improve the conversion speed of the ADC. The implemented asynchronous circuit is presented in Fig. 5. The clock generation circuit employs minimal combinatorial logic to generate the comparator clock signals. During sampling phase, CK_{EXT_N} is low, pulling down CK_1 and CK_2. The comparators being in reset mode, $COMP_1$ and $COMP_2$ are at logic 0, making the *init* signal high and node A_1 low. As soon as CK_{EXT_N} rises, $MP0$ is activated and CK_1 rises. A successful decision of comparator 1 generates a rising of $COMP_1$, which leads to the falling of CK_1 and the rising of CK_2. In the same manner, a successful decision of comparator 2 leads to the falling of CK_2 and the rising of CK_1.
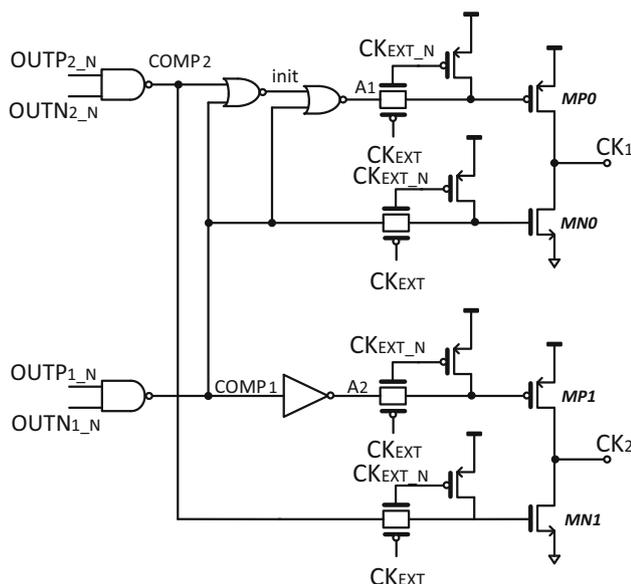

Fig. 5 Asynchronous clock generation

3.4 Capacitive DAC

The 5-bit CDAC in this work consists of two symmetrical capacitor arrays at each node, similarly to [5]. In this configuration, the digital outputs $D_P\langle 0:4\rangle$ and $D_N\langle 0:4\rangle$ correspond to the capacitors settling signals for the first five comparator decisions. These signals, as well as their complementary ones $D_{P\_n}\langle 0:4\rangle$ and $D_{N\_n}\langle 0:4\rangle$ are connected to the bottom plates of the binary-weighted capacitors of the CDAC, as shown in Fig. 1. The switching scheme implemented in this ADC maintains a constant common mode voltage in the DAC. This is crucial in order to avoid variations in the non-idealities and in the decision speed of the comparators. Furthermore, it maintains a high effective resolution of the threshold configuring comparators. Initially, all digital outputs $D_{P,N}\langle 0:8\rangle$ are set to V_{DD}. This means that half of the capacitors at each node are switched to V_{DD} and the other half to GND. No reference voltage or fractional reference voltages are used in order to reduce capacitor settling times. This comes at the expense of increasing the total capacitance in the DAC, but no reference generation circuit needs to be implemented in the ADC. The unit capacitor used in the CDAC is 2fF. This results in a total capacitance of approximately 182fF in the DAC.

3.5 SAR memory logic

The SAR Memory Logic is implemented similarly to [5]. For the proper operation of the ADC it is necessary that the CDAC and the comparator threshold control circuits have fully settled before the next comparison. For that reason, logic gates in the data path are asymmetrically sized to reduce propagation delays of high-to-low transitions of $D_{P,N}\langle 0:8\rangle$ feedback signals.

3.6 Threshold configuring comparator

The overall ADC conversion speed largely depends on comparator decision times in asynchronously clocked SAR ADCs. For that reason, the comparator architecture implemented in this work and displayed on Fig. 6 is the double-tail variation of the StrongARM latch [9].

This is a dynamic architecture controlled by the clock signals CLK and CLK_n. In the reset phase (CLK is low), the nodes P and Q are charged to V_{DD} by S_1–S_2 so that transistors M_3–M_4 discharge output nodes X, Y to GND. A rising CLK signal turns on transistors M_0 and M_9 so that M_1-M_2 and M_7–M_8 start conducting in saturation. A differential voltage $V_P - V_Q$ is accumulated because nodes P,Q are discharging at different rates depending on the differential input $V_{in+} - V_{in-}$. The difference in the gate
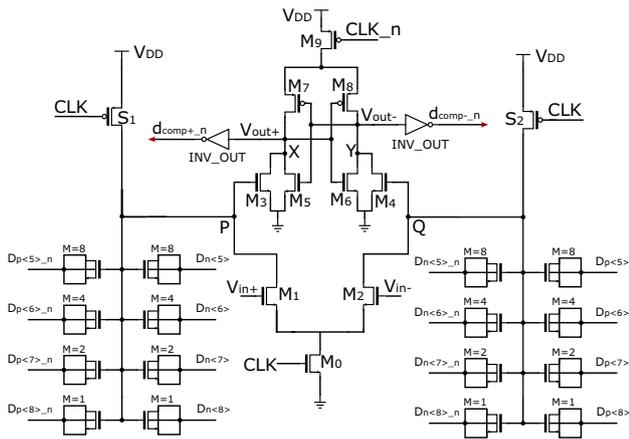
Fig. 6 Double-tail latch-type comparator with configurable threshold

voltages of M_3–M_4 causes output nodes X,Y to charge at different rates. As soon as transistors M_5-M_6 turn on, the accumulated difference $V_X - V_P$ is regenerated by the cross-coupled inverters. Finally, the output $V_{OUT+/-}$ corresponding to the larger input $V_{in+/-}$ rises to V_{DD} while the other output drops to GND.

The discharging rates of nodes P,Q not only depend on the differential input, but also on their load capacitances. The minimum differential input ΔV_{in} to counteract the effect of an imbalance in load capacitances of P,Q is defined as the threshold voltage and is given according to Eq. (1).

$$\Delta V_{in,thr} = V_{in+} - V_{in-} = \frac{2I_{CM}}{g_{m1,2}} \frac{C_P - C_Q}{C_P + C_Q} \qquad (1)$$

This effect was first used in [7] to implement a binary search algorithm by programming the comparator threshold. In this work two binary scaled symmetrical arrays (M = 1,2,...,8) of unit MOSCAP capacitors are implemented similarly to [10], where M indicates the number of unit capacitors. The source, drain, and body of capacitors are controlled by the digital feedback signals $D_{P,N}\langle 5 : 8\rangle$. For a high control voltage (V_{DD}), a MOSCAP device is in accumulation mode (OFF-state), so the effective capacitance at its gate is the sum of the gate-source and gate-drain overlap capacitances $C_{OFF} = C_{GS0} + C_{GD0}$. For a low control voltage the device is in strong inversion mode, so the effective capacitance includes the gate-channel intrinsic capacitance $C_{ON} = C_{GS0} + C_{GD0} + WLC_{OX}$. The resulting imbalance in the implemented comparator is given by

$$\frac{C_P - C_Q}{C_P + C_Q} = \frac{(N_{Pon} - N_{Qon})WLC_{OX}}{2NC_{OFF} + NWLC_{OX}} \qquad (2)$$

In the above equation N indicates the total number of unit MOSCAPs at each node P, Q. Even though the equation indicates a linear relationship between threshold voltage and capacitive imbalance, the dynamic range of such a configuration is limited. Indeed, the assumptions that

$g_{m1} = g_{m2}$ and that I_{CM} is independent of the differential ΔV_{in} are no longer valid for large ΔV_{in}. As a result, published works on SAR ADCs using solely the comparator threshold configuring technique report a limited dynamic range and a target resolution not exceeding 6 bits. Implementing a hybrid SAR architecture allows us to benefit from the area-efficiency and power-consumption advantages of threshold-configuring comparators, while operating them at an input range where the binary search algorithm can be implemented with high accuracy.

3.7 Comparator offset calibration

Alternate comparators bring a real speed advantage but come at a price of offset compensation. Since two different comparators are used, offset cancellation is required for the accurate operation of the ADC. A similar approach to the calibration process of [11] is used to reduce comparators offsets in the foreground. The relative circuit is presented in Fig. 7 and the signals transient response is presented in Fig. 8. An additional differential pair $M_1 - M_2$ is added in parallel to the comparator main differential pair. While the gate M_1 is connected to the common mode voltage V_{CM}, the gate of M_2 is controlled by the calibration circuit. [11] is based on the charge and discharge of a capacitor that hold V_{CAL}. This requires a recharge after some time in order to prevent capacitor leakage. In order to avoid an additional clock cycle to update the capacitor charge and dismiss capacitor leakage problem, a current DAC based voltage biasing is applied. A 6-bit counter increments at each clock cycle, increasing the current steering DAC tail current. To keep a relevant variation range, resistors R_1 and R_2 are added. There is no need of having high voltage variations for V_{CAL}. The ratio between the current flowing in R_2 and the current flowing in the DAC determines the voltage steps at each counter incrementation. The smaller R_2, the smaller are the steps but the bigger is the static current consumption. The resistance value of R_1 is then fixed to set the initial voltage level of V_{CAL} The DAC current is set to vary by
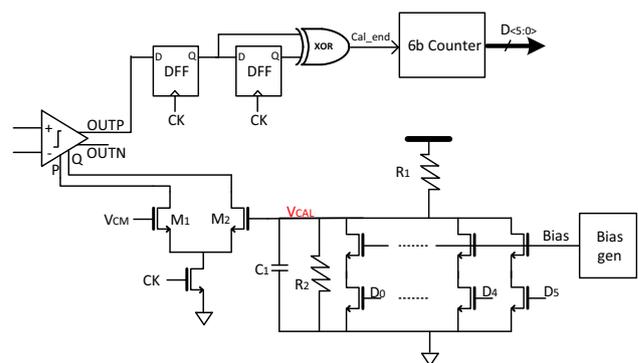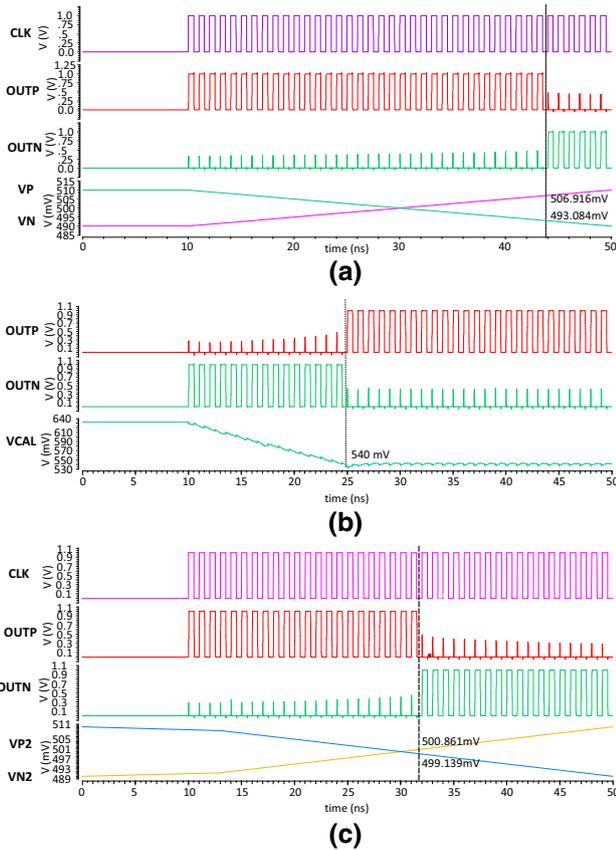

Fig. 7 Comparator calibration circuit

Fig. 8 Comparator calibration simulation: **a** offset before calibration, **b** calibration process, **c** offset after calibration

± 130 mV around V_{CM}. It provides a decreasing bias voltage V_{CAL} to the gate of M_1 during the process. When the crossing point is reached, the comparator outputs change their states. A XOR-based circuit detects the state change and stops the counter at its last value.

A 10% mismatch has been intentionally introduced into the transistor M_3 of the comparator (Fig. 6) to illustrate the calibration process. The initial offset of the comparator is measured as 7 mV when $V_{CAL} = V_{CM}$, as shown in Fig. 8(a). The calibration runs and V_{CAL} sets on 540 mV, as in Fig. 8(b). After calibration process, the offset voltage is reduced below 1mV, as shown in Fig. 8(c).

4 Simulation results

The ADC proposed in this work was designed in 28 nm FDSOI technology. The differential input dynamic range of the ADC ranges from -640mV to $+640$ mV with a common mode of 500 mV, which results to an LSB voltage of 2.5 mV. The period of the external clock is chosen at 780ps which results to a sampling frequency of approximately 1.28 GHz. A 1.0 V supply is used for all building

blocks of the ADC, and a total power consumption of 4.1 mW is simulated. The power consumption breakdown among the different blocks is presented in Fig. 9. Unlike to conventional architectures where DAC switching energy is the dominant source of power consumption, this topology has an almost negligible DAC switching energy consumption. The main reason is the reduced size of the CDAC (5-bit) and the use of monotonic switching. The highest power consuming block is the internal clock generation with 1.6 mW. Even if the corresponding circuit is not dense, it generates clock pulses in very short periods which results in a very high power consumption. The two comparators have a common consumption of 1.1 mW.
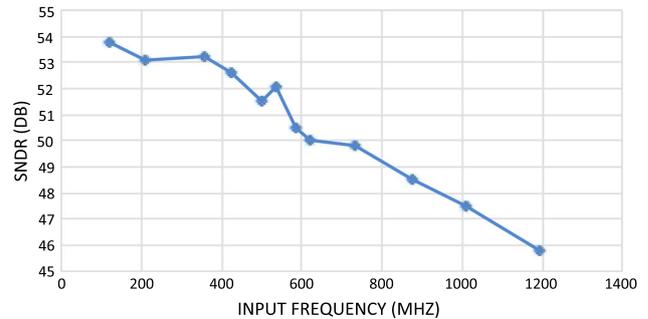

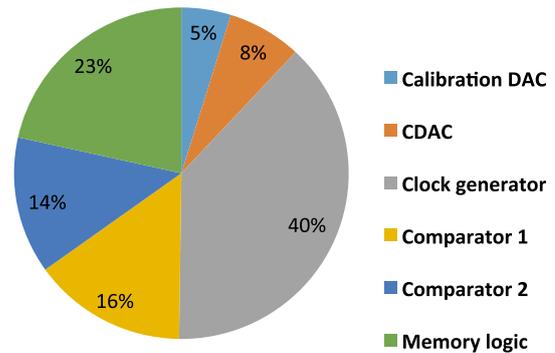**Fig. 9** Power consumption distribution

Power Consumption

- Calibration DAC
- CDAC
- Clock generator
- Comparator 1
- Comparator 2
- Memory logic

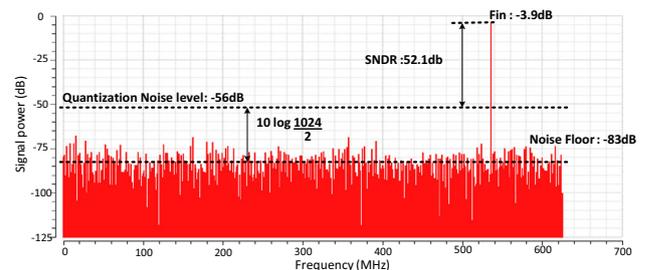**Fig. 10** SNDR with respect to input frequency

Fig. 11 Frequency spectrum of the reconstructed signal

Table 1 Comparison of results

	This work (Simulation)	Kull [5] (Chip)	Hong[12] (Chip)	Nuzzo [7] (Chip)
Architecture	CDAC-TC Hybrid	CDAC	CDAC 2b/cycle	TC
Technology	28 nm FDSOI CMOS	32 nm SOI CMOS	45 nm CMOS	90 nm CMOS
Supply Voltage	1 V	1 V	1.2 V	1 V 0.7 V
Sampling Rate	1.3 GS/s	1.2 GS/s	900 MS/s	50 MS/s
Resolution	9b	8b	9b	6b
SNDR (Nyquist)	52.1 dB	39.3 dB	51.2 dB	32 dB
Power Consumption	4.1 mW	3.1 mW	10.8 mW	0.24 mW
FoM [fJ/step]	11.4	34	40	150

Although both comparators are identical, a small difference in their power consumption is remarked. Even if both comparators have the same number of conversion cycles, that is 5, the capacitor switching is more power hungry in comparator 1. The first switching consumes higher power than the others and threshold configuring starts always with comparator 1 at the 7th clock cycle. The rest of the power is distributed as 0.3 mW for the bootstrapped switches and the capacitive DAC, 0.9 mW for the SAR memory block and 0.2 mW for the calibration current DAC. The latter have a static power consumption due to resistors R_1 and R_2. Depending on the calibration voltage V_{CAL}, power consumption of 1 calibration DAC could vary from 60 to 100 μA.

Simulation results for the static performance of the ADC show an INL below 0.58 LSB and a DNL below 0.83 LSB.

The dynamic performance of the ADC is tested by driving the input with an ideal differential sinusoidal wave covering the full dynamic range (640 mV peak-to-peak amplitude). Figure 10 shows the Signal-to-Noise-and-Distortion (SNDR) for input frequencies between 100 MHz and 1 GHz. The results were obtained by computing a 1024-point FFT on the digital output samples. The spectrum for an input frequency of 535 MHz is shown in Fig. 11. The simulated SNDR is 52.1 dB from which an ENOB of 8.4 bits is obtained. The resulting FoM near the Nyquist frequency is 11.4 fJ/conversion-step with respect to the expression in (3).

$$FoM = \frac{Power}{2 \cdot f_{in} \cdot 2^{ENOB}} \qquad (3)$$

5 Conclusion

In this paper a single-channel hybrid ADC architecture has been presented. It combines the traditional charge redistribution principle in the CDAC and configurable comparator thresholds. It also uses asynchronous timing and alternately clocked comparators in order to achieve high power efficiency in high-speed operation. The architecture proposes a much smaller CDAC in the front-end, that is 5-bit instead of 9. This enables lower silicon area, less switching power consumption, increased input bandwidth and higher operating speed due to shorten logic-to-capacitor delays. Thus, this topology is highly suitable to be implemented in time-interleaved architectures in order to reach sampling rates greater than 10 GS/s. Table 1 compares the performance of this ADC with related state of the art single-channel SAR ADC. It indicates that such a hybrid design overcomes the performance limitations of the main circuit techniques when treated separately, so that such an architecture is proven promising to be implemented on chip.

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