Analog Integrated Circuits and Signal Processing (2018) 96:21–38
https://doi.org/10.1007/s10470-018-1208-3

A comprehensive survey on UHF RFID rectifiers and investigating the effect of device threshold voltage on the rectifier performance

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Received: 21 June 2017 / Revised: 10 May 2018 / Accepted: 12 May 2018 / Published online: 17 May 2018

Abstract
Rectifiers are an integral part of power harvesting systems. In this paper, the literature on RF power rectifiers is surveyed, starting from the well-known voltage doubler. Effects of using low turn-on voltage devices on forward and reverse losses, and therefore, on conversion efficiency, is discussed. Samples of rectifiers with external devices, such as Schottky diodes are presented. Idea of external V_{th} cancellation through a rechargeable battery, self V_{th} cancellation, and floating gate transistors with charge injection onto the gates are demonstrated. Then, standard bridge rectifier and its modified versions, including V_{th} cancellation technique, are explained. Using low voltage devices in other technologies, such as silicon on sapphire and silicon on isolator are also discussed. After literature survey, the bridge rectifier is studied in detail, to extract guidelines for efficiency enhancement. Bridge rectifier has high PCE, because the transistors have a dynamic bias that lowers their forward and reverse losses, simultaneously. Then, the effect of transistor threshold voltages on the bridge rectifier performance is investigated. We propose to shift peak region in the efficiency curve to a desired output voltage, based on which, two modified rectifiers are introduced. A single stage modified bridge rectifier is proposed with 3.3 V transistors, that achieves efficiency of around 80% at 0.9 V output. Then, a two stage modified bridge rectifier is proposed, that uses a combination of 1.8 and 3.3 V transistors to remove the need to source-bulk connection in NMOS transistors (that requires triple-well CMOS technology). Simulations predict around 80% efficiency at 1.7 V output.

Keywords UHF RFID · Rectifier survey · Power extraction · Wireless power transfer · Bridge rectifier · Standard digital CMOS

1 Introduction

Very low cost fully passive UHF RF power extraction systems are desired for several applications such as Radio Frequency IDentification (RFID), wireless sensor networks, Internet of Things (IoT), wireless power transfer for biomedical implants, etc. Among these applications, especially the applications of RFID technology are extended from simple ones, such as monitoring and management systems for buildings, through more sophisticated ones, such as open-air events or logistics [1]. All of those are wireless sensing applications, and need ultra-low power IC design, long system reading range, and small tag size [2]. One of the major goals of today research efforts is the improvement of the operating range, which is desired for many RFID applications, such as supply chain management, intelligent transportation systems, etc. [3, 4]. This improvement requires better antenna design and/or using

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higher performance circuits, which can happen in the design of the reader and/or tags.

In the design of tag, based on the tag application, active or passive tags can be used. In applications where reading range is a priority and higher cost can be tolerated, active tags are used, which can offer high reading ranges. Active tags need external battery that provides the supply voltage. So, there is no need to extract power from the input signal. However, because of their battery, the final product would have a larger size and higher weight, and would need battery replacement over time, that leads to a higher total system cost.

On the other hand, passive tags have less operating range compared to active ones. However, they are designed without a battery, and therefore can be built in small sizes, and much lower prices in case of mass production. In passive tags, power is extracted from the reader transmitted RF signals [3]. To overcome the problem of short operating range, passive tags are usually used at high frequencies, such as Ultra High Frequency (UHF) band of 900 MHz, which is available worldwide. Other bands are also available for shorter ranges, including Low Frequency (LF) band of 125 kHz and High Frequency (HF) band of 13.56 MHz. Operating in the UHF band results in antenna length reduction and small size tag design.

In a RF power extraction system, rectifier, or the RF-to-DC circuit, is the main building block, which converts the incoming RF signal power into a suitable DC voltage. This voltage is used to supply the succeeding blocks, including analog front end circuits such as modulator and demodulator, and analog and digital baseband circuits. Investigation into the efficient design of the rectifier circuit is the focus of this paper. Output DC voltage and Power Conversion Efficiency (PCE) are two main specifications of a rectifier, which are used for evaluation and performance comparison among different rectifier architectures.

As a passive tag obtains its power from the incoming reader RF carrier signal, and not from a battery, designing simple and power-efficient circuits, compatible with such small powers, is rather a complicated issue. To achieve a low power design, many researches are focused on power-hungry blocks such as modulator [4] and demodulator [5] blocks. Some others have investigated the use of different technologies, such as silicon on sapphire (SOS) [6], organic thin film transistor (OTFT) [7], and silicon on isolator (SOI) [8]. Using some technologies other than the digital CMOS, and also taking advantage of external components, such as Schottky diodes could be helpful in the design of high efficiency rectifiers, by providing low threshold voltage transistors or low voltage drop diodes. However, using those technologies or external components are not suitable for low cost applications. Therefore, power efficient circuit design techniques in digital CMOS technology are usually considered for the tag implementation.

In this paper, first, a literature survey is presented on the most important rectifier circuits and topologies. The circuits start with the well-known voltage doubler, and are improved in several steps, until they reach to the recognized bridge rectifier, and the enhancements that are done on this type of rectifier. Then, the bridge rectifier is studied in detail, to extract guidelines for efficiency enhancement in the bridge rectifier. We propose to shift peak region in the efficiency curve versus output voltage to a desired output voltage, by changing voltage threshold of the transistors. Such a voltage shift makes the rectifier suitable for supplying the tag circuits, which require a higher supply voltage for proper operation. Two modified rectifiers are then introduced, that are designed in 0.18 μm CMOS technology. In the first design, we propose to use 3.3 V transistors instead of 1.8 V ones. As a result, an efficiency of around 80% is achieved at 0.9 V output DC voltage, which is enough for supplying the tag digital circuits. To further increase the optimum output voltage, a two-stage rectifier is also proposed in this paper, in which, around 80% efficiency is achieved at 1.7 V output voltage. Such a voltage is suitable for supplying analog and RF circuits.

The rest of the paper is organized as follows. In Sect. 2, a background is provided for the contents of the paper. Section 3 provides a comprehensive review on the previous work on rectifiers, followed by a detailed simulation and analysis of the well-known bridge rectifier, in Sect. 4. In Sect. 5, the modified rectifiers with transistor threshold adjustment to improve efficiency and reduce fabrication costs, and also their simulation results are presented. Finally, conclusions are drawn in Sect. 6.

2 Background

Part of the background required for this paper is presented in this section, which includes an explanation about the digital CMOS technology, followed by description of an RF power extraction system.

2.1 Standard digital CMOS technology

In the standard digital CMOS technology, neither the option of Metal–Insulator–Metal (MIM) capacitor, nor the option of triple well is available. The MIM capacitor option allows to have passive capacitors that ideally have no noise. Also, their capacitance remains constant across their operating voltage range, which could be much higher than voltage range of MOS capacitors. Therefore, they are suitable for RF and precise analog applications. However, their density is much less than that of MOS capacitors. On

the other hand, the triple well option adds a deep N-well layer to the fabrication process, which makes possible to have P-wells inside N-wells. Isolated NMOS transistors can be built inside these P-wells, and are allowed to have body-source connection; therefore, body effect is removed. Also, the threshold voltage is not increased due to the V_{SB} voltage. These two options, MIM capacitor and triple well, would be available in CMOS technology at extra fabrication costs.

2.2 Structure of an RF power extraction system

A complete RF power extraction system is shown in Fig. 1(a). The antenna receives the RF signal. Maximum power is transferred to the system by the matching circuit, and then, the rectifier extracts a DC voltage from the received RF signal.

In the resonance frequency, i.e., the frequency that the antenna is designed to work in, imaginary part of the antenna impedance can be approximately neglected [10]. Also, the ohmic resistance of the antenna is negligible. Therefore, the antenna is modeled as an open circuit voltage source, V_{RF}, in series with the radiation resistance, R_R, as shown in Fig. 1(b). In order to achieve maximum efficiency, the antenna impedance should be matched to the tag input impedance. This is performed by an LC matching circuit [11]. Also, an adaptive matching can be used where the tag input impedance changes during the circuit operation [12].

Rectifier is the most important building block of an RF power extraction system. This circuit supplies the required DC power for the rest of internal circuits of the tag. The power that reaches the tag internal circuits is given by $P_{Tag} = \eta_{Rectifier} P_{available}$. Here, $P_{available}$ is the available power at the tag input and $\eta_{Rectifier}$ is the rectifier efficiency. Therefore, to increase the reading range, one should provide a good matching between antenna and the tag, to increase $P_{available}$, and also design a high efficiency rectifier to improve $\eta_{Rectifier}$.

Rectifiers are nonlinear and their input impedance is changed instantaneously by the input voltage and output current. Therefore, it is difficult to analyze them in time domain. Also, presenting a changeless circuit model for their input impedance is not possible [13]. However, using a matching circuit between the antenna and the tag, higher order harmonics of the input impedance are eliminated and fundamental frequency impedance approximation becomes reasonable [11]. In the steady state, the input impedance can be assumed constant, which is modeled by a resistance in parallel with a capacitance.

3 Previous work on rectifiers

In this section, conventional structures for the rectifiers are presented, followed by modifications introduced in the previous work. The structures start with voltage doubler and reach to the bridge rectifier and its modified versions.

3.1 Voltage doubler

A voltage doubler is the simplest form of a rectifier, which charges capacitors from the AC input voltage and transfers the charges to the output in such a way that ideally twice the maximum input voltage is produced at the output. Two

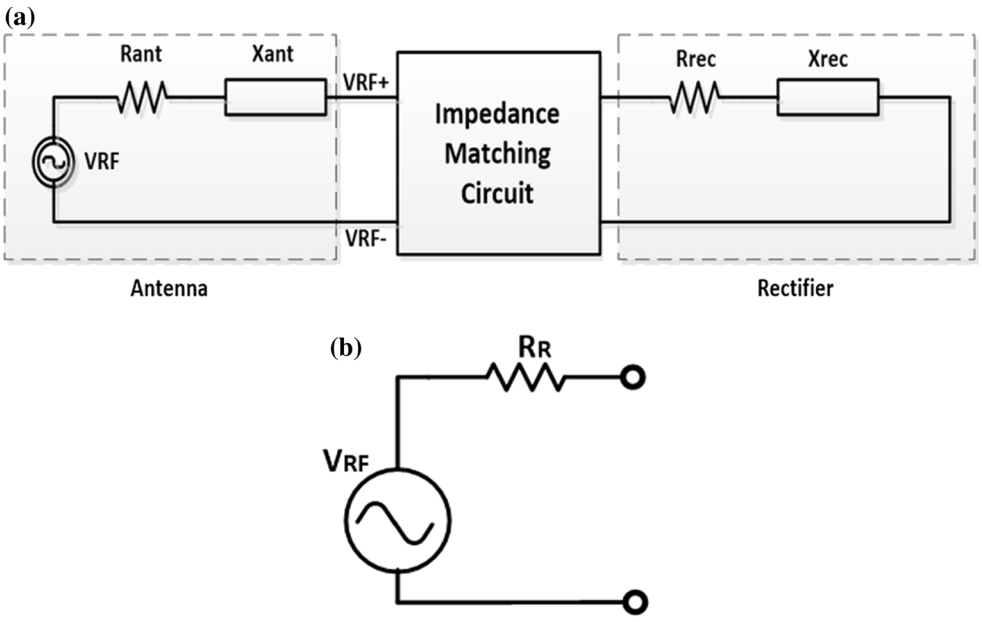


Fig. 1 **a** A complete RF power extraction system [9], **b** equivalent circuit of the antenna at the resonance frequency

well-known rectifiers, namely Dickson and Cockcroft–Walton, are derived from the voltage doubler rectifier.

The structure of a voltage doubler is shown in Fig. 2 and is composed of a clamp circuit, C_1 and D_1, and an envelope detector, D_2 and C_2. In the negative half cycle of the input voltage, the input capacitance C_1 is charged by the diode D_1 to $V_{peak} - V_{D(ON)}$ in the shown direction, and in the positive half cycle, the capacitance C_2 is charged to 2 $(V_{peak} - V_{D(ON)})$ by diode D_2.

The conventional CMOS doubler circuits use diode connected transistors as diodes. The turn-on voltage of diode connected transistors are almost equal to the transistor threshold voltage. Thus, only if the input signal is larger than the threshold voltage of transistors, the doubler works well. Therefore, using this simple structure with diode connected transistors would have low power efficiency, and therefore, is not suitable for high efficiency rectifiers.

Using low turn-on voltage devices, as the rectifying elements, is the simplest method to increase efficiency. However, this efficiency increment will be limited by reverse leakage current, since, decreasing the turn-on voltage leads to more reverse leakage current and consequently higher power consumption. Moreover, this method needs more fabrication process steps, which leads to more cost.

Implementing the rectifier in newer CMOS technologies takes advantage of the lower threshold voltage of the devices, while the digital and analog blocks also take advantage of lower voltage and lower power operation. However, these advantages come at the higher cost of technology. In [15], a rectifier (with bridge topology, as will be explained in Sect. 3.2) is presented, which is implemented in 0.13 µm CMOS technology and achieves a peak efficiency of 60%.

Using external devices with low turn-on voltage is a conventional technique. Reference [16] utilizes a 2-stage Dickson rectifier implemented by Schottky diodes. The rectifier is realized on a PCB with FR4 substrate using a photolithographic process, and other blocks are realized in 0.18 µm CMOS technology. This converter operates in 866.5 MHz and provides a sensitivity (i.e., minimum detectable RF power) of − 26 dBm. Another rectifier is reported in [17], which operates in the HF band and consists of a 4-stage Dickson rectifier with Schottky diodes. A sensitivity of − 19 dBm is achieved, as a result of using those external devices. The next blocks are fabricated in 0.35 µm CMOS technology, including a voltage monitor that holds the output voltage in the range of 1.8–2.4 V. Using external devices, while may increase the sensitivity and the reading range, does not result in a fully integrated solution, and therefore, causes the implementation cost to increase.

For fully integrated rectifiers, external V_{TH} cancelation is an idea that decreases the transistor threshold voltage with use of a switched capacitor circuit, as shown in Fig. 3. M_1 and M_2 are diode connected transistors in the voltage doubler. The two capacitors, C_{b1} and C_{b2}, in their gate terminals are then used as a battery to eliminate the threshold voltage effect. The voltage of these capacitors will be built up and made stable by a voltage distributer, which is a switched-capacitor circuit. This circuit, in turn, is supplied by a rechargeable battery. After the rectifier is setup, i.e., reaches the steady state and starts its normal rectification process, the battery is re-charged for the next start up process of the rectifier. Herein, battery increases the power efficiency and therefore reading range, however, results in increase in the weight, volume, and cost of the tag, and at the same time reduction in the useful life of the device. A six-stage rectifier using this idea is presented in [18].

Self (i.e., internal) V_{TH} cancelation is another method that decreases threshold voltage using the DC voltage produced by the rectifier circuit itself [19, 20]. The general implementation method is shown in Fig. 4. The gate of NMOS transistor is connected to a higher voltage and the

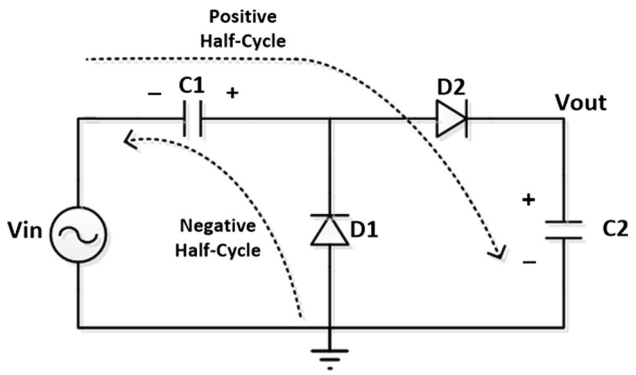


Fig. 2 Conventional voltage doubler [14]

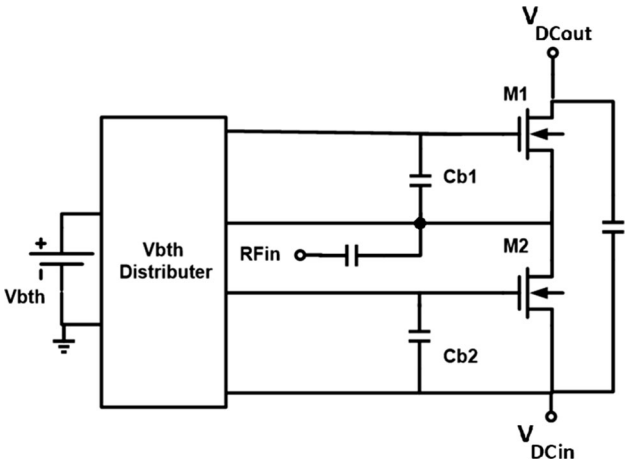


Fig. 3 External V_{TH} cancelation [18]

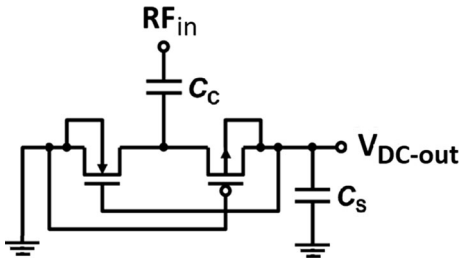


Fig. 4 Self V_{TH} cancelation [21]

gate of PMOS transistor is connected to a lower voltage, and therefore, part of the threshold voltage effect is cancelled. This is performed by connecting PMOS gate to the ground node, and NMOS gate to the DC output node. By turning on the circuit, over time, some amount of voltage is built up in the output and the effect of the threshold voltages is gradually reduced. This circuit does not require an external power supply and can be completely implemented in a standard low cost digital CMOS technology. However, as it just decreases the forward loss, not the reverse loss, the power efficiency improvement is limited.

To separately adjust threshold voltage of each transistor, floating gate transistors are used in [9]. The threshold voltage is adjusted after fabrication, using charge injection onto the floating gate. A voltage doubler using this technique is shown in Fig. 5. In this figure, V_{DCin} is the DC output of the previous stage, when this circuit is used in a multi-stage rectifier to achieve a higher output voltage. In this technique, the optimum threshold voltage for each stage is first calculated, and then, adjusted by a long and costly process, after fabrication. Two methods are proposed for charge injection. Firstly, via Fowler–Nordheim tunneling, when the rectifier is not operating, and secondly, by injecting a relatively large sinusoidal signal to the rectifier input, at any time. The first method is faster, but the amount of charge is harder to control. Using the floating gate transistors, a 36-stage rectifier is designed in [9] and fabricated in 0.25 μm CMOS technology. By programming the tag with the best operating voltage of each stage, the rectifying elements work as near zero threshold voltage elements. As a result, a high sensitivity of − 22.6 dBm is achieved. Also, a maximum power efficiency of 60% at 1 V DC output voltage is reported.

Using ultra-low voltage diodes in SOI technology is another efficient way in rectifier design. In this structure, shown in Fig. 6, two low threshold voltage SOI transistors are connected to each other in such a way that the turn-on voltage of this diode is equal to threshold voltage of each transistor. Therefore, the forward loss is lower than that of a standard MOS transistor [14].

The difference between this SOI diode and a diode connected transistor is in the reverse bias mode. When a normal diode connected transistor is in reverse bias, the drain and source terminals are changed, so, the gate is connected to source, i.e. V_{GS} equals zero. Therefore, there is a leakage current. In reverse bias of the ultra-low power diode in Fig. 6, the sources of both NMOS and PMOS transistors fall on the middle node, and this node voltage is almost the average of the diode terminals voltages. Therefore, by increasing the reverse bias voltage, the V_{GS} of NMOS transistor becomes more negative and the reverse leakage current is decreased. Thus, the reverse loss is reduced. This structure, proposed in [14], is the only voltage doubler that decreases the forward loss and the reverse loss, simultaneously. However, this circuit is not cost efficient, as it uses a costly technology. It should be noted that such a circuit is not useful for CMOS technology, since standard CMOS suffers from forward loss, which is not improved by this technique.

In any of the above rectifiers, several stages can be used in series to increase the output DC voltage. As a result, the output voltages are added to each other. Furthermore, in some applications, the voltage doubler circuit or other rectifiers can be used with sub-threshold currents. In a recent publication, sub-threshold operation of the Dickson rectifier is investigated and a model is proposed for prediction of the circuit behavior [22].

3.2 Cross coupled bridge rectifier

Changing the structure of the rectifier is another way to increase power efficiency. Cross coupled bridge rectifier, or

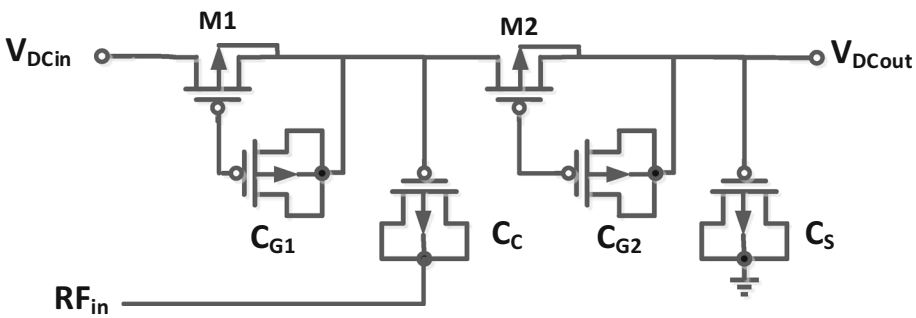


Fig. 5 A voltage doubler with floating gate transistors [9]

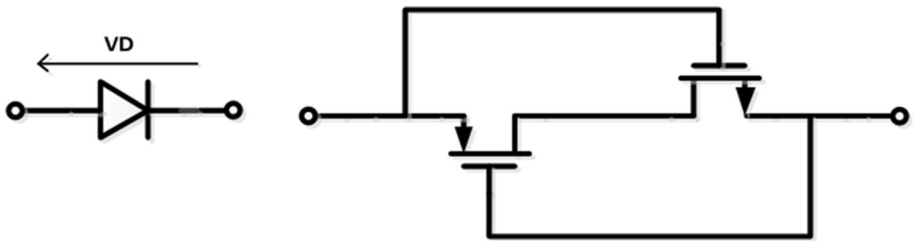


Fig. 6 The ultra-low voltage diode in SOI technology [14]

bridge rectifier in short, is the most power efficient one, as it decreases forward and reverse losses, simultaneously, similar to the SOI ultra-low power diode. This rectifier was primarily used for rectifying low frequency signals, until 2007 that Facen and Boni [23] showed that it could be used also for rectifying UHF signals. The circuit is shown in Fig. 7. The principle of operation is similar to an H-Bridge rectifier. In the positive cycle of input, M_1 and M_4 are ON and the other two transistors are OFF, and in the negative cycle of input, the opposite is true. As a result, V_{out} would be positive. This circuit will be discussed in detail, in Sect. 4. For proper operation of the bridge rectifier, a differential input larger than sum of the threshold voltages, i.e., $V_{th\text{-}NMOS} + |V_{th\text{-}PMOS}|$, is needed. To solve this problem, all techniques explained above for reducing or removing V_{th} effects can be utilized here, as well. Some samples of previous work on bridge rectifiers are explained in the following.

One solution is fabricating the bridge rectifier circuit in silicon-on-sapphire (SOS) technology. In this technology, intrinsic near zero threshold voltage devices are available. Designing a rectifier with such devices results in activating the rectifier, even with near zero RF input voltages. An example of such a rectifier circuit is shown in Fig. 8 [24]. An important issue of using near zero V_{th} devices in the bridge rectifier is leakage of current from output capacitor back to the input, when the input is changing polarity. Also, when RF inputs achieve a common positive DC bias, there would be a leakage current. According to Fig. 8, four transistors are added between cross coupled NMOS and

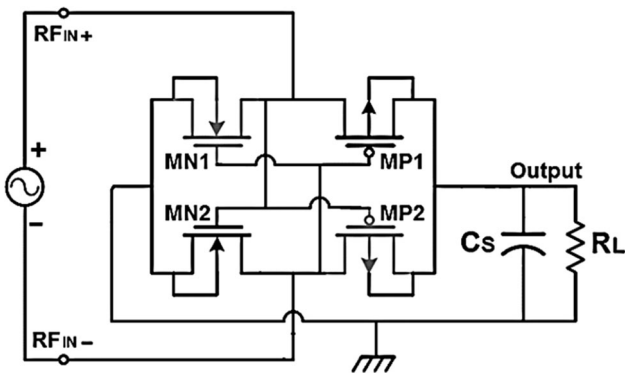


Fig. 7 Cross coupled bridge rectifier, or bridge rectifier, in short

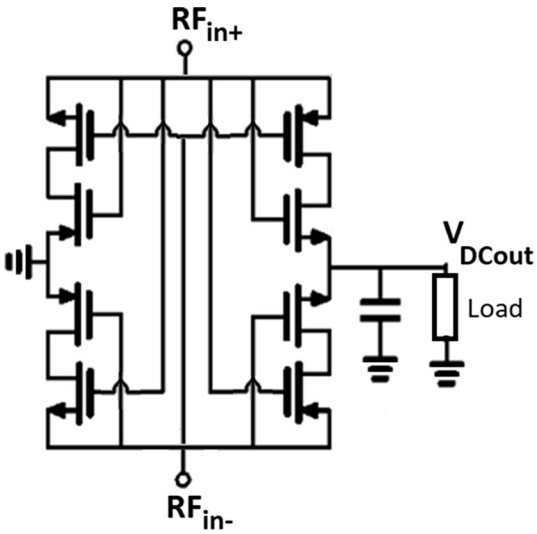


Fig. 8 The modified bridge rectifier circuit in SOS technology [24]

PMOS transistors. These transistors would block the leakage current, and as a result, the efficiency is improved. However, this rectifier circuit is not cost effective, as it uses a costly technology, and it cannot be integrated with other digital/analog circuits that are easily implemented in a standard digital CMOS technology.

Another solution is to use newer CMOS technologies, at the expense of higher cost of implementation. In [15], a reconfigurable topology for the rectifier with 2 or 4 stages is proposed, in which, using a switch network and a control signal in the rectifier architecture, two bridge rectifiers are connected in series or in parallel, and as a result, output DC voltage is increased. Also, a smart voltage regulator is used to keep the converter output voltage constant at the reference voltage. Implemented in 0.13 μm CMOS technology and operating at 868 MHz, a peak efficiency of 60% is achieved. Also, the reconfigurable structure of the rectifier and lower voltage threshold of 0.13 μm CMOS devices resulted in a good sensitivity of − 17 dBm.

Another improvement on the bridge rectifier is biasing the gate of the cross coupled transistors, as shown in Fig. 9 [25]. As a result, the effect of threshold voltages is reduced. However, this circuit needs a battery or another external energy source for initial charge of capacitors, to prepare V_{OS} voltages in the gates.

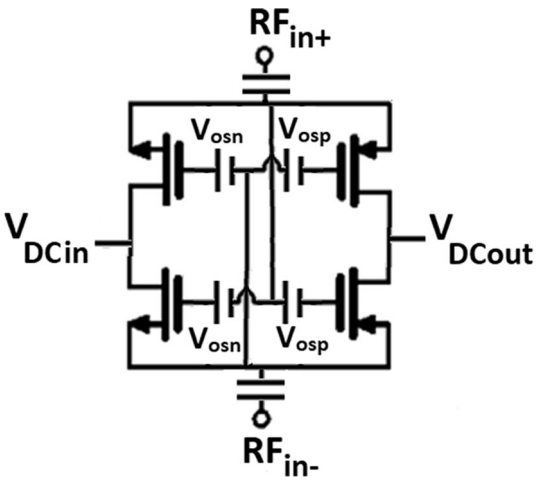


Fig. 9 Biasing the transistors of bridge rectifier to reduce the effect of V_{th} [25]

3.3 Summary

In this section, a number of important published designs in RFID energy harvesting was investigated and the effect of the devices threshold voltage on their performance was discussed. Table 1 provides a comparison between the presented ideas, their pros and cons, and also a performance summary of the abovementioned references.

4 Analysis of the bridge rectifier operation

Bridge rectifier is the most conventional circuit topology, due to its high efficiency. In this section, this structure is discussed in detail. The circuit was previously shown in Fig. 7. When a differential RF input signal larger than device threshold voltages is applied to bridge rectifier, one pair of transistors, a NMOS and a PMOS, turns on, and the other pair turns off. In the next half cycle, the opposite happens. This operation results in rectification of the input signal, and produces a DC voltage at the output port. Also, a DC voltage would also appear at the RF input port, that is almost half the output voltage in the steady state [24, 26], as shown in Fig. 10.

Part of the power entered into the rectifier appears as the power loss, P_{loss}, and the remaining part appears at the output, as P_{out}. There are two sources of losses in the bridge rectifier, including forward loss of transistors channel resistance, R_{ON}, and reverse loss of the leakage current, I_{LEAK}. High efficiency of bridge rectifier is the result of biasing the gates of transistors dynamically, so that their forward and reverse losses are reduced, at the same time. Part of the bias is a DC voltage, through which, the threshold voltage is partially cancelled out. The other part is a variable or an AC voltage that comes from the input RF signal, and reduces R_{ON} in the positive and I_{LEAK} in the negative input half-cycles [21]. The abovementioned DC part has different sources for NMOS and PMOS transistors. For the NMOS transistors, the V_{DC_N} voltage comes from the DC voltage developed at RF input port with respect to ground, and for the PMOS transistors, the V_{DC_P} voltage originates from the DC voltage difference between input and output ports, as shown in Fig. 10. Therefore, we can write $V_{DC\_N} + |V_{DC\_P}| = V_{DC\_OUT}$.

Maximum efficiency is achieved at an optimum DC bias for each transistor, which is related to its threshold voltage. Below that optimum voltage, forward loss because of high channel resistance, and above that level, reverse loss due to high leakage current become dominant. Since this DC bias voltage is a portion of the output DC voltage, maximum efficiency is achieved at a specific output voltage. This is shown in Fig. 11. Such a concept is presented in more detail in a thesis from our research group [27]. According to the simulation results shown in this figure, from the single stage bridge rectifier designed in 0.18 µm CMOS technology, an optimum output voltage of only 0.65 V is achieved. However, this low voltage is not enough for supplying the tag circuits. In fact, it is required that maximum efficiency to occur at a higher V_{DC_OUT}. In the next section, we play with the transistor threshold voltages, to achieve the required performance, in the bridge rectifier.

5 Investigating threshold voltage effect on bridge rectifier performance

In this section, we investigate the effect of transistors threshold voltages on the bridge rectifier performance, by designing two modified rectifier circuits, with different threshold voltage devices.

The first modified rectifier, shown in Fig. 12(a), has the conventional structure of Fig. 7, but with 3.3 V transistors. These transistors are available in the standard 0.18 µm CMOS technology at no extra cost. The 3.3 V transistors are chosen because of their higher threshold voltages. As a result, their optimum DC biases are higher, and therefore, the maximum efficiency occurs at a higher output voltage, while the efficiency is not compromised. In fact, we can shift the peak region in the efficiency diagram to a higher output voltage by changing the devices threshold voltages. Simulations show that the threshold voltage for 3.3 V PMOS transistors are around 0.65 V. Therefore, by changing the threshold voltages from 0.45 V for 1.8 V PMOS transistors to 0.65 V for 3.3 V PMOS transistors, it is expected that the optimum V_{DC_out} is also increased by 0.2 V or so. Therefore, this single stage rectifier can be used to supply digital circuits and low voltage analog circuits [28].

Table 1 Comparison between previously published ideas in RFID energy harvesting, their pros and cons, and a performance summary of the related references

References #	Freq. (MHz)	Pin (dBm)/ Vin (mV)	PCE (%)	V_{DC_OUT} (V)	Load (kΩ) (μA)	Number of stages	Technology	Idea, pros and cons	Measurement/ simulation
[14]	13.56	–	70	2.5	1.5 μA	3	150 nm SOI CMOS	Idea: low Vth SOI transistors Pros: decreases both forward and reverse losses Cons: costly technology	S
[18]	950	− 14 dBm	–	1.5	–	6	0.3 μm CMOS	Idea: external Vth cancellation Pros: increases efficiency and thus reading range Cons: weight, volume, and cost of tag	M
[15]	868	− 17 dBm	60	2	….	2	0.13 μm CMOS	Idea: reconfigurable topology for rectifier Pros: avoids Vth increase due to body effect and enhances efficiency Cons: larger PMOS transistor with increased parasitics and degraded matching	M
[16]	866.5 (UHF)	− 25 dBm	–	0.4	1000 kΩ	2	0.18 μm Standard Digital CMOS (plus discrete Schottky diodes)	Idea: external devices Pros: increased sensitivity and reading range Cons: high cost due to external devices	M
[9]	900 (UHF)	− 8 dBm	60	3.9	330 kΩ	36	0.25 μm CMOS (with floating gate transistors)	Idea: adjust Vth after fabrication by charge injection onto float gates Pros: near zero Vth devices Cons: long and costly process	M
[21]	953 (UHF)	− 10 dBm	65	1.8	50 kΩ	3	0.18 μm CMOS (with MIM & Triple-Well)	Idea: active Vth cancellation, automatically decrease/increase Vth in forward/reverse biases Pros: no need to external supply Cons: lower efficiency due to reverse loss	M
[24]	915 (UHF)	− 4 dBm	71.5	2.9	30 kΩ	1	0.25 μm CMOS Silicon-on-Sapphire (SoS)	Idea: intrinsic near zero Vth devices in silicon-on-sapphire tech Pros: near zero Vth devices Cons: costly technology, not suitable for other CMOS digital/analog circuits	M
[17]	13.56 (HF)	− 19 dBm	10	0.5	50 Ω Matched	4	0.35 μm Standard Digital CMOS (plus discrete Schottky diodes)	Idea: Schottky diodes and 2-stage charge pump for more isolation of RF source and load Pros: increased sensitivity and reading range Cons: high cost due to external devices	M
[25]	–	350 mV	60	0.9	4 μA	1	0.13 μm CMOS	Idea: biasing gates of cross coupled transistors Pros: Vth effect is reduced Cons: needs external battery/source for initial charge of capacitors	S

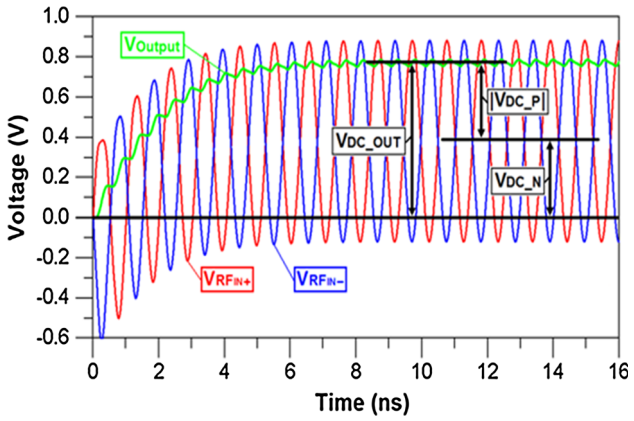


Fig. 10 Simulated waveforms of the nodes for bridge rectifier of Fig. 7

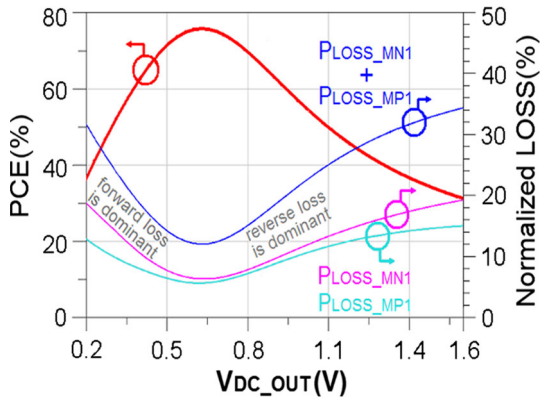


Fig. 11 PCE versus V_{DC_OUT} [21], and normalized loss of transistors

Also, in this output DC voltage, we can use 1.8 V NMOS capacitor, as C_L. Because of using a MOS capacitor, the area and cost of the rectifier becomes significantly lower than the designs with MIM capacitors [21, 24]. We are allowed to use MOS capacitor for C_S, because the DC voltage is high enough, and on the other hand, the capacitor does not need to be linear [26].

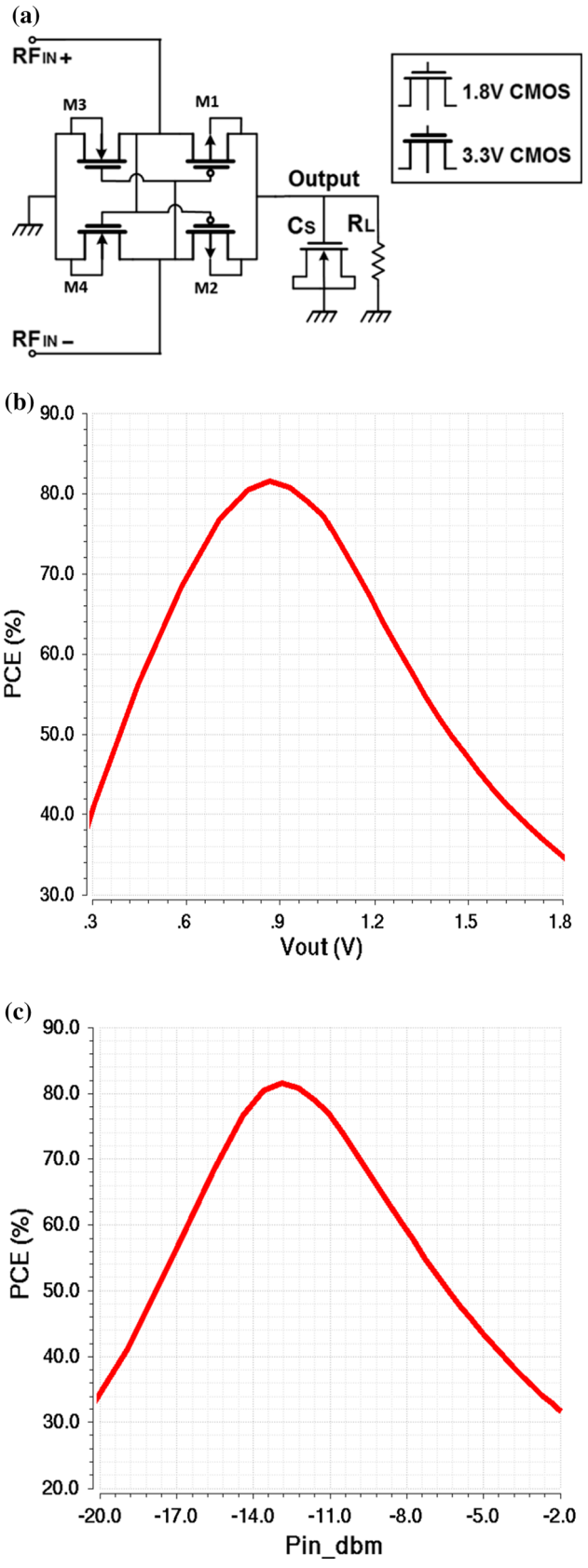
However, a rectifier with higher threshold voltage devices needs higher amplitude of input signal to work properly in the low available powers. This can be done by a proper matching circuit, if the input shunt resistance of the rectifier is high enough [21]. Figure 12(b), (c) show the simulation results of the proposed single-stage rectifier, for the transistor sizes given in Table 2. The procedure of transistor sizing is explained later in this section. As seen in this figure, maximum PCE of 81% is achieved, when V_{DC_OUT} is around 0.9 V. Fortunately, this voltage is sufficient for supplying the digital circuits. It would also be sufficient for the analog circuits, if low voltage design techniques are used in their design [26]. The input impedance measured by simulations at the typical frequency of 953 MHz is 502–j2414 Ω, equivalent to a parallel resistance and capacitance of 12.1 kΩ and 66.3 fF, respectively.

In order to further increase the optimum DC output voltage, multi-stage structures should be utilized, in which similar stages are connected in series [21, 28]. If the multi-stage bridge rectifier is optimally designed, each stage produces a DC voltage which is related to its maximum efficiency. The multi-stage structure, however, suffers from using coupling capacitor, C_C, which is used at the point of connection to the input RF signal. This capacitor reduces the input signal applied to the second stage by a factor of $C_C/(C_C + C_P)$; where C_P is the parasitic capacitance of the second stage input [28]. Therefore, a lower AC part would be available for the dynamic bias, and therefore, results in efficiency drop. On the other hand, NMOS in the second stage would have a bulk-source voltage, due to output DC voltage of the first stage, which results in increase of their V_{th} voltage. As a result, the balanced operation of the bridge is degraded.

Figure 13 is the solution that we propose for such issues. First stage is the same as before, however, in the second stage, 1.8 V NMOS transistors with grounded bodies are used instead of 3.3 V ones, with connected body-source, which require triple well option to be available in the CMOS technology. Such an option is not available in digital CMOS and is only available at extra cost. 1.8 V grounded body NMOS, due to having a V_{SB} of -0.9 V would have a V_{th} of 0.63 V, which is close to V_{th} of 0.65 V for 3.3 V transistors with body-source connections. As the threshold voltages are close to those of the first stage, a relative matching between the two stages are also achieved. This method is more cost efficient than using triple-well option with separate NMOS body connections [21] or other special technologies, such as silicon on sapphire [24].

Since the input DC voltage of the two stages are not equal, their optimum working points occur at different amplitudes of the input signal, which is not an optimal situation. We take advantage of the capacitive division of the input signal, caused by C_C, to compensate the resulted mismatch. This means that C_C in the second stage should be chosen such that the stages operate in their optimum working points, simultaneously, for the same amplitude of the input signal. This is possible, because the optimum amplitude for the second stage is lower than that of the first stage.

Simulations show that the first stage achieves the maximum efficiency at 12.5 dBm or 56 μW input power. Considering input resistance of 12.1 kΩ, this is equal to a 1.15 V RF amplitude, using $P_{IN} = \frac{V_{IN}^2}{2R}$. Now, to find the optimum amplitude, or equivalently, the optimum capacitance value for C_C, a 1.15 V input amplitude is applied through the MOS capacitance C_C to the second stage, and



◀**Fig. 12** **a** The proposed single-stage rectifier with 3.3 V transistors, **b**, **c** simulation results for efficiency versus output voltage and input power for the proposed circuit

the C_C value is swept, until the maximum efficiency point is reached. Simulations show that a collection of 50 parallel MOS capacitors with $\frac{5\ \mu m}{0.5\ \mu m}$ sizes, which in total generate around 1.25 pF capacitance, gives the maximum efficiency. This capacitor is used to couple the input signal to the second stage, with the ratio of $a = \frac{C_C}{C_C+C_P}$. Another capacitor is also placed at the output of the first stage to reduce ripple, which is a collection of 20 parallel MOS capacitors with $\frac{5\ \mu m}{0.5\ \mu m}$ sizes, equivalent to a 450 fF capacitance.

It is known that MOS capacitors are not a suitable choice for coupling capacitors in today's technologies with below 1 V supply voltages, where there is not enough DC bias voltage (i.e., higher than the threshold voltage) available, to keep the transistor in the strong inversion region. However, we implement C_C by MOS capacitors, as enough DC voltage is produced across them, and as a result, the MOS coupling capacitors are kept ON. This choice leads to a low-area and therefore low-cost rectifier design.

Figure 14 shows the simulation results for the second stage, stand alone, and also the complete two stage rectifier. The maximum efficiency of around 80% is achieved at 1.7 V output voltage. It should be added here that both rectifiers are simulated assuming an input waveform amplitude of 1.15 V and R_L of 19 and 40 kΩ, respectively, for the single- and two-stage rectifiers.

In the proposed rectifiers, the transistors are sized according to the following. With increasing W/L ratio of the transistors, both R_{ON} and R_{OFF} of the transistors are reduced, which means the forward loss reduces and reverse loss increases. Therefore, for a given output load, there is an optimum W/L sizing for transistors, for minimizing losses and optimizing the power efficiency. As a rule of thumb, according to [20], the sizing of PMOS transistors are considered five times that of NMOS transistors, for balanced operation of the circuit, as shown in Fig. 11. To reduce input capacitate of the circuit, length of transistors is considered as minimum, which is 0.35 μm for the 3.3 V transistors. In fact, sizing of transistors impose a trade-off between input capacitance of the rectifier circuit and its efficiency. After maximizing efficiency, if the input capacitance is too large, either the sizes can be scaled down, or the ratio of PMOS to NMOS widths can be reduced from 5 to 3. The finalized sizes of transistors in both designs are shown in Table 2.

Table 2 Transistor sizing for the proposed rectifiers

Rectifier	Device	L (μm)	W (μm)
Single stage rectifier	3.3 V NMOS	0.35	3.5×2
	3.3 V PMOS	0.35	3.5×10
	1.8 V MOS Cap (C_S = 1.8 pF)	0.5	5×80
Two-stage rectifier			
First stage	3.3 V NMOS	0.35	3.5×2
	3.3 V PMOS	0.35	3.5×10
	1.8 V MOS Cap (C_S = 1.8 pF)	0.5	5×80
Second stage	1.8 V NMOS	0.18	1.8×4
	3.3 V PMOS	0.35	3.5×12
	1.8 V MOS Cap (C_S = 1.8 pF)	0.5	5×80
	1.8 V MOS Cap (C_C = 1.25 pF)	0.5	5×50

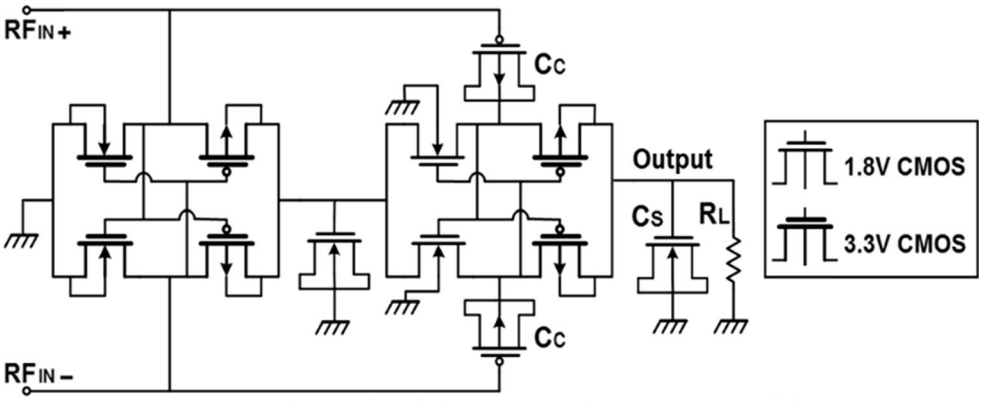


Fig. 13 Schematic of the proposed two-stage rectifier

Table 3 summarizes the performance of the proposed modified rectifiers and provides a comparison with some related previous work.

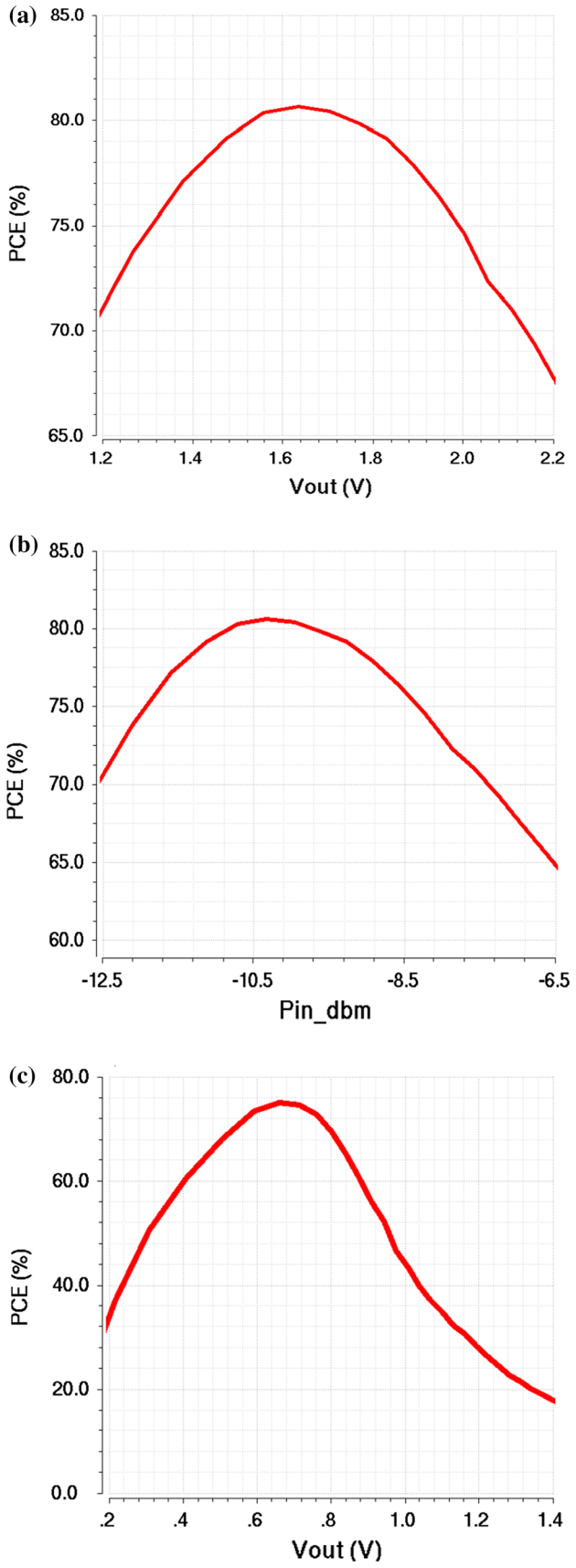
6 Discussions

6.1 Investigating effects of layout parasitics and PVT variations

In order to investigate the effect of layout parasitics, the proposed rectifiers are laid out, as shown in Fig. 15(a), (b). The single-stage rectifier with load capacitor occupies 28.2 μm × 15 μm or 395 μm^2, and the two-stage rectifier including all capacitors occupies 54.1 μm × 94.2 μm or around 5100 μm^2. Post layout simulation is performed to achieve the curves for PCE versus V_{out} and PCE versus P_{in}. In the circuit layout, it is tried to increase the number of transistor fingers to reduce the gate resistance. Also, for high current paths, including the gate of large transistors, the widths are extended for higher current tolerance and lower IR drop. It is also tried to draw the layout as symmetric as possible, to preserve the matching between corresponding paths and elements. Since the layout size is dominated by transistor and MOS capacitor sizes, it is not tried to make the wiring compact, to allow for later layout revisions.

The schematic and post layout simulations are performed in the Cadence environment. The PCE versus V_{out} and PCE versus P_{in} curves in schematics and post-layout simulation results for the single-stage rectifier are shown in Fig. 16(a), (b), respectively, and the same results for the two-stage rectifier are shown in Fig. 16(c), (d). According to Fig. 16, post layout and schematic simulations are close to each other. For both circuits, there is a maximum of 3% difference between the peak efficiencies.

To investigate the effect of process and temperature corners, both circuits are simulated at two corners of {FF, − 40°C} and {SS, 120°C} in addition to the typical case of {TT, 25°C}. The results are shown in Fig. 17(a), (b) for the single stage and two stage rectifiers, which respectively show ± 0.15 and ± 0.2 V variations. In fact, having slow devices means higher threshold voltages, that results in an increase in the output voltage of rectifiers. Also, for the two stage rectifier, each stage has around ± 0.1 V variation, that results in a total of ± 0.2 V variation.



◀**Fig. 14** Efficiency versus **a** output voltage and **b** input power for the proposed two-stage rectifier, **c** efficiency versus output voltage for the second stage, when simulated separately

6.2 Device modeling effects

For analog and RF circuits that are not fabricated and tested in practice, an important issue is the device modeling accuracy and its effect on the circuit performance. In this paper, we have used TSMC 0.18 μm digital CMOS technology with BSIM 3 version 3.2 models and the Spectre simulator in Cadence design environment.

Fortunately, 0.18 μm CMOS technology is a mature technology, in which, the UHF frequency of around 1 GHz is not considered very high. Therefore, it is expected that the transistor models be accurate at this medium frequency. However, in case of any inaccuracy in the models, some important aspects of the rectifier operation could be affected that is investigated in the following.

Variations in the R_{ON} resistance and the threshold voltage of the transistors show their effects at the charging time of the output capacitor, which happens in one half cycle of the input waveform. Variations of the R_{OFF} resistance and the threshold voltage show their effect at the time of output capacitor discharge, that occurs at the other half cycle of the input waveform. Any change in the parasitic capacitance values changes the MOS capacitor storage elements, and therefore, the amount of stored energy changes accordingly. Also, it changes the RC time constants of the charging and discharging paths, and consequently changes the number of input cycles required for the output to be available for the tag circuits. There is also a capacitor voltage division at the input of the second stage, which has a lower chance of being affected, assuming the voltage across the capacitors remain unchanged, since the voltage division depends on the capacitor ratios, and not on their absolute values.

6.3 Effects of target application on circuit specifications

Since the RFID tags are used in many applications, the circuit specifications would accordingly change based on the application and top system requirements. Some of those affected circuit specifications are explained in the following.

First of all, the frequency band of operation changes the antenna dimensions. It also changes the matching circuit that provides matching between antenna and input impedance of the rectifier, at the required band of operation.

On the other hand, the reading range or the maximum distance between the reader and the tag, as the most

Table 3 Performacne summary of the proposed two-stage rectifier and comparison with some previous work

References #	Frequency (MHz)	Pin (dBm)	PCE (%)	V_{DC_OUT} (V)	R_L (KΩ)	Number of stages	Area (mm^2) (W × L) (μm^2)	Type of architecture	Technology	Simulation/ measurement
[1]	868/915 (UHF)	− 19	18	1.5	–	–	–	Conventional voltage multiplier	0.5 µm CMOS (with integrated Schottky diodes)	M
[15]	868 (UHF)	− 17	60	2	–	2–4	0.22 (550 × 400)	Reconfigurable 2-stage Dickson charge pump	0.13 µm Standard Digital CMOS	M
[17]	13.56 (HF)	− 19	–	0.5	–	4	0.213 (670 × 318)	Dickson rectifier + Pelliconi's charge pump	0.35 µm Standard Digital CMOS (plus discrete Schottky diodes)	M
[16]	866.5 (UHF)	− 25	–	0.4	1000	2	0.6	2-stage discrete Dickson rectifier + 5-stage integrated Pelliconi's charge pump	0.18 µm Standard Digital CMOS (plus discrete Schottky diodes)	M
[9]	900 (UHF)	− 8	60	3.9	330	36	0.4 (400 × 1000)	Floating gate transistor	0.25 µm CMOS (with floating gate transistors)	M
[21] (single-stage)	953 (UHF)	− 12.5	67.5	0.63	10	1	–	Cross-coupled bridge rectifier + self-Vth cancellation	0.18 µm CMOS (with MIM & Triple-Well)	M
[21] (three-stage)	953 (UHF)	− 10	65	1.8	50	3	–	Cross-coupled bridge rectifier + self-Vth cancellation	0.18 µm CMOS (with MIM & Triple-Well)	M
[24]	915 (UHF)	− 4	71.5	2.9	30	1	0.002121 (52.5 × 40.4)	Cross-coupled bridge rectifier + added efficiency enhancing transistors	0.25 µm CMOS Silicon-on-Sapphire	M
[28]	900 UHF)	− 14.7	13	1.48	500	9	–	Diode-connected zero-threshold voltage multiplier	0.35 µm CMOS (with MIM)	M
[29]	900 (UHF)	− 14.8	–	0.5	–	1	–	Cross coupled bridge rectifier	0.18 µm Standard Digital CMOS	M
[14]	13.56 (HF)	–	70	2.5	1600	3	–	Ultra-low voltage diode in SOI	0.15 µm SOI CMOS	**S**
[25]	–	350 mV	60	0.9	200	1	–	Bridge rectifier + biasing transistors (reduce Vth effect)	0.13 µm CMOS	**S**
[30]	915 (UHF)	− 10	–	1.13	1000	6	–	Cross coupled bridge rectifier	0.13 µm CMOS	S
[31]	950 (UHF)	− 14	23.44	1.77	–	2	–	Tunable matching circuit + 2-stage voltage multiplier	0.35 µm CMOS	S
[32]	868.3	− 20	–	0.8	Open circuit	2	–	Voltage boosting network + Villard doubler with Schottky diodes	Silicon-on-glass	S
This work (single-stage)	953 (UHF)	− 12.8	78	0.85	19	1	0.000395 (28.2 × 15)	Modified cross-coupled bridge rectifier with 3.3 V transistors	0.18 µm standard digital CMOS	Post-layout simulation
This work (two-stage)	953 (UHF)	− 10.3	78.5	1.68	40	2	0.0051 (54 × 94.2)	Modified cross-coupled bridge rectifier with a combination of 3.3 and 1.8 V transistors	0.18 µm standard digital CMOS	Post-layout simulation

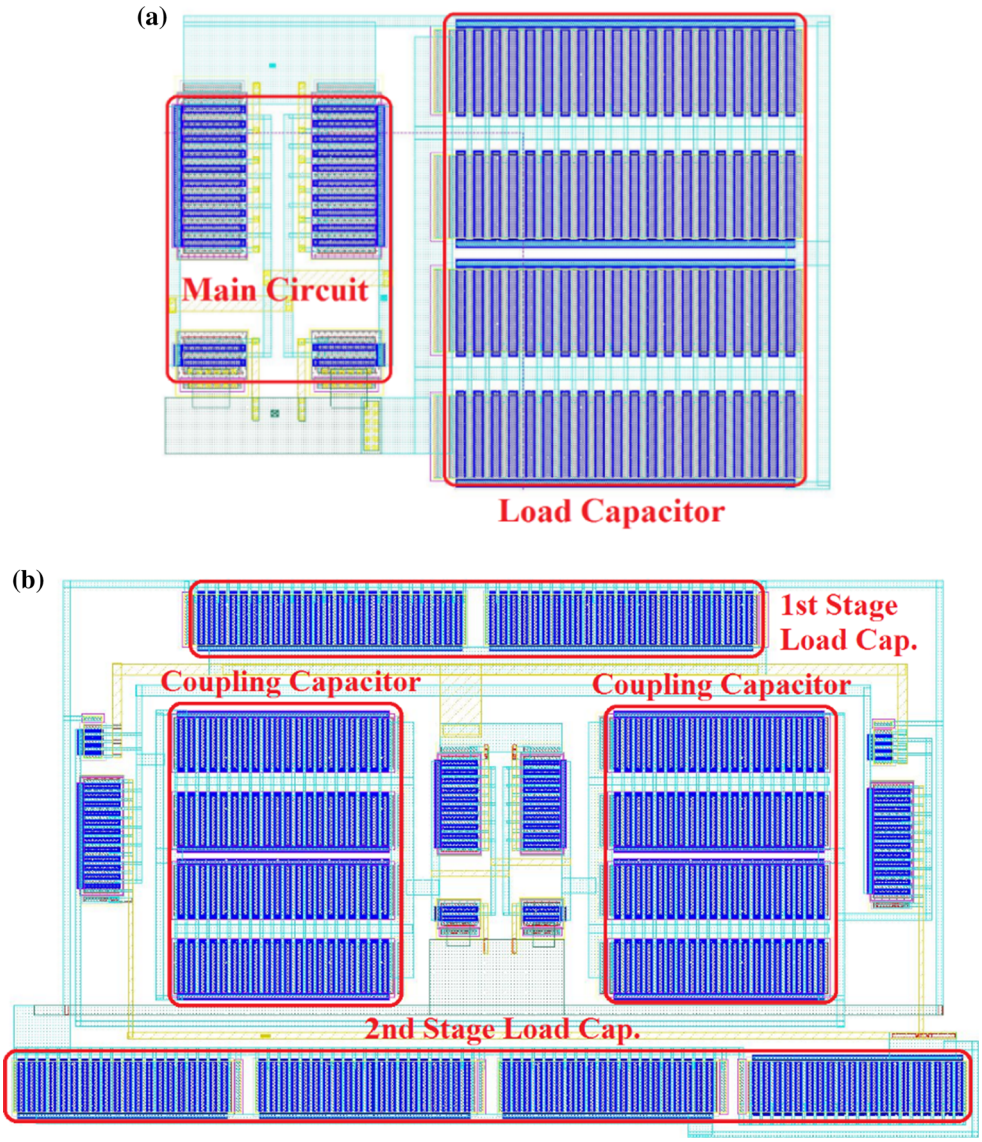


Fig. 15 Pictures of the layout for the proposed circuits, **a** single-stage rectifier with load capacitor, **b** two-stage rectifier with all capacitors

important feature of the tag, is determined by the specific tag application. To increase the read range, lower threshold devices or higher efficiencies are required.

Since the tag is integrated with other analog and digital circuits of the tag, it should be implemented in the same integration technology, that is usually a standard CMOS technology.

The required output voltage also depends on the requirement of the tag internal circuits. If a higher voltage is required, the available solutions include: changing the rectifier topology; changing the number of cascaded rectifier stages; and using a boost power converter.

In addition, the required output power also depends on the requirement of the tag internal circuits. If the intended rectifier cannot provide the required power, the solutions to be considered include: changing the rectifier topology to increase the rectifier efficiency; parallelizing a number of rectennas (a rectenna is a pair of antenna and rectifier) in order to increase the absorbed and harvested energy; using a battery to assist powering the tag circuits; using a rechargeable battery to charge up and store energy at the times the tag circuits require less power (e.g., standby time); and finally using harvesting circuits for other energy sources.

7 Conclusions and future work

Rectifiers are the most important building blocks in the structure of passive RFID tags and IoT, and their design is faced with various challenges, such as threshold voltage of the devices and large signal matching to the antenna, that result in low power efficiencies, and therefore, reduced reading range. In this paper, a comprehensive survey on

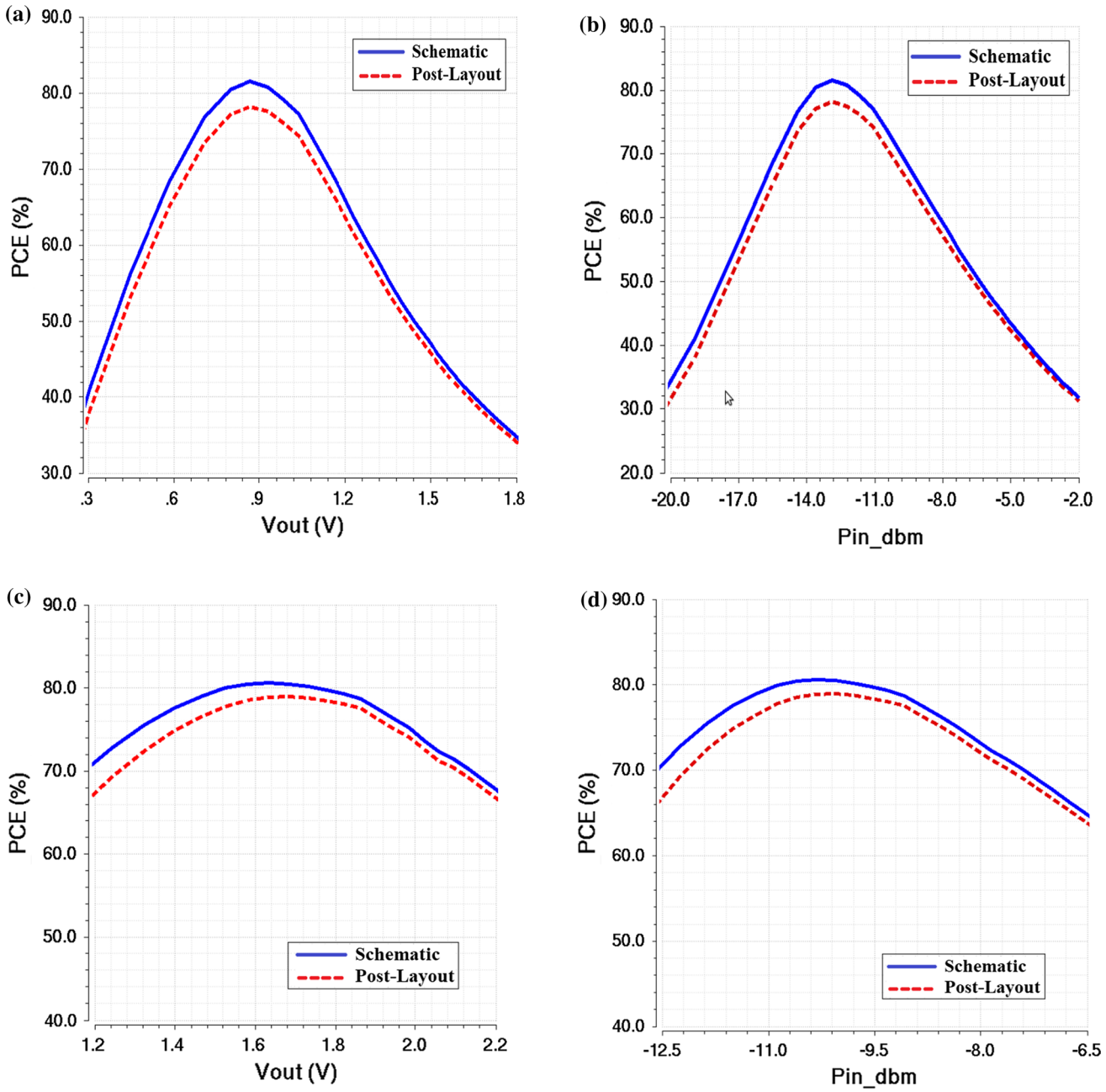


Fig. 16 The PCE curves in schematics and post-layout simulation results for **a**, **b** the single-stage rectifier, and **c**, **d** the two-stage rectifier

high efficiency rectifiers was presented. First, the voltage doubler was introduced. Effect of device threshold voltage on the efficiency was discussed, and based on that, several rectifiers including the ones with external Schottky diodes, which have low threshold voltage, and also rectifiers implemented in other technologies such as SOI, SOS, and OTFT were discussed. Various techniques were surveyed from the literature for reducing the V_{th} effect, including external and internal V_{th} cancellation methods and using floating gate transistors. Standard bridge rectifier as a high efficiency rectifier was then investigated in detail, and through simulations, the forward and reverse losses were examined. It was proposed that changing V_{th} of devices could shift the optimum output DC voltage to a higher voltage, which is suitable for supplying analog and digital circuits of the tag. Two modified bridge rectifiers, a one stage and a two stage, were then proposed using the mentioned threshold adjustment technique. The single stage bridge rectifier was enhanced using 3.3 V transistors and achieved efficiency of around 80% at 0.9 V output. In the two stage rectifier a combination of 1.8 and 3.3 V transistors and MOS capacitors were used, and a low cost

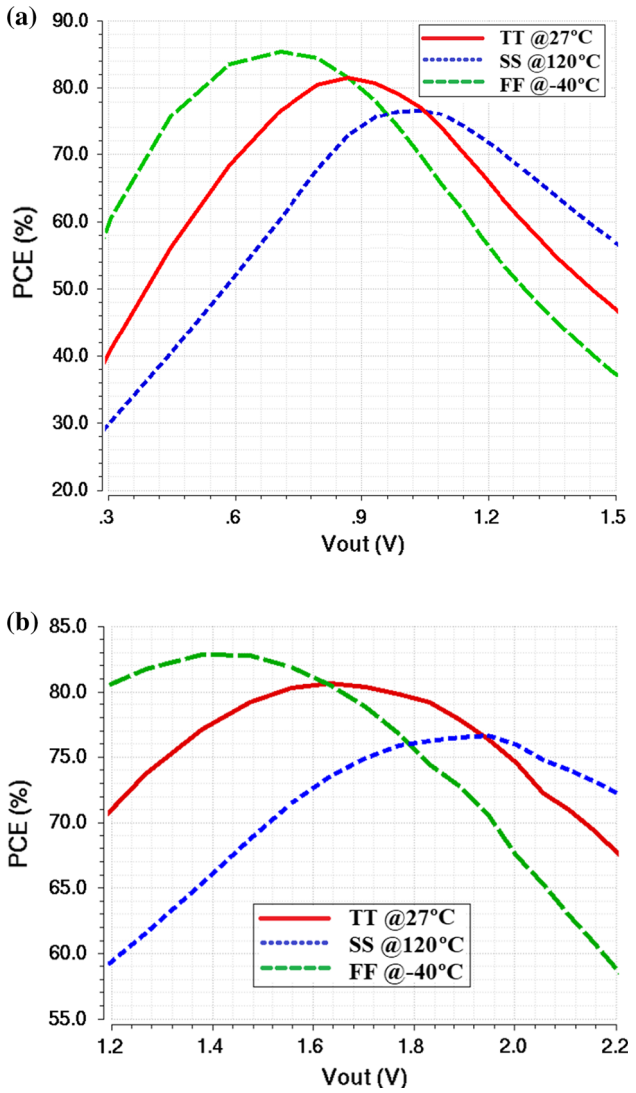


Fig. 17 Effects of process and temperature corners on the PCE versus output voltage curve for the **a** single-stage and **b** two-stage rectifiers

design in digital CMOS technology with no extra technology option was achieved. Simulations predicted a high efficiency of around 80% at 1.7 V output voltage. This paper, not only presents a comprehensive literature survey for the newcomers to the field of power extraction systems, but also, through a step by step design approach, demonstrates a method of efficiency enhancement in the conventional circuit of the bridge rectifier.

As future work, further enhancement to the circuit is suggested as follows. If all analog and digital circuits of the tag is designed with 0.9 V supply, the single-stage rectifier can be used, which is a simple rectifier circuit. Also, the digital and analog circuits of the tag can be designed to operate with two separate supplies. Therefore, in the proposed two stage rectifier, the outputs of the first and second stages can be used, respectively, for the digital and analog circuits of the tag. As a result, the total power consumption is reduced, as the power of digital circuits is reduced according to $P = CV^2f$. Another suggestion for the future work is to design a combined rectifier, to increase the reading range. The circuit includes two rectifiers. The first one is a passive RF energy rectifier, without any external energy source. It harvests some energy and stores it on a capacitor. Such a rectifier may harvest energy from other sources as well. The charged capacitor is later used as an external source of energy for the second rectifier, which is an active one, and therefore, has a high reading range. This technique has been used in some previous publications. The last suggestion is to co-design the rectifier and the antenna. In the proposed rectifiers, the input resistance and input capacitance of the two-stage rectifier is respectively around half and double that of the single-stage, which is reasonable, due to the parallel paths to the input port in the two-stage rectifier. Therefore, the rectifier, the antenna, and the matching circuit in between, could be designed simultaneously, to have the best efficiency performance.

Acknowledgements The authors would like to acknowledge the financial support of the University of Tehran for this research, under Grant Number 8101013/rp/03.

References

1. Karthaus, U., & Fischer, M. (2003). Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power. *IEEE Journal of Solid-State Circuits, 38*(10), 1602–1608.
2. Lu, X., Wang, P., & Niyato, D. (2015). Wireless networks with RF energy harvesting: A contemporary survey. *IEEE Communications Surveys & Tutorials, 17*(2), 757–789.
3. Liu, Z., Zhang, C., Li, Y., Wang, Z., & Wang, Z. (2009). A novel demodulator for low modulation index RF signal in passive UHF RFID tag. In *IEEE international symposium on circuits and systems (ISCAS)* (pp. 2109–2112).
4. Gharaei Jomehei, M., & Sheikhaei, S. (2014). An ultra-low-voltage low power PSK backscatter modulator for passive UHF RFID tags compatible with C1 G2 EPC standard protocol. *Analog Integrated Circuits and Signal Processing, 78,* 489–499.
5. Gharaei Jomehei, M., Sheikhaei, S., & Forouzandeh, B. (2013). A novel ultra-low power ASK demodulator for a passive UHF RFID tag compatible with C1 G2 EPC standard protocol. *Analog Integrated Circuits and Signal Processing, 75,* 21–29.
6. Curty, J.-P., Joehl, N., Dehollain, C., & Declercq, M. J. (2003). Remotely powered addressable UHF RFID integrated system. *IEEE Journal of Solid-State Circuits, 40*(11), 2193–2195.
7. Cantatore, E. (2007). A 13.56 MHz RFID system based on organic transponders. *IEEE Journal of Solid-State Circuits, 42*(1), 84–85.
8. Usami, M. (2003). Powder LSI: An ultra-small RF identification chip for individual recognition applications. *IEEE ISSCC Digest of Technical Papers, 1,* 398–399.
9. Le, T., Mayaram, K., & Fiez, T. (2008). Efficient far-field radio frequency energy harvesting for passively powered sensor networks. *IEEE Journal of Solid-State Circuits, 43*(5), 1287–1302.
10. Xi, Y., Kwon, S., Kim, H., Cho, H., Kim, M., Jung, S., et al. (2009). Optimum ASK modulation scheme for passive RFID tags

under antenna mismatch conditions. *IEEE Transactions on Microwave Theory and Techniques, 57*(10), 2337–2343.
11. Barnett, R. E., Jin, L., & Lazar, S. (2009). A RF to DC voltage conversion model for multi-stage rectifiers in UHF RFID transponders. *IEEE Journal of Solid-State Circuits, 44*(2), 354–370.
12. O'Driscoll, S., Poon, A., & Meng, T. H. (2009). A mm-sized implantable power receiver with adaptive link compensation. In *IEEE international of solid-state circuits conference, digest of technical papers* (pp. 294–295).
13. Curty, J. P., et al. (2005). A model for μ-power rectifier analysis and design. *IEEE Transactions on Circuits and Systems I, 52*(12), 2771–2779.
14. Gosset, G., & Flandre, D. (2009). A very high efficiency ultra-low-power 13.56 MHz voltage rectifier in 150 nm SOI CMOS. In *IEEE international symposium on radio-frequency integration technology* (pp. 347–350).
15. Scorcioni, S., Bertacchini, A., & Larcher, L. (2012). A 868 MHz CMOS RF-DC power converter with − 17 dBm input power sensitivity and efficiency higher than 40% Over 14 dB input power range. In *Proceedings of the ESSCIRC* (pp. 109–112).
16. Pasca, M., Colella, R., Catarinucci, L., Tarricone, L., D'Amico, S., & Baschirotto, A. (2016). UHF front-end feeding RFID-based body sensor networks by exploiting the reader signal. *Radio Science, 51,* 481–489.
17. Colella, R., Pasca, M., Catarinucci, L., Tarricone, L., & D'Amico, S. (2016). High-sensitivity CMOS RF-DC converter in HF RFID band. *IEEE Microwave and Wireless Components Letters, 26*(9), 732–734.
18. Umeda, T., et al. (2006). A 950-MHz rectifier circuit for sensor network tags with 10-m distance. *IEEE Journal of Solid-State Circuits, 41*(1), 35–41.
19. Nakamoto, H., et al. (2007). A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35-μm technology. *IEEE Journal of Solid-State Circuits, 42*(1), 101–110.
20. Kotani, K., & Ito, T. (2009). Self-Vth-cancellation high-efficiency CMOS rectifier circuit for UHF RFIDs. *IEICE Transactions on Electronics, E92-C*(1), 153–160.
21. Kotani, K., Sasaki, A., & Ito, T. (2009). High-efficiency differential-drive CMOS rectifier for UHF RFIDs. *IEEE Journal of Solid-State Circuits, 44*(11), 3011–3018.
22. Razavi Haeri, A. A., Ghaderi Karkani, M., Sharifkhani, M., Kamarei, M., & Fotowat-Ahmady, A. (2017). Analysis and design of power harvesting circuits for ultra-low power applications. *IEEE Transactions on Circuits and Systems I: Regular Papers, 64*(2), 471–479.
23. Facen, A., & Boni, A. (2007). CMOS power retriever for UHF RFID tags. *IET Electronics Letters, 43*(25), 1424–1425.
24. Theilmann, P. T., Presti, C. D., Kelly, D., & Asbeck, P. M. (2010). Near zero turn-on voltage high-efficiency UHF RFID rectifier in silicon-on-sapphire CMOS. In *Radio frequency integrated circuits symposium (RFIC)* (pp. 105–108).
25. Bakhtiar, A. S., Jalili, M. S., & Mirabbasi, S. (2010). A high-efficiency CMOS rectifier for low-power RFID tags. In *IEEE international conference on RFID* (pp. 83–88).
26. Mandal, S., & Sarpeshkar, R. (2007). Low-power CMOS rectifier design for RFID applications. *IEEE Transactions on Circuits and Systems I: Regular Papers, 54*(6), 1177–1188.
27. Rabet, S. B. (2012, September). *Performance enhancement of RFID power extraction systems using circuit techniques*. M.Sc. Thesis, University of Tehran, Iran.
28. Yao, Y., Wu, J., Shi, Y., & Dai, F. F. (2009). A fully integrated 900-MHz passive RFID transponder front end with novel zero-threshold RF–DC rectifier. *IEEE Transactions on Industrial Electronics, 56*(7), 2317–2325.
29. Boni, A., & Bigi, M. (2015). 900 MHZ radio-frequency identification rectifier with optimization and reusing of electro-static discharges protections in 180 nm digital CMOS technology. *International Journal of Circuit Theory and Applications, 43,* 1655–1670.
30. Sampe, J., Mohamad, T. N. T., & Berhanuddin, D. D. (2017). Higher sensitivity RF-DC rectifier for ultra-low power semi-active RFID tags. In *Proceedings of the international conference on high performance compilation, computing and communications* (pp. 131–135).
31. Wilas, J., Jirasereeamornkul, K., & Kumhom, P. (2009). Power harvester design for semi-passive UHF RFID tag using a tunable impedance transformation. In *Proceeding ISCIT'09* (pp. 1441–1445).
32. Yan, H., Macias Montero, J. G., Akhnoukh, A., de Vreede, L. C. N., & Burghartz, J. N. (2005, November). An integration scheme for RF power harvesting. *STW annual workshop on semiconductor advances for future electronics and sensors* (pp. 64–66).

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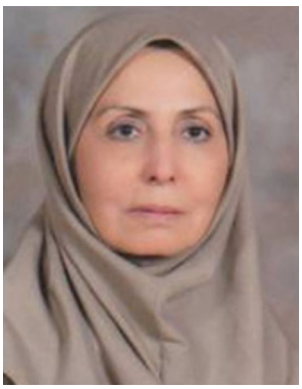

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