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A novel low offset low power CMOS dynamic comparator

Priyesh P. Gandhi[1] · N. M. Devashrayee[1]

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Abstract
This paper presents a novel fully dynamic double tail dynamic comparator that exhibits low offset voltage compared to the traditional dynamic comparators. This paper comprises a novel fully differential double tail high performance comparator suitable for low-voltage low-power applications. A fully differential double tail comparator has been intended to meet the necessity of low offset voltage with optimum power with relatively high speed. In this paper expression for the calculation of the offset voltage and delay of the proposed comparator are derived. These expressions corroborate previously stated results with analytical support as well as providing useful insight for the design of dynamic comparator by analyzing the influence of each transistor pair individually. Transistor mismatch analysis is carried out for offset voltage to fully explore the trade-offs in the design of comparator. The results are validated by Monte Carlo simulations and corner analysis. It is shown that in proposed comparator offset voltage is significantly reduced with optimum power. Authors have proposed novel architecture of dynamic voltage comparator which is differential and double tail and verified the architecture by simulation in 180 nm CMOS technology with $\pm$ 0.9 V supply. The Post-layout simulation results illustrates that a comparator designed with the proposed techniques is 45% faster, and 30% more power efficient and exhibits 91% low offset as compared with conventional comparator, which is the fastest among the conventional comparators.

Keywords Comparator · Fully differential dynamic comparator (FDDC) · Fully differential double tail dynamic comparator (FDDTDC) · Analog to digital converters (ADCs) · Propagation delay · Offset voltage · Power dissipation

1 Introduction

The incredible demand for high performance ADC is forcing towards the employ of dynamic comparator to optimize the speed-power trade-off. In most of all ICs, a significant component called ADC, that bridges the gap between the analog world and the digital systems, is used. The comparator forms the main heart of any ADC architecture used in contemporary technology for conversion from analog to digital and vice versa. The accuracy of such converters has strong relation on design of inter stage gain amplifier and comparator.

The performance of a comparator will determine overall performance of A/D converter because of large number of comparators is used compared to inter stage gain amplifier. The large number of comparator makes it the most critical block of a ADC architecture, not allowing efficient background calibration of all the comparators which directly affects the effective resolution of the ADC due to the comparator input offset voltage.

The overall performance of ADC the speed and the power consumption of the comparator have significant effect; owing to the enormous number of comparisons in ADC [2]. The speed of the ADC is prime concern for high speed digital system and speed of comparator is the key factor [3]. The prerequisite to prolong the battery life of the digital system, speed and accuracy of the ADC is major concern; for comparator it is essential to have low offset, high speed with optimum power. In recent years the emphasis has been given towards the design of high speed comparator with power optimization. The comparator circuits should be immune to speed, power and offset trade off.

✉ Priyesh P. Gandhi
priyeshgandhi@gmail.com

N. M. Devashrayee
nmd@nirmauni.ac.in

[1] EC Department, Institute of Technology, Nirma University, Ahmedabad, India

Several approaches have been proposed in the literature discussed either differential architecture or double tail architecture with offset voltage varies from 10 to 50 mV. In comparators, a lower offset comes at the cost of bigger transistor dimension therefore it will lead to more power dissipation and increased in delay. In addition, the traditional comparators are difficult to design and there are not many design procedures to diminish the offset voltage. To decrease power spending and area of the comparators, dynamic comparators are proposed [3–6]. However, such comparators generally experience comparatively large offset voltage in comparison to static comparators [6, 7]. Some designs have been proposed for dynamic comparators in the literatures. The dynamic comparators are categorized into three groups: Resistor divider [6], Differential pair and Charge Sharing dynamic comparator [6]. Other structures are mainly derived from these architectures [3–8].

The designs proposed in literature, few are anxious with speed [7], few give emphasis to power optimization and enhance resolution [2], some on offset elimination [6]. In this paper authors come out with novel design one with low offset with optimum power and speed.

In order to break the deadlock between offset and power consumption authors have proposed novel architecture which combines the features of differential pair and double tail. The proposed architecture is more robust against any misalignment and non idealities. More importantly, it involves a significantly smaller input offset voltage without sacrificing speed and power penalty.

The paper is organized in 5 sections; Sect. 2 discussed the existing architecture of fully differential dynamic comparator (FDDC). Section 3 presents the novel architecture of fully differential double tail dynamic comparator (FDDTDC). Section 4 discussed the design consideration and simulation results, Sect. 5 conclude the paper.

2 Existing architectures of fully differential dynamic comparator

The existing fully differential dynamic comparator (FDDC) structure is illustrated in Fig. 1 [7]. When Φ_{clk} goes high comparator makes the decision. For the tail clock signal, an identical phase controlled voltage swing clock has been employed rather using same clock which swing from V_{SS} to V_{DD}. To ensure tail current remains in the saturation the limited clock swing is used for tail transistor M_5 and make sure that tail current not enter into linear region.

All transistors M_1–M_4 are of the equal dimension and perfectly balance to ensure all input transistors have same currents the differential pair $V_{in}+$ and $V_{ref}+$ (and $V_{in}-$ and $V_{ref}-$) are grouped in single differential pair [4, 5]. During the time of decision all input transistors will contribute respectively.

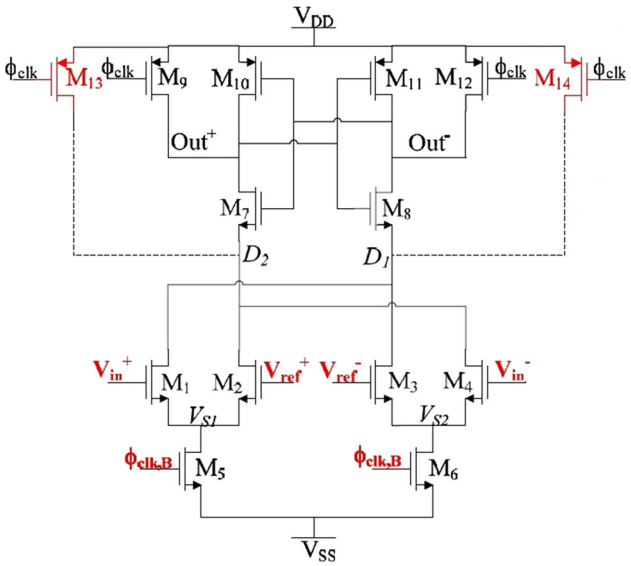


Fig. 1 Fully differential dynamic comparator (FDDC). (Reproduced with the permission from [7])

The inner nodes are reset to V_{DD} when comparator is in ideal mode and help comparator to retune all the nodes prior to the comparator enters into the evaluation mode.

3 Proposed comparator

The fully differential double tail dynamic comparator (FDDTDC) is illustrated in Fig. 2. Some modification has been made to the structure in comparison to the structure shown in Fig. 1. Transistors M_{13} and M_{14} are removed from the structure because transistors M_A and M_B will serve the same purpose to reset the internal nodes D_1 and D_2. On the removal of two clock driven transistors M_{13} and M_{14} the power dissipation of the comparator has drastically reduced in comparison to FDDC. The FDDTDC can work at lower supply voltages in comparison to the FDDC due less stacking.

3.1 Operation of the proposed comparator

Reset Mode: When Φ_{Clk} is low, transistors M_A, M_B, M_9 and M_{12} are on. Out^+ and Out^- are precharge to V_{DD} similarly inner nodes D_1 and D_2 are retune to V_{DD}.

Comparison Mode: When Φ_{Clk} is high, $\Phi_{Clk,B}$ is active, transistors M_A, M_B, M_9 and M_{12} are off. Out^+ and Out^- are discharge to ground through M_1–M_4. If the voltage at V_{in}^+ is higher than the voltage at V_{in}^- ($V_{in}^+ > V_{in}^-$), Out^- is discharged faster than Out^+. The addition of two transistors of

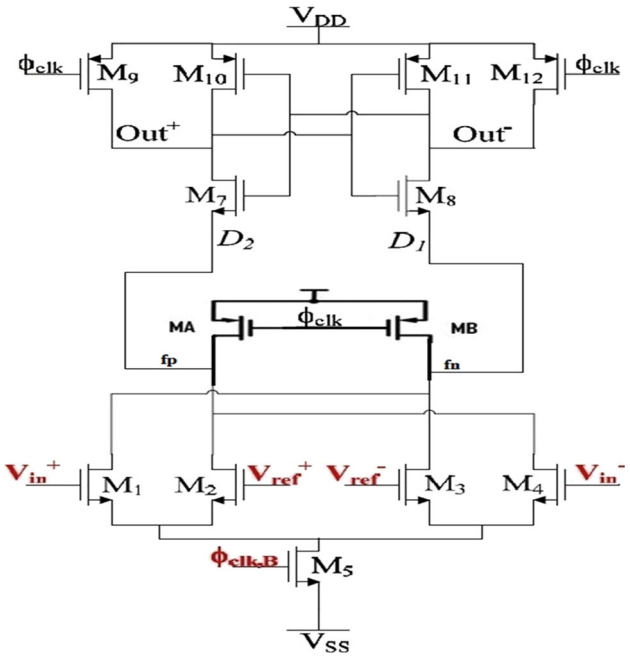


Fig. 2 Proposed fully differential double tail dynamic comparator (FDDTDC)

the M_A and M_B convert the single tail comparator into double tail comparator with differential input and on removal of transistors M_{13} and M_{14} reduced the power dissipation and reduces the offset voltage with moderate increase in propagation delay.

3.2 Performance analysis

The comparator depends on many aspects of the performance parameter. The parameters such as gain, offset, kickback noise, linearity, overdrive recovery, speed and supply voltage are important along with speed and power dissipation, and. In practice, comparator design is a multi-dimensional optimization problem because most of these constraints deal with each other. The performance analysis for offset voltage, delay and power is presented in the following subsection.

3.2.1 Offset

By definition, the offset voltage V_{OS} of the comparator equals to the differential input voltage that establishes the condition $V_{out}^{+} = V_{out}^{-}$.

In the beginning of the decision moment, M_1 to M_4 and M_5 are in the saturation region. This is the main reason of the low sensitivity of this topology to the transistor mismatch as will be demonstrate hereafter. If all the transistors of the two differential pairs have the same dimensions, $\beta_1 = \beta_2 = \beta_3 = \beta_4$, then in the balanced point the two output currents are equal [8, 9].

$$I_O^+ = I_{D7}, I_O^- = I_{D8}, I_{D7} = I_{D8}, I_{D7} = M_2 + M_4, I_{D8} = M_1 + M_3 \quad (1)$$

$$I_{ds1} = \mu_1 C_{ox} \cdot \left(\frac{W_1}{L_1}\right) \cdot \left(V_{in+} + \Delta V_{in} - V_{t1} - \frac{V_{ds1}}{2}\right) \cdot V_{ds1} \quad (2)$$

$$I_{ds2} = \mu_2 C_{ox} \cdot \left(\frac{W_2}{L_2}\right) \cdot \left(V_{ref+} - V_{t2} - \frac{V_{ds1}}{2}\right) \cdot V_{ds1} \quad (3)$$

$$I_{ds3} = \mu_3 C_{ox} \cdot \left(\frac{W_3}{L_3}\right) \cdot \left(V_{ref-} - V_{t3} - \frac{V_{ds3}}{2}\right) \cdot V_{ds3} \quad (4)$$

$$I_{ds4} = \mu_4 C_{ox} \cdot \left(\frac{W_4}{L_4}\right) \cdot \left(V_{in-} - V_{t4} - \frac{V_{ds3}}{2}\right) \cdot V_{ds3} \quad (5)$$

$$I_{ds7} = \mu_7 C_{ox} \cdot \left(\frac{W_7}{L_7}\right) \cdot (V_{out+} - V_{s7} - V_{t7})^2 \quad (6)$$

$$I_{ds8} = \mu_8 C_{ox} \cdot \left(\frac{W_8}{L_8}\right) \cdot (V_{out-} - V_{s8} - V_{t8})^2 \quad (7)$$

The threshold voltage V_{th} and μCox can be explicit in terms of a nominal part and a deviation part owing to mismatch between M_7 and M_8. For ease of calculation collective deviation between μ and C_{ox} can be consider as only deviation in mobility μ [8, 9].

$$\mu_7 = \mu_n + \Delta\mu_7 \quad (8)$$

$$\mu_8 = \mu_n + \Delta\mu_8 \quad (9)$$

$$V_{t7} = V_{tn} + \Delta V_{t7} \quad (10)$$

$$V_{t8} = V_{tn} + \Delta V_{t8} \quad (11)$$

The mismatch between M_2 and M_3 random offset is:

$$\sigma^2_{V_{OS\_M2M3}} = \sigma^2_{V_{t2}} + \sigma^2_{V_{t3}} + \left(V_{ref+} - V_{d5} - V_{tn} - \frac{V_{ds2}}{2}\right)^2 \cdot \sigma^2_{\mu_2/\mu_n} + \left(V_{ref-} - V_{d5} - V_{tn} - \frac{V_{ds3}}{2}\right)^2 \cdot \sigma^2_{\mu_3/\mu_n} \quad (12)$$

The mismatch between M_1 and M_4 results in random offset is

$$\sigma^2_{V_{OS\_M1M4}} = \sigma^2_{V_{t1}} + \sigma^2_{V_{t4}} + \left(V_{in+} - V_{d5} - V_{tn} - \frac{V_{ds1}}{2}\right)^2 \cdot \sigma^2_{\mu_1/\mu_n} + \left(V_{in-} - V_{d5} - V_{tn} - \frac{V_{ds4}}{2}\right)^2 \cdot \sigma^2_{\mu_4/\mu_n} \quad (13)$$

The mismatch between M_7 and M_8 results in random offset is

$$\sigma^2_{V_{OS\_M7M8}} = \left(\frac{W_8}{W_1}\right)^2 \frac{(V_{out-} - V_{s8} - V_{tn})^2}{V^2_{ds1}} \sigma^2_{V_{t8}} + \left(\frac{W_7}{W_1}\right)^2 \frac{(V_{out+} - V_{s7} - V_{tn})^2}{V^2_{ds1}} \sigma^2_{V_{t7}} + \left(\frac{W_8}{W_1}\right)^2 \frac{(V_{out-} - V_{s8} - V_{tn})^4}{4 \cdot V^2_{ds1}} \sigma^2_{\mu_8/\mu_n} + \left(\frac{W_7}{W_1}\right)^2 \frac{(V_{out+} - V_{s7} - V_{tn})^4}{4 \cdot V^2_{ds1}} \sigma^2_{\mu_7/\mu_n} \quad (14)$$

The mismatch between M_{10} and M_{11} results in random offset is

$$\sigma^2_{V_{OS\_M10M11}} = \left(\frac{W_{10}}{W_1}\right)^2 \frac{(V_{DD} - V_{out+} - V_{tn})^2}{4 \cdot V^2_{ds1}} \sigma^2_{V_{t10}} + \left(\frac{W_{11}}{W_1}\right)^2 \frac{(V_{DD} - V_{out-} - V_{tn})^2}{4 \cdot V^2_{ds1}} \sigma^2_{V_{t11}} + \left(\frac{W_{10}}{W_1}\right)^2 \frac{(V_{DD} - V_{out+} - V_{tn})^4}{16 \cdot V^2_{ds1}} \sigma^2_{\mu_{10}/\mu_n} + \left(\frac{W_{11}}{W_1}\right)^2 \frac{(V_{DD} - V_{out-} - V_{tn})^4}{16 \cdot V^2_{ds1}} \sigma^2_{\mu_{11}/\mu_n} \quad (15)$$

In general static random offset voltage σ_{Vos} in the proposed fully differential double tail dynamic comparator is as follows:

$$\sigma^2_{V_{OS}} = \left(\sigma^2_{V_{OS\_M1M4}} + \sigma^2_{V_{OS\_M2M3}} + \sigma^2_{V_{OS\_M7M8}} + \sigma^2_{V_{OS\_M10M11}}\right)^{1/2} \quad (16)$$

The random mismatch in the V_{th} and μ of transistor pair can be modelled as follows [8, 9]:

$$\sigma^2_{V_{th}} = \frac{A^2_{V_{th}}}{WL} + S^2_{V_{T0}} D^2 \quad (17)$$

$$\sigma^2_{\mu} = \frac{A^2_{\mu}}{WL} + S^2_{\mu} D^2 \quad (18)$$

where A_{Vth} is process-dependent parameter, S_{VT0} is the variation of V_{T0}, W, L are the width and length of transistor, D is the distance between the transistor pair in layout. In 180 nm CMOS process, for nMOS is $A_{Vth} \approx 5$ mV µm, $A_{\mu} \approx 1.04\%$. For pMOS $A_{Vth} \approx 5.49$ mV µm, $A_{\mu} \approx 0.99\%$.

For fully differential dynamic comparator static random offset voltage σ_{Vos} is as follows:

$$\sigma^2_{V_{OS}} = \left(\sigma^2_{V_{OS\_M5M6}} + \sigma^2_{V_{OS\_M1M4}} + \sigma^2_{V_{OS\_M2M3}} + \sigma^2_{V_{OS\_M7M8}} + \sigma^2_{V_{OS\_M10M11}}\right)^{1/2} \quad (19)$$

In literature various digital calibration techniques and offset cancellation circuits [10], such supplementary circuits to diminish offset voltages comes with area, power penalty and decline the overall speed. The challenging demand of area and power efficient, high speed applications such as A/D converters pushes to the investigation and usage of dynamic comparator to optimize area, power with enhance the speed. In this paper, new high-speed low offset power efficient comparator structure is introduced.

3.2.2 Delay

The delay is characterized as the time between the start of the amplification phase and the time where 50% of the latch final output is reached. Based on this definition, the inner latch delay can be calculated from derivations presented in [11, 12].

The delay of the comparator consists of two major parts, t_0 and t_{latch} [11]. The charging of the load capacitance C_{Lout} until the first n-channel transistor (M_7/M_8) turns on is represented as delay t_0, subsequently the start of latch regeneration; thus t_0 is derived as

$$t_0 = \frac{V_{Thn} C_{Lout}}{I_{B1}} \approx 2 \frac{V_{Thn} C_{Lout}}{I_{M7}} \quad (20)$$

The drain current of the M_7 is defined as ($I_{B1} \approx (I_{M5}/2)$).

As soon as first nMOS transistor for instance M_7 of the latch turns on, the analogous output (Out_p) will discharged to the ground, will lead pMOS transistor M_{11} to turn on, charging subsequent output (Out_n) to the supply voltage. For initial voltage difference at the output at time t_0, ΔV_0 we have

$$\Delta V_0 = \left|V_{outp}(t = t_0) - V_{outn}(t = t_0)\right| = V_{Thn} - \frac{I_{B2} t_0}{C_{Lout}} = V_{Thn}\left(1 - \frac{I_{B2}}{I_{B1}}\right) \quad (21)$$

Considering $\Delta I_{\text{latch}} = |I_{B1} - I_{B2}| = \Delta V f_n/f_p$, (21) can be rewritten as

$$\Delta V_0 = V_{Thn} \frac{\Delta I_{latch}}{I_{B1}} \approx 2 V_{Thn} \frac{\Delta I_{latch}}{I_{M5}} = \frac{2 V_{Thn}}{I_{M5}} \Delta V_{fn/fp} \quad (22)$$

It can concluded that at time t_0, $\Delta V f_n/f_p$ is the voltage difference at the first stage output is the parameter which affect the initial output difference voltage (ΔV_0) and thus latch regeneration time.

The differential voltage ($\Delta V f_n/f_p$) at time t_0 can be derived as

$$\Delta V_{fn/fp} = \left|V_{fn}(t = t_0) - V_{fp}(t = t_0)\right|$$

$$\Delta V_{fn/fp} = t_0 \cdot \frac{I_{N1} - I_{N2}}{C_{L,fn(p)}}$$

$$\Delta V_{fn/fp} = t_0 \cdot \frac{g_{m1,2,3,4} \Delta V_{in}}{C_{L,fn(p)}} \quad (23)$$

In the above equation discharging current I_{N1} and I_{N2} of input transistors (M_1–M_4), dependent on the differential input voltage (i.e., $\Delta I_N = g_{m1,2,3,4}\ \Delta V_{in}$).

Substituting (23) in (22), ΔV_0 will be

$$\Delta V_0 = 2V_{Thn}\frac{g_{m1,2,3,4}}{I_{M5}}\Delta V_{fn/fp}$$

$$\Delta V_0 = \left(\frac{2V_{Thn}}{I_{M5}}\right)^2 \cdot \frac{C_{Lout}}{C_{L,fn(p)}} \cdot g_{m1,2,3,4}\Delta V_{in} \tag{24}$$

Above equation illustrates that transconductance of input transistors, voltage difference at input (ΔV_{in}), current of latch tail, and the ratio of C_{Lout} to $C_{L,fn(p)}$ have strong influence on ΔV_0. The entire delay of the FDDTDC comparator is derived by substituting ΔV_0 in latch regeneration time.

$$t_{delay} = t_0 + t_{latch} = 2\frac{V_{Thn}C_{Lout}}{I_{M5}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right)$$

$$t_{delay} = 2\frac{V_{Thn}C_{Lout}}{I_{M5}} + \frac{C_{Lout}}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD} \cdot I_{M5}^2 \cdot C_{L,fn(p)}}{8V_{Thn}^2 C_{Lout} g_{m1,2,3,4}\Delta V_{in}}\right) \tag{25}$$

The differential output voltage (ΔV_0) is under enormous influence of the first stage output voltage difference and consequently on latch delay time t_0. The first stage voltage difference should be increased to reduce the delay of the comparator.

The delay of the FDDC is defined as below [11]:

$$t_{delay} = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2,3,4}}}\right) \tag{26}$$

3.2.3 Power analysis

The dynamic power consumption is used to estimate the power is as below [1, 2].

$$P = f_{CLK}C_L V_{DD}^2 + V_{DD} \cdot I_{leakage} \tag{27}$$

$$P_{Dynamic} = \frac{1}{2} \cdot V_{DD}^2 \cdot f \cdot C_L \tag{28}$$

$$P_{static} = V_{DD} \cdot I_{leak} \tag{29}$$

These formulas do not disclose the design parameters which count for power consumption still they are acceptable for the designers with acceptable estimation [13].

In dynamic comparator extensive equation of power is expressed as below [13].

$$P_{avg} = f_{clk}V_{DD}I_{sp5}\left(\frac{1}{8n\emptyset_t^2}\right) \cdot \tau_{latch}|V_{Thp}| \times \left[2k - n|V_{Thp}| + \left(2k + n|V_{Thp}|\right) \cdot exp\left(-2\frac{t_p - t_0}{\tau_{latch}}\right) - 4K \cdot exp\left(-\frac{t_p - t_0}{\tau_{latch}}\right)\right] \tag{30}$$

In the equation, k is equal to the V_{DD}-$|V_{Thp}|$ and t_p and t_0 are

$$t_0 = \frac{C_{Load}|V_{Thp}|}{I_{tail}/2} \tag{31}$$

$$I_{tail} = I_{M5} + I_{M6} for FDDC and I_{tail} = I_{M5} for FDDTDC \tag{32}$$

$$t_p = \frac{C_{Load}}{G_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{\Delta V_{in}}\right) \tag{33}$$

Equation (30) indicates that the dominant design parameters are clock frequency, dimensions of input transistors, V_{DD} and evaluation period (t_p–t_0) which influence the most on the power expenditure of the comparator.

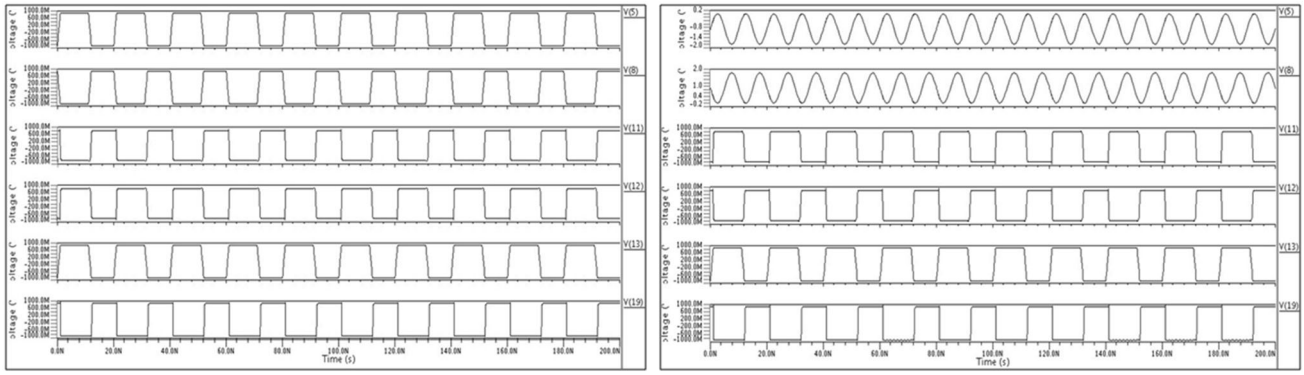
4 Design considerations and simulation results

4.1 Design considerations

a. Differential Design or Double Tail Design: Numerous techniques to realize comparator such as open loop comparator, preamplifier based comparator, dynamic latch comparator and double tail comparator. None of the literature discussed on configuring the feature of differential pair with double tail.
b. Design of Tail Transistor: It confines the current flow through the both of the output branches; it shows greater reliance on speed and offset voltage with different values of V_{CM}.
c. The isolated input and output latch stage: The comparator have a low and more stable offset voltage over a wide range of input common mode voltage and function at a reduced supply voltage.
d. The previous code dependent errors or decision: The internal nodes should be initialized to V_{DD} during the phase when the comparator is not making a decision.

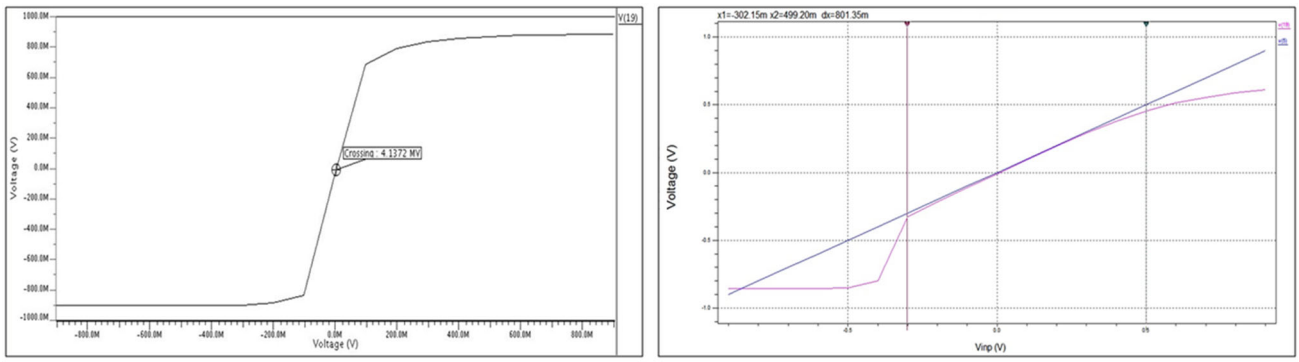
4.2 Simulation results

To verify its operation and the consistency with the analytical derivations including delay, offset ICMR, frequency response and input –output noise spectral density. The circuit operates from a ± 0.9 V power supply. The



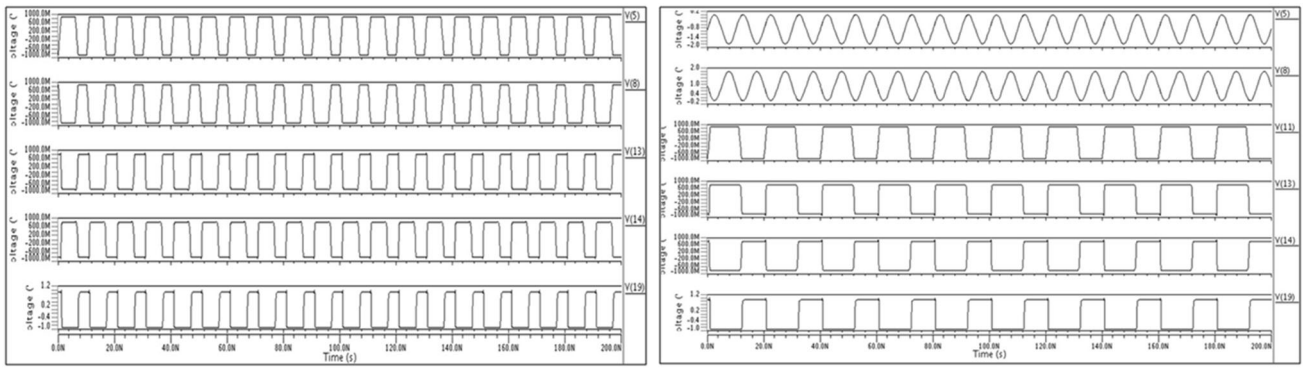
(a) (b)

Fig. 3 Transient response of FDDC. **a** i/p square, **b** i/p sine



(a) (b)

Fig. 4 FDDC. **a** offset voltage, **b** ICMR



(a) (b)

Fig. 5 Transient response of FDDTDC. **a** i/p square, **b** i/p sine

simulation results and layouts are shown in Figs. 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 and 16, the delay of FDDTDC comparator is 0.37 ns, absolute offset voltage of 0.36 mV, ICMR is − 0.40 to 0.56 V with power consumption of 216.37 mW which is quite low in comparison FDDC and other reported structures. The FDDTDC can successfully resolve difference of 1 mV (10 bit resolution) at 1.3 GS/S. Considering that there is no extra circuitry require for offset cancellation, the new-flanged design is appropriate for applications demanding high resolution, high speed with optimum power. The transistor sizing is illustrated in Table 1.

Figure 7 illustrates the input–output noise spectral density for FDDC and FDDTDC. It is evident from the simulations that FDDTDC is more immune to noise in comparison to FDDC. Figure 8 depicts the frequency response of FDDC and FDDTDC.

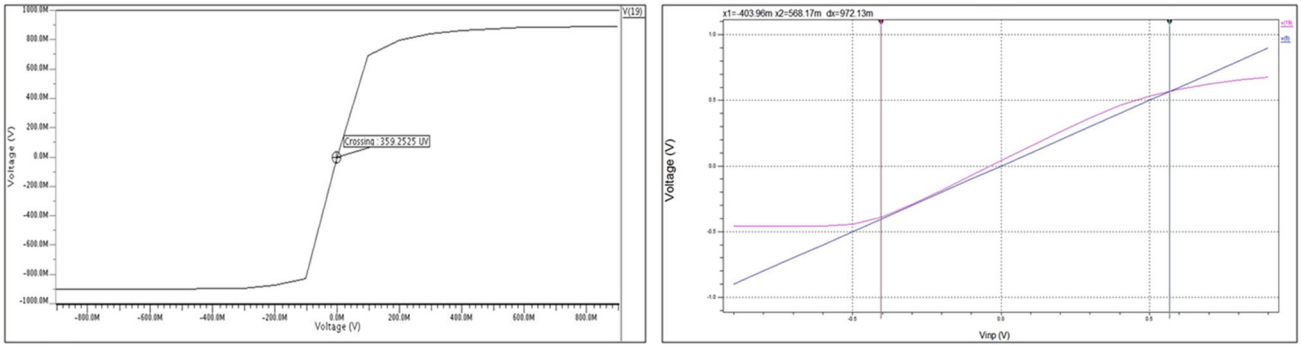


Fig. 6 FDDTDC. **a** Offset voltage, **b** ICMR

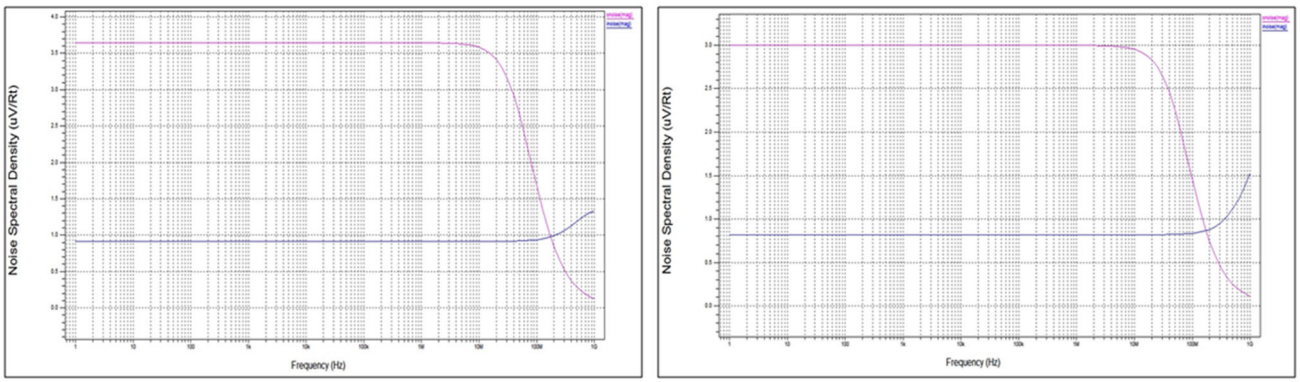


Fig. 7 Input–Output Noise Spectral Density of **a** FDDC, **b** FDDTDC

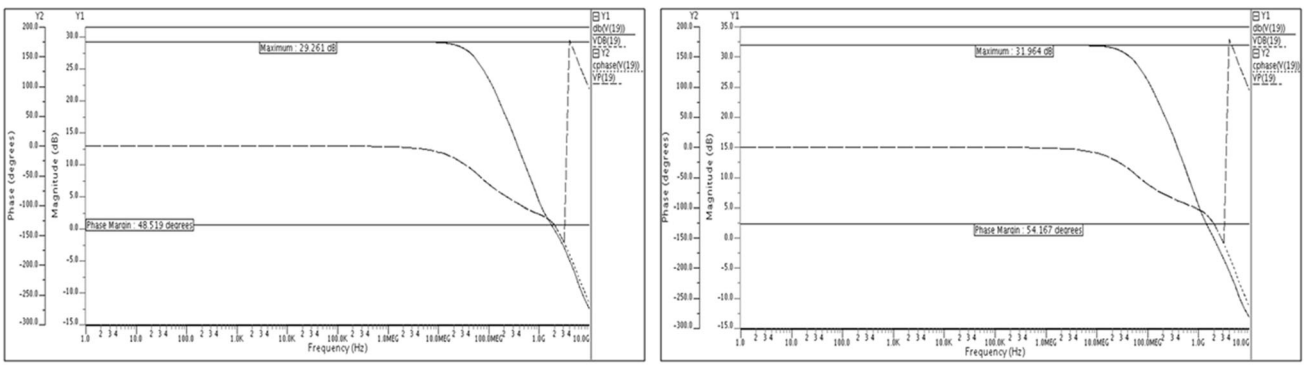


Fig. 8 Frequency response of **a** FDDC, **b** FDDTDC

Figure 9 illustrates the sensitivity of the offset voltage to common input mode voltage (V_{CM}) and power expenditure as a function of V_{CM}. As V_{CM} incases power dissipation is decreasing in both the comparator in identical manner. The Proposed fully differential double tail dynamic comparator has low offset voltage as compared to FDDC mentioned in the Fig. 3.

Figure 10(a) depicts effect of power supply on delay for differential input voltages. The delay is 370 ps (0.37 ns) at V_{DD} = 0.9 V for ΔV_{in} = 1 mV. As V_{DD} changes from 0.9 to 1.5 V, the delay decreases from 370 to 132 ps. Furthermore, lower the delay for the higher value of the differential input voltage for a given V_{DD}. In addition, For a

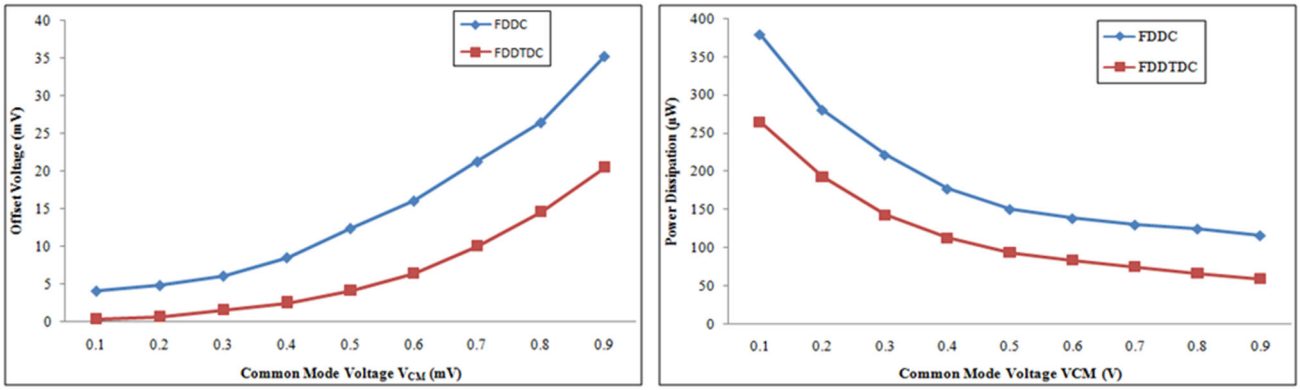


Fig. 9 **a** Common mode voltage v/s offset voltage, **b** common mode voltage v/s power dissipation

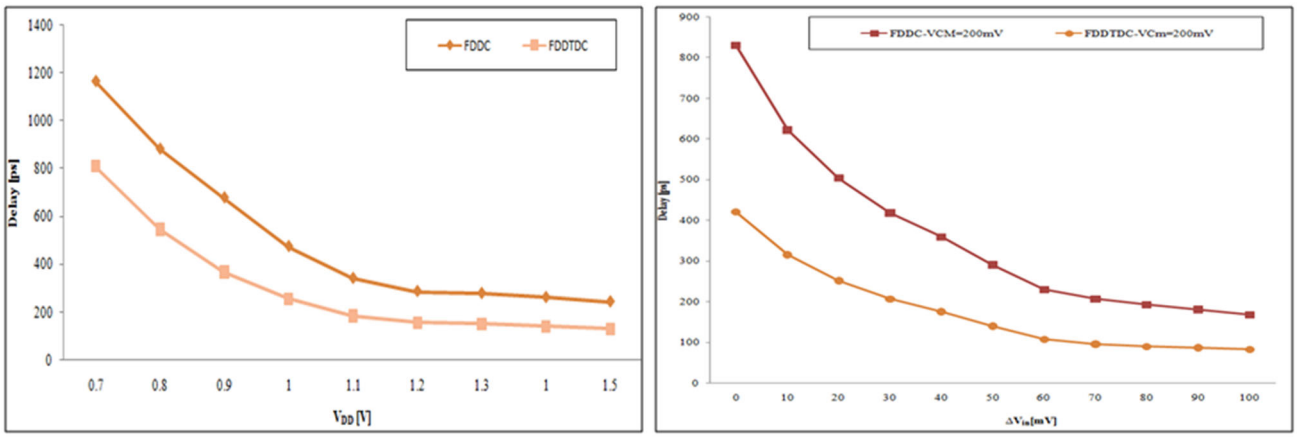


Fig. 10 **a** Delay v/s V_{DD}, **b** delay v/s ΔV_{in}

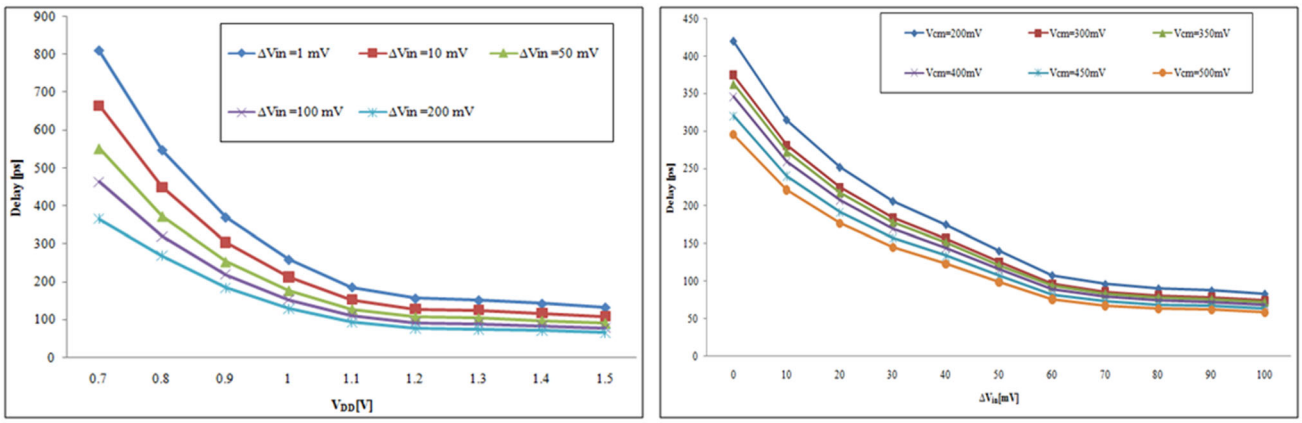


Fig. 11 FDDTDC. **a** Delay v/s V_{DD}, **b** delay v/s ΔV_{in}

given V_{DD}, the higher the differential input voltage, the lesser the delay of comparator.

Figure 10(b) illustrates the effect of different input common-mode voltage V_{CM}, on delay of the comparator for differential input voltage. The delay of the comparator is 370 ps (0.37 ns) for ΔV_{in} = 1 mV@V_{cm} = 200 mV. The delay reduces as differential input voltage enlarges for a given value of V_{CM}.

Figure 11(a) shows the performance of the FDDTDC for delay versus variation in supply voltage for different input

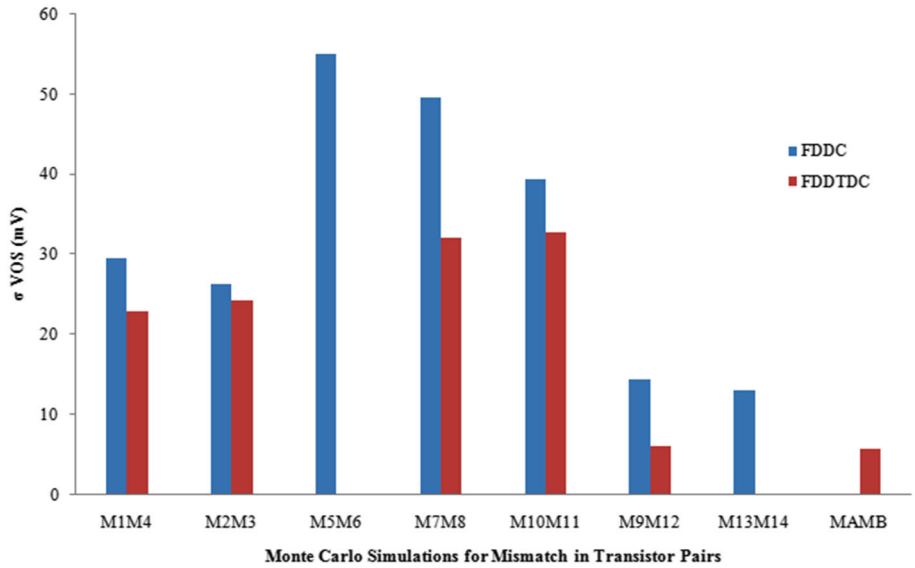
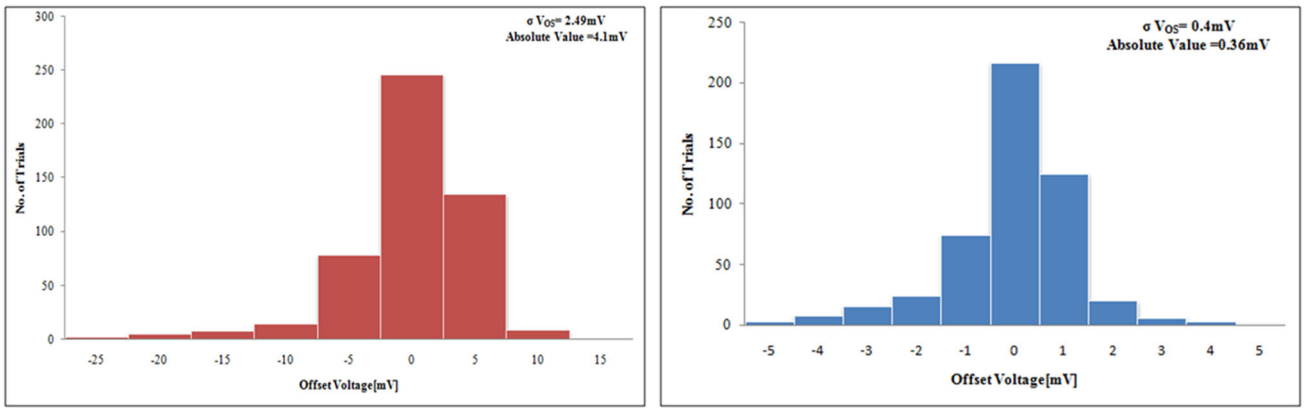
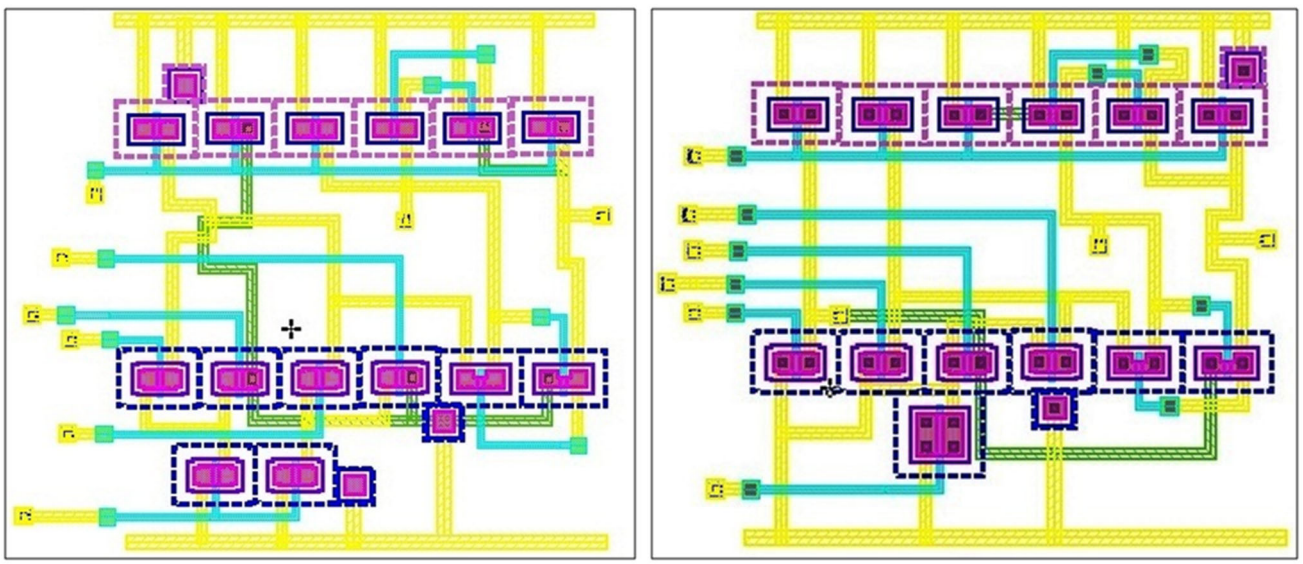


Fig. 12 Monte Carlo simulation for each transistor pair input random offset voltage



(a) **(b)**

Fig. 13 Histogram of Monte Carlo simulation for the offset voltage. **a** DDC, **b** FDDTDC



(a) **(b)**

Fig. 14 Layout. **a** FDDC, **b** FDDTDC

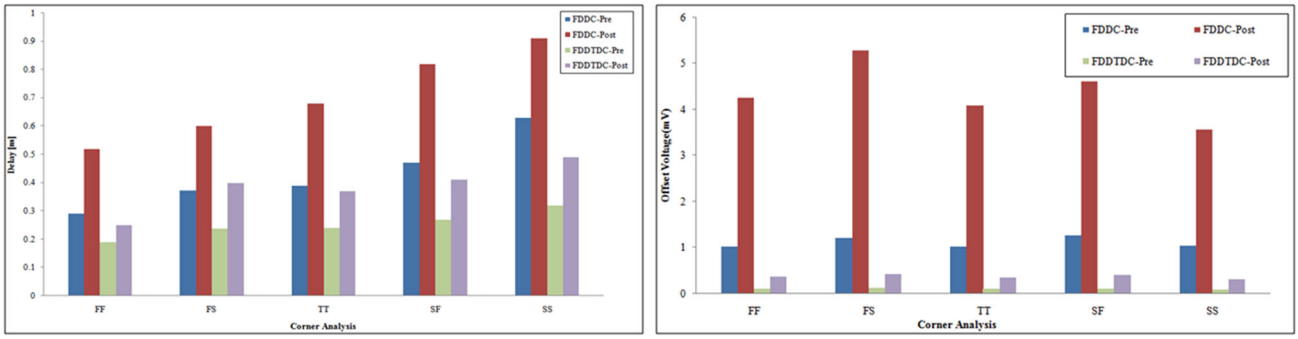


Fig. 15 Corner analysis. **a** Delay, **b** offset voltage

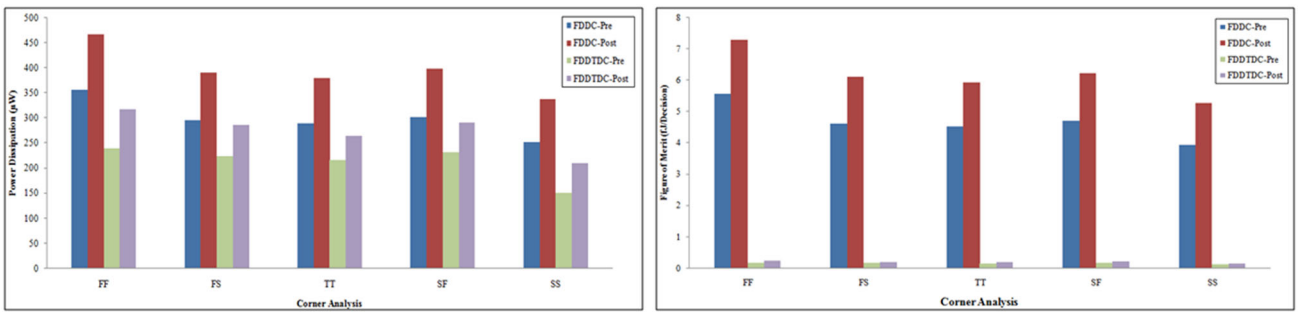


Fig. 16 Corner analysis. **a** Power dissipation, **b** FOM

Table 1 Transistor sizing for FDDC and FDDTDC

MOSFET	Size	
	FDDC	FDDTDC
M_1, M_2, M_3, M_4	6 µm/0.4 µm	6 µm/0.4 µm
M_5,M_6	6 µm/0.4 µm	10 µm/0.4 µm (only M5)
M_7, M_8	0.75 µm/0.35 µm	0.75 µm/0.35 µm
M_9, M_{10}, M_{11}, M_{12}	0.70 µm/0.35 µm	0.70 µm/0.35 µm
M_{13},M_{14}	1.5 µm/0.4 µm	–
M_A, M_B	–	1.0 µm/0.18 µm

voltages. Figure 11(b) shows the effect of delay of the FDDTDC against differential input voltage under different values of V_{CM}.

Figure 12, demonstrates the random offset voltage with the Monte Carlo Simulation for 1σ due to mismatch in different transistor pair of FDDC and FDDTDC as described conditions in Eqs. (16) and (19). From the simulation results and the Eq. (16) and (19) it affirms that FDDTDC has lower offset voltage than the FDDC. The transistor pair which causes the major offset and more venerable to mismatch is M_5–M_6.The $\sigma^2_{V_{OS\_M5M6}}$ which represents the maximum mismatch for transistor pair M_5 and M_6, is not present according to Eq. (16) for the FDDTDC result into lower offset voltage.

Figure 13 shows Histogram of Monte Carlo Simulation for the Offset Voltage for DDC and FDDTDC. The Monte Carlo simulations for 500 iterations have been carried out for FDDC and FDDTDC. The FDDTDC have very offset voltage and improved ICMR. In case of *FDDTDC* the absolute value (average offset voltage) of the input offset voltage is 0.36 mV at one sigma, with the standard deviation from the simulation is 0.4 mV.

Figure 14 shows the layout of DDC and FDDTDC. All the transistors are positioned symmetrically to diminish mismatch and parasitics. Figures 15 and 16 shows the corner analysis (FF, FS, TT, SF, SS) for Delay, Offset Voltage, Power Dissipation and Figure of Merit for FDDC and FDDTDC.

Table 2 evaluates the performance of the FDDTDC with the FDDC. The FDDTDC provides low offset with high dynamic range and better sensitivity at low input for optimum power with considerable reduction in delay.

Table 2 Performance comparison

Parameter	FDDC	FDDTDC
Technology (nm)	180	
Supply voltage (V)	± 0.9	
No. of transistors	14	13
Delay (ns)	0.680	0.37
Sampling frequency	250 MS/s	1.3 GS/s
Offset (mV)	4.1	0.36
ICMR (V)	− 0.30 to 0.49	− 0.40 to 0.56
Input–output noise spectral density ($\mu V/\sqrt{Hz}$)	0.91 and 3.64	0.81 and 3.00
Gain (dB)	29.261	31.964
Phase margin	48.519	54.167
Sensitivity (mV)	4	1
Bit resolution	8	10
Power dissipation (μW)	379.82	265.25
PDP (fJ)	15.69	8.59
FOM (fJ/decision)	5.93	0.20
Area (μm × μm)	16.5 × 17.6	15.03 × 17.09

Table 3 Performance summary and comparison

Parameter	[10]	[11]	[12]	[14–16]	[17]	[18]	[19]	[20]	This work
Technology (nm)	130	180	90	90	180	180	180	180	180
Supply voltage (V)	1.2	1.2	1.0	1	1.8	–	–	1.8	± 0.9
Delay (ns)	Calibration Time 400 ns	0.29	0.15	0.17	1.699	–	–	–	0.37
Sampling frequency (GS/s)	–	0.5	1	3.0	0.1	0.8	0.625	0.1	1.3
Offset (mV)	100/0.22	7.8	33	16.3	–	0.15	0.35	–	0.36
Bit resolution	–	–	–	–	–	–	–	–	10
Power dissipation (μW)	3500 + 580 (= 4080)	329	51	162	460	780	1200	900	265.25
PDP (fJ)	–	–	–	–	–	–	–	–	8.59
FOM (fJ/decision)	–	658	51	59.20	–	–	–	–	0.20

Table 3 compares the FDDTDC with other reported comparator architectures. The FDDTDC has the very low offset and lowest FOM energy dissipated per conversation for optimum power with low offset voltage.

5 Conclusion

A novel design structure of Differential Double Tail Dynamic Comparator for high performance ADC is proposed with comprehensive offset and delay analysis. A new structure of the circuit are used to improve head room as well as the accuracy with which comparator can make decision. Simulation is carried out in 180 nm CMOS technology and result affirms that design metrics, delay, offset power and FoM are improved to a immensely. The simulation results illustrates that a comparator designed with the proposed techniques is 45% faster, and 30% more power efficient than reference comparator FDDC. The FDDTDC exhibits 91% low offset without any power hungry offset cancellation circuits as compared with conventional comparator. Parametric variations also carried out to verify the performance parameter of the proposed comparator and demonstrate stable performance over the process variations and for different transistor corners. The FDDTDC makes a superior trade-offs among speed, resolution, power, offset and area for applications which requires high speed, high resolutions such as ADCs, wearable electronics, and recently captured attention of IoT.

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Priyesh P. Gandhi was born in Diu, India in 1983. He received the B.E. in Electronics and Communication from the Hemchandracharya North Gujarat University, India in 2004 and M. Tech in VLSI Design from the Nirma University, Ahmedabad in 2010, where he is currently pursuing the Ph.D. Degree, from the Electronics and Communication Department, with research on High Performance CMOS Voltage Comparator. His Current research interest includes low power low voltage analog and mixed signal integrated circuit.

N. M. Devashrayee received the M.S. from the M. S. University, Baroda, India in 1977 and Ph.D. in Kurukshetra University, India, 1990. Since 2003 he has been with Nirma University, Ahmedabad, where he is currently a Professor in Electronics and Communication Department. He was with the Rensselaer Polytechnic Institute, Troy, New York as a Post Doctoral Scientific Researcher involved in research on Chemical Vapor Deposition (CVD) of copper for multilevel metallization for the development of ULSI. His current research interest include low voltage low power analog integrated circuit design.