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A novel algorithm to study the impact of the mismatch on analog building blocks: a case study in basic 35 nm CMOS amplifiers

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Abstract
In this paper, the context of modeling of the impact of mismatch and statistical variations on analogue circuit building blocks is emphasized. The aim is to develop a new algorithm which predicts the statistical behavior of important parameters of an amplifier including output resistance, voltage gain and trans-conductance. The relative error of standard deviation of statistical parameters will remain less than 5% compared with the most accurate Monte-Carlo (MC) simulations using atomistic library model-cards. In comparison with other models which are based on the normal distribution of parameters, the proposed model does not need this limiting presumption. On the other hand, the proposed algorithm is more efficient compared with time consuming MC atomistic simulations.

Keywords Statistical variability · Analogue amplifiers · Mismatch models · Atomistic simulations · Monte-Carlo simulations

1 Introduction

According to transistor size reduction which in turn leads to deca-nanometer regime, process variability due to the I.C. fabrication steps and statistical random variations due to intrinsic parameter fluctuations increase circuit vulnerability and causes precision and reliability issues in circuits [1–3]. Without having an exact model of these effects, designed circuits would not be guaranteed to follow their predicted performance. To make confidence about final performance of the circuit, the impact of these variations on circuit parameters should be considered in early design stage. This needs an accurate modeling of variation effects in order to achieve an accurate variability aware design [3–5].

Fabrication-induced variations have been identified as one of the most significant impediments for the IC design. The magnitude of these variations highly depends on the relevant IC technology process [4–6]. For instance with shrinking the transistor dimensions to 45 nm technology node and below, process variations make a significant rule in performance variability and eventually in diminishment of yield [7]. A significant amount of research has been carried out to characterize and model the device variability and to estimate its impact on circuit behavior and to develop new topologies and design techniques that can reduce the impact [8–11]. For a new technology appropriate modeling of these variations is necessary to predict the performance of the system. By shrinking the device dimensions, the magnitude of random variations increases [6]. Moreover it is possible to observe new variation sources. Thus, variation modeling, for both present and next generation technology is necessary.

Different number of modeling approaches presented by researchers, among them the Pelgrom's model is one of the most basic models. In this model standard deviation (SD) of electrical parameters has an inverse square proportional with the active area of the device [8–12]. Scaling down the dimensions and advancements in technology causes new effects. Thus, this model is not reliable any more. Therefore, more accurate and complicated modeling is required to estimate these variations with an acceptable precision particularly in SRAM [13], ADC/DAC [14, 15], and amplifier circuits [16]. Authors in [17] presented an

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approach for statistical simulation and circuit performance-driven optimization of semiconductor technologies. Moreover, in [18], authors presented a reliability simulation framework that has been integrated with variability analysis. Authors in [19] have investigated the impact of statistical variability on the accuracy of a propagation delay time compact model. In model presented in [20], the impact of transistor mismatch on the design tradeoffs at the circuit level and some techniques that can break the mismatch imposed limits in certain applications in analog circuits are investigated. In model [21], comprehensive mismatch characterization data and analysis in deep-sub-micrometer have been investigated. Threshold voltage mismatch in nano-meter regimes has been investigated and modeled in [22].

Mismatch effects can be divided into two components: systematic and random. Systematic component arises from fabrication induced variations and it can be reduced by applying various techniques in layout design. The other one is random component whose the main variation sources are Random Discrete Dopants (RDD) [23], Line Edge Roughness (LER) [24], and Poly Gate Granularity (PGG) [25] which are all considered as intrinsic parameter fluctuations [1, 2, 26–28]. A list of electrical and physical parameters of the device is presented in Table 1. Mismatch effects has a significant impact on electrical parameters and cause variations in operating point, bandwidth, gain and other circuit's main characteristics [4]. Authors in [29] presented a study on drain current mismatch by considering the threshold voltage and subthreshold swing fluctuations.

The paper is organized as follows: in Sect. 2 analytical models of mismatch in short channel regime are reviewed. In the Sect. 3 the proposed algorithm is presented which is based on the introduction of appropriate variations in the channel length, width and input voltage of the gate in single stage amplifiers. In Sect. 4, the verification of the algorithm is carried out using single stage amplifiers. It means that the statistical behavior of the small signal parameters for common source, common drain and common gate amplifiers are modeled using the proposed method and their accuracies are evaluated. Finally, Conclusion is presented in Sect. 5.

Table 1 Process and electrical parameters as presented in [4]

Process parameter	Electrical parameter
Flatband voltage (V_{fb})	Drive current (I_{on})
Mobility (μ)	Leakage current (I_{off})
Substrate dopant conc. (N_{sub})	Trans-conductance (g_m)
Length offset (ΔL)	Input voltage (V_{gs})
Width offset (ΔW)	
Gate oxide thickness (t_{ox})	
Source/drain sheet resistance (P_{sh})	

2 Mismatch models

For modeling mismatch effects, the main variation sources should be identified. Dominant variations are physical parameter's random variation of device. After identification of sources, they were historically formulated and calculated based on their SD variations. Their impact on electrical parameters of the circuits has been always in attention [28]. Pelgrom's model is an analytical relation which models local and global variation. Variance of a parameter's difference (ΔP) between two transistors with the same bias is given by [11]:

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D \tag{1}$$

where A_P and S_P are technology-dependent parameters, W and L are channel dimensions, and D is the distance between two transistors. The current factor (β) and threshold voltage (V_{th}) commonly are used as mismatch modeling parameters [2, 11]. This model can be used for long channel transistors by prediction of variations down to channel lengths of 2 μm [3]. By scaling down dimensions into deca-nanometer regime and subsequent Short Channel Effects (SCE), the long channel variation models are not true at all and hence, more accuracy is required to model these variations. Two important manifests of SCE are velocity saturation and mobility degradation. Velocity saturation occurs when drain-source voltage is high enough to make a critical field in channel length ($E_C = V_{DS,sat}/L$). Subject to this equation, $V_{DS,sat}$ is drain-source voltage in velocity saturation [30]. In fact drain current in short channel transistors enters saturation regime earlier than long channel ones because carrier's velocity saturates ($v_{sat} = \mu_0 E_C$). The drain current relation in short channel transistor in the saturation regime, when the velocity saturation occurs, is expressed as [31]:

$$\begin{aligned} I_{DS} &= v_{sat} C_{ox} W (V_{GS} - V_{TH}) \\ &= \beta (V_{GS} - V_{TH}) V_{DS,sat} \end{aligned} \tag{2}$$

where C_{OX} is the gate oxide capacitance per unit area, β defined as $\beta \triangleq \mu_0 C_{ox} W/L$ which μ_0 is the low-field mobility of the carriers. Current mismatch (ΔI_{ds}) that is the difference between two identical transistor currents, based on variance of β and V_{TH}, will be given by:

$$\Delta I_{DS} = \frac{\partial I_{DS}}{\partial \beta}\Delta\beta + \frac{\partial I_{DS}}{\partial V_{TH}}\Delta V_{TH} = (V_{GS} - V_{TH})V_{DS,sat} \cdot \Delta\beta - \beta V_{DS,sat} \cdot \Delta V_{TH} \quad (3)$$

where $\Delta\beta$ and ΔV_{TH} are the differences between current factor and threshold voltage of two identical transistors. It can be shown that $\Delta I_{DS} = \beta V_{DS,sat} \cdot \Delta V_{GS}$. Thus an equation for the modeling of the gate voltage mismatch as an offset voltage in the gate can be derived as presented in Eq. (4). This equation can be used to compensate the mismatch between 1000 identical transistors subject to intrinsic parameter fluctuations as presented in Fig. 1 [1].

$$\Delta V_{GS} = \frac{V_{GS} - V_{TH}}{\beta}\Delta\beta - \Delta V_{TH}. \quad (4)$$

The other SCE, mobility degradation, happens when the gate voltage is higher than drain-source voltage. If $V_{GS} - V_{DS} > 0.7$ V, the effect of mobility degradation remarkably affects circuit performance [1]. To take this phenomenon into account in the drain current equation, effective carrier mobility (μ_{eff}) should be used in drain current equations which can be expressed as:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{GS} - V_{TH})} \approx \mu_0[1 - \theta(V_{GS} - V_{TH})] \quad (5)$$

where θ is the mobility degradation coefficient. Substituting Eq. (5) into Eqs. (2) and (4) gives:

$$\begin{aligned} I_{DS} &\approx \beta[1 - \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})V_{DS,sat} \\ \Delta V_{GS} &\approx \frac{[1 - \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})V_{DS,sat}}{V_{DS,sat}[1 - 2\theta(V_{GS} - V_{TH})]}\frac{\Delta\beta}{\beta} - \Delta V_{TH} \\ &\approx [1 + \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})\frac{\Delta\beta}{\beta} - \Delta V_{TH}. \end{aligned} \quad (6)$$

3 Proposed method for mismatch modeling

Current circuit mismatch models use a series input voltage source (V_{GS}) to compensate the mismatch between identical transistors as shown in Fig. 1. However, these DC-compensated mismatch models are not accurate to predict variation of AC parameters of transistors. The aim of this paper is to analyze the mismatch in small signal parameters and model these variations in single stage amplifiers.

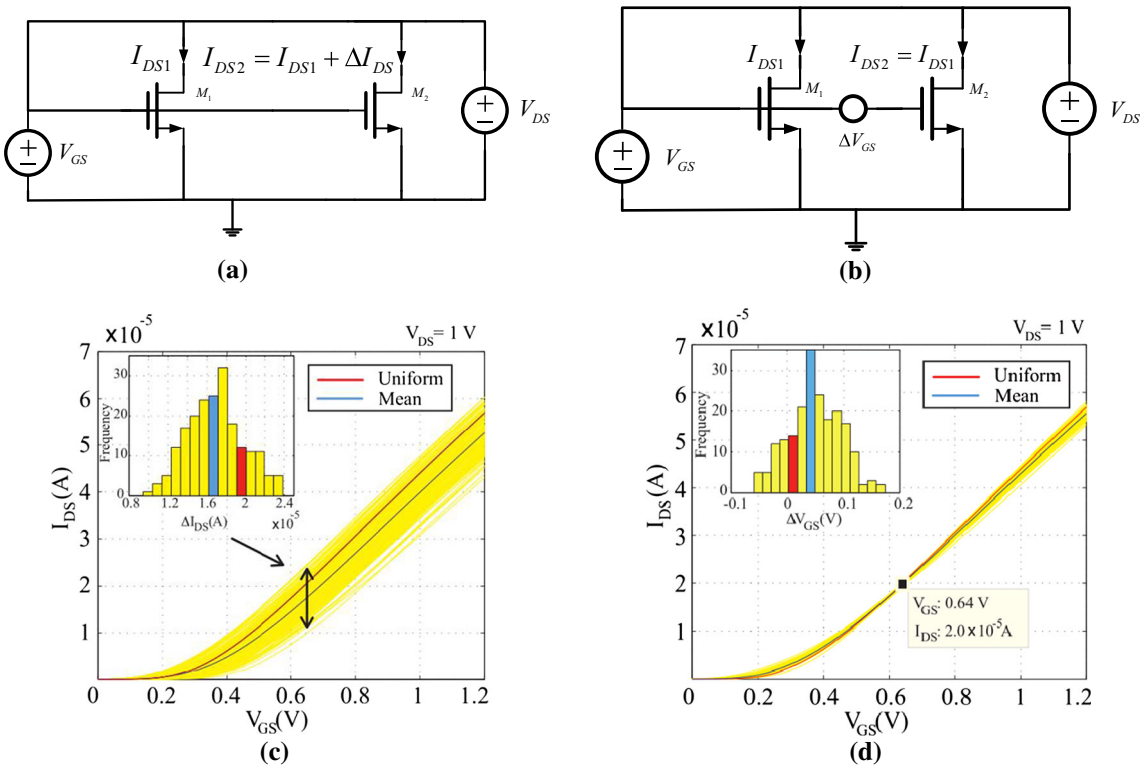

Fig. 1 **a** Drain current mismatch between two identical transistors under same bias conditions, **b** compensation of mismatch with addition of appropriate voltage source in the gate of transistors, **c** I_{DS}–V_{GS} characteristics of 1000 identical transistors subject to mismatch with the inset histogram at a given point, **d** I_{DS}–V_{GS} characteristics of mismatch compensated transistors with the inset histogram at a given point [1]

In the proposed method, modeling is carried out using appropriate channel length variations in the transistor under test. This makes sense in the first order because LER which is one of the important sources of variation as defined in Sect. 1, has a significant impact on the channel length. Hence, we need to use the HSPICE netlist and statistical information of the desired parameters as the input data according to Fig. 2. Statistical information contains standard deviation and mean value (average) of transistor parameters. Using mismatch models, the desired variation sources are calculated based on the first guess for the standard deviation of the channel length and input voltage.

As shown in Fig. 3, a variation source across the channel length (σL) is added to netlist. Then, the Monte Carlo simulations will be carried out in HSPICE and finally statistical information of important parameters will be extracted. We repeat this process by increasing σL, until the SD error of the voltage gain reaches to less than 10% (X is a set point or minimum value for SD error of gain voltage, and assume equal to 10% at the first). At the first step, voltage gain parameter will be analyzed, because the better this parameter get modeled, the less error other parameters will have in modeling. At the next step, we investigate the introduced error in other parameters. Considering target error of 5%, the algorithm decides whether to repeat previous step or enter to second. In the second loop a variation source will be added in series with transistor gate and then the error of important parameters will be extracted. Note that increasing $\sigma(V_{GS})$ affects operating region of the transistor. However, for the validation of our proposed algorithm with real data, as presented in Ref. [6], it can be seen that our obtained results for $\sigma(V_{GS})$ agrees very well with the corresponding value of $\sigma(V_{TH})$, roughly equal to 50 mV. Finally, the error of standard deviation of

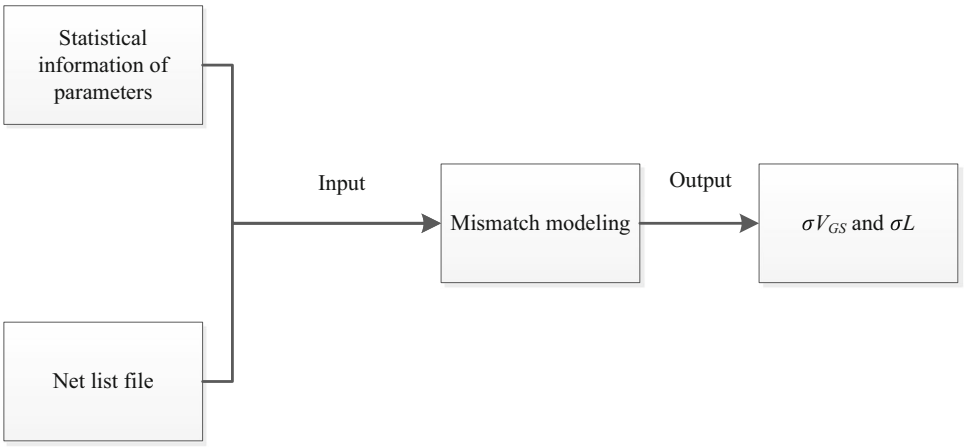

Fig. 2 Mismatch modeling approach

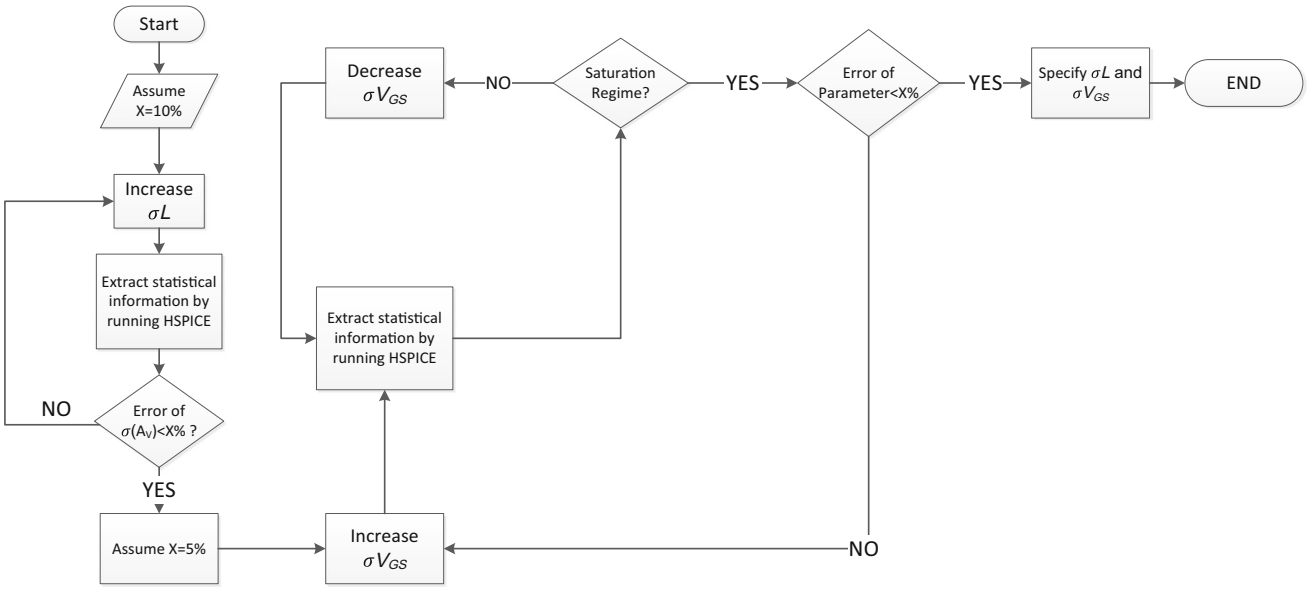

Fig. 3 Proposed algorithm of mismatch modeling

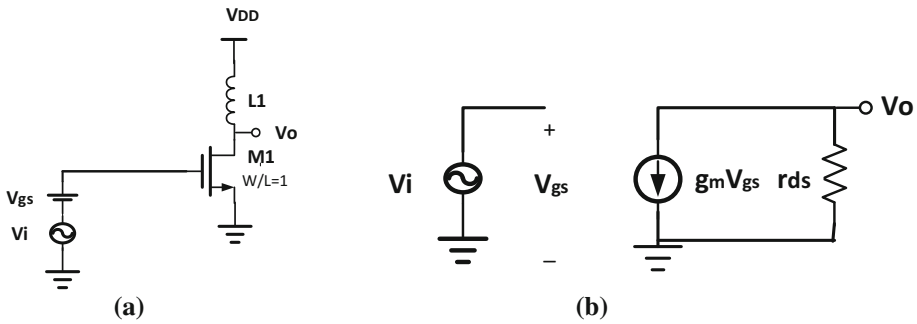

Fig. 4 **a** Common source amplifier circuit under test, **b** its small signal model

parameters will be faded by increasing each variation source. This process repeats two times, the first time will be continued with less than 10% error and the second time with less than 5%. It should be noticed that as technology advanced to decreased channel lengths, it is expected that the variation sources ($\sigma(V_{GS})$, σL) will be increased [6]. However, to evaluate the introduced error in our proposed algorithm in respect to accurate MC simulations, we need appropriate library of modelcards for that particular technology.

Table 2 Common source amplifier parameters

Parameters	Value	Dimension
L_1	10	μH
V_{GS}	500	mV
V_{DD}	1.2	V
I_{DS}	8.75	μA
g_m	46.97	$\mu\Omega^{-1}$
r_{ds}	238	kΩ
A_v	13.31	–

4 Evaluating the accuracy of algorithm

4.1 Common source amplifier

For a complete study on the modeling of the statistical variability in a common source amplifier, we use Fig. 4(a). Since devices with larger area cause less mismatch effects, to achieve maximum variations we adopt W = L = 35 nm. Using this topology, the intrinsic gain of the amplifier can be achieved. Small signal model of this configuration is shown in Fig. 4(b) where the gain is given by:

$$A_V = -g_m r_{ds}. \tag{7}$$

The bias point and small signal parameters are presented in Table 2. Now, using 1000 samples of BSIM4 compact model cards in 35 nm technology node for M_1, we simulate the mismatch variation of parameters of the amplifier. The important parameters are extracted and the standard deviations are calculated. Based on the novel algorithm, statistical replication is carried out two times: first with a Gaussian source with 6 nm SD along transistor's length and the second time with a 35 mV SD source in series with the gate-source voltage. Results of the statistical model are finally compared with atomistic model results and are represented in Table 3(a). It can be seen that results have less than 5% error for all important parameters of an amplifier. Moreover, number of computational cycles and time to reach less than 10% error in the first stage and less than 5% error in the second stage of the proposed algorithm is represented in Table 3(b). This is while the required time for the MC simulations using atomistic library modelcards is approximately 20 min. It should be noticed that the computational time measurements are carried out on a CPU of Intel-Core i3-2.40 GHz and memory RAM of 4 GB.

Table 3 (a) Results of the proposed mismatch model for the common source amplifier, (b) number of computational cycles and time to reach less than 10% error in the first stage and less than 5% error in the second stage of the proposed algorithm

	Atomistic simulation		Proposed model		SD error %
	Mean	SD	Mean	SD	
(a)					
g_m ($\mu\Omega^{-1}$)	50.2	7.27	47.7	6.93	4.67
r_{ds} (kΩ)	287	135.8	298	141.1	3.90
A_v	13.73	4.927	14.55	4.914	0.25
	Number of computational cycles				Computational time (s)
(b)					
First stage	4				420
Second stage	3				307
Total	7				727

For more detailed investigation, a resistor in parallel with the inductor used as the amplifier load as depicted in Fig. 5. Voltage gain of the circuit will be:

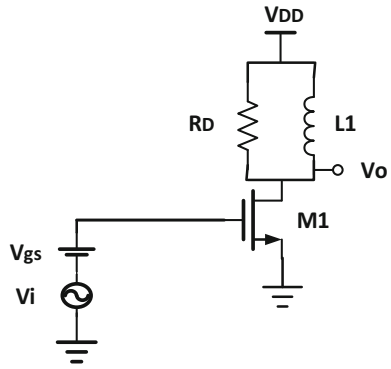

Fig. 5 Common source amplifier with R_D

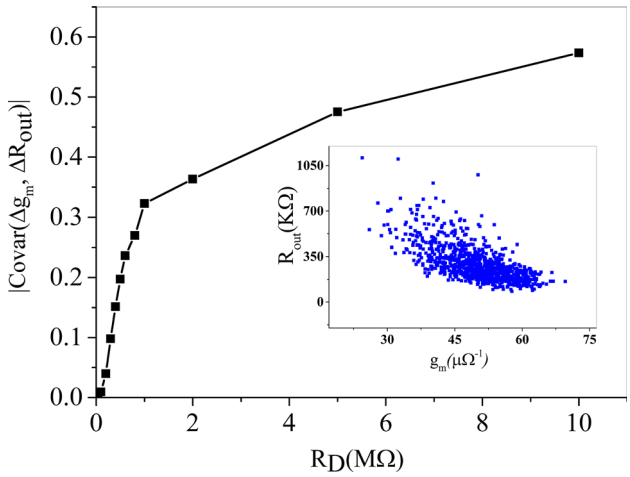

Fig. 6 Correlation between g_m and R_{out} for various R_D, insert is the scatter plots of g_m versus Rout for $R_D = 100$ kΩ

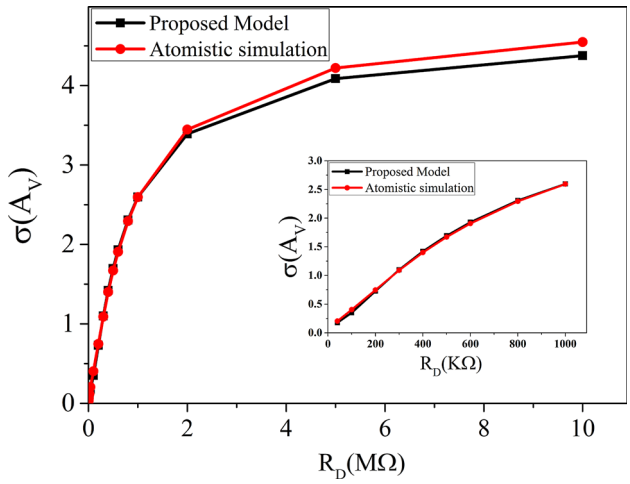

Fig. 7 SD of the voltage gain for various R_D. The inset is the magnified figure for R_D between 100 Ω to 1000 kΩ

$$A_V = -g_m(r_{ds}||R_D) = -g_m R_{out} \tag{8}$$

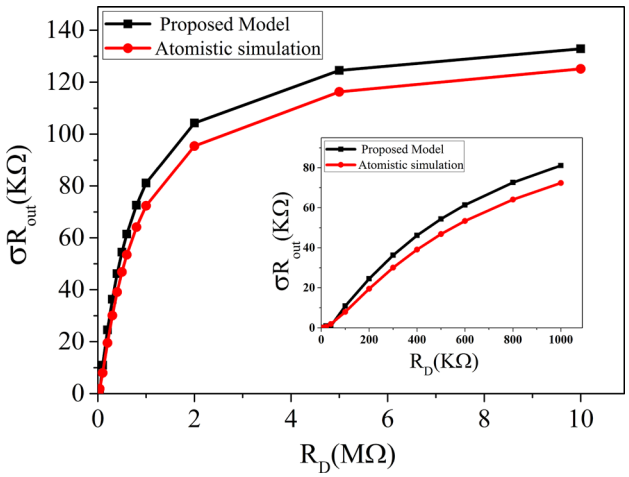

Fig. 8 SD of output resistance for various R_D. The inset is the magnified figure for R_D between 100 Ω to 1000 kΩ

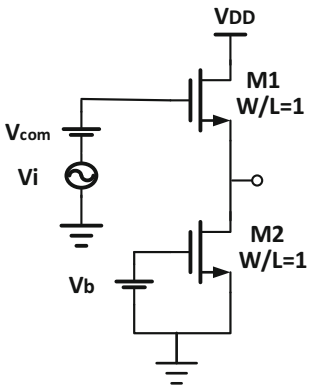

Fig. 9 Common drain amplifier

Table 4 Common drain amplifier parameters

Parameters	Value	Dimension
V_{com}	850	mV
V_{DD}	1.2	V
V_b	400	mV
I_{DS}	2.268	μA
g_m	24.702	$\mu\Omega^{-1}$
R_{out}	31.57	kΩ
A_v	0.77	–

where for $R_D \ll r_{ds}$, $R_{out} \approx R_D$. In this case, it is concluded that g_m and R_{out} are independent and the gain almost varies with g_m variation because changes in R_{out} values are negligible. By increasing R_D, the correlation between g_m and R_{out} will increase as shown in Fig. 6. On the other hand, when R_D is much higher than r_{ds}, the gain

Table 5 (a) Results of the proposed mismatch model for the source follower amplifier. (b) Number of computational cycles and time to reach less than 10% error in the first stage and less than 5% error in the second stage of the proposed algorithm

	Atomistic simulation		Proposed model		SD error %
	Mean	SD	Mean	SD	
(a)					
g_m ($\mu\Omega^{-1}$)	24.5	3.66	24.5	3.48	4.91
R_{out} (kΩ)	32.53	5.042	31.94	4.859	3.64
A_v	0.7785	0.01814	0.7733	0.01853	2.15
		Number of computational cycles			Computational time (s)
(b)					
First stage		4			431
Second stage		4			428
Total		8			859

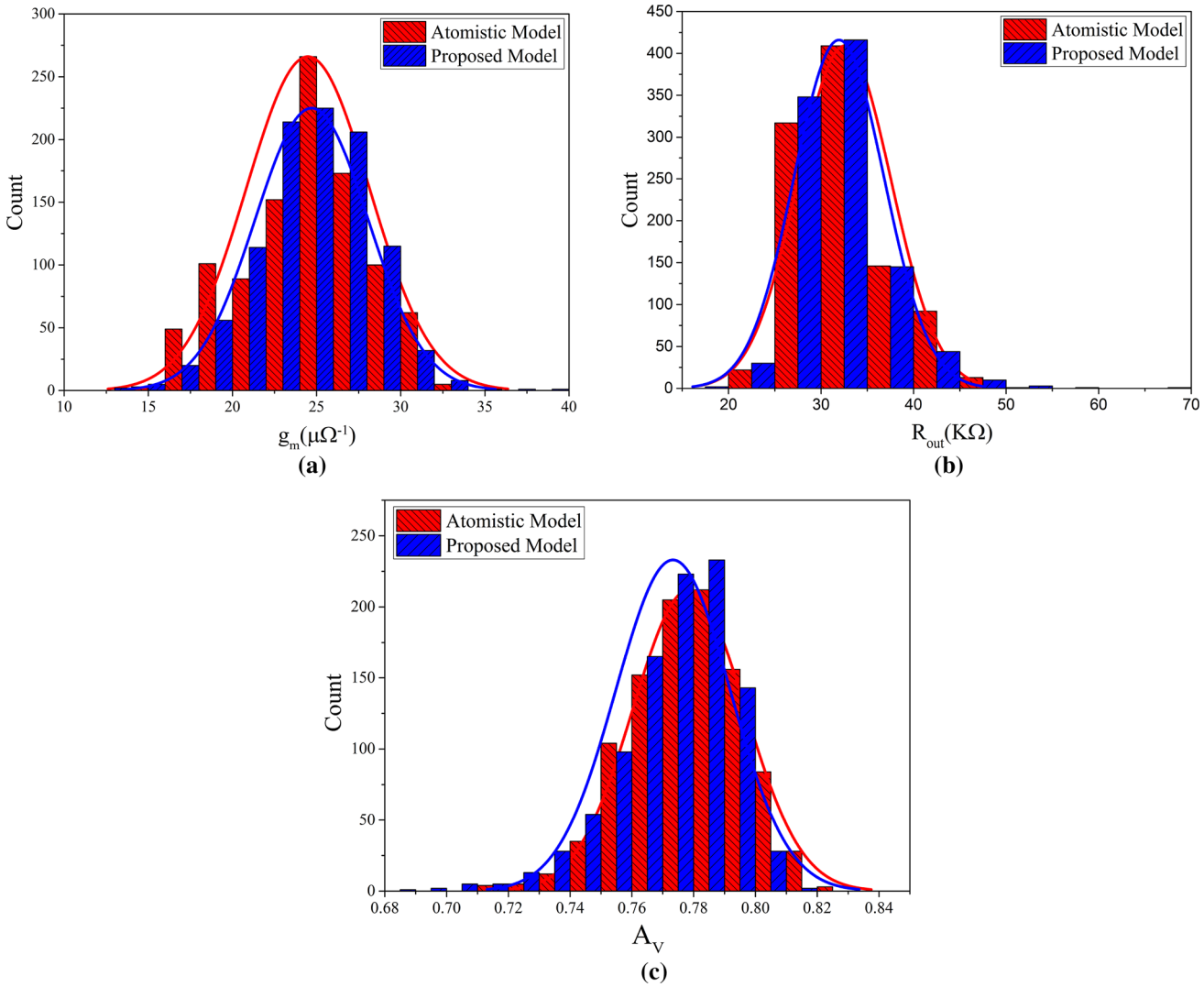

Fig. 10 Histogram of variations for **a** transconductance (g_m), **b** output resistance (R_{out}), and **c** voltage gain (A_v) of common drain amplifier. The red bins represent most accurate results from 'Atomistic' model and blue bins are obtained from the proposed model (Color figure online)

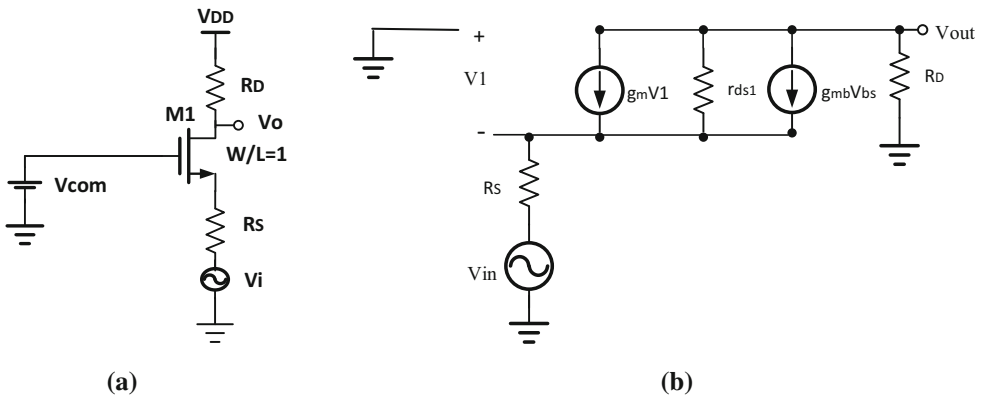

Fig. 11 **a** Common gate amplifier, **b** its small signal model

fluctuations is close to intrinsic mode. Whereas correlation of g_m and R_{out} increases due to increase in R_D, SD of R_{out} and then variation of gain will be increased.

This circuit could be modeled using variation sources came from last circuit in intrinsic mode because both circuits have same bias current. Statistical simulations are carried out using various values of R_D from 100 Ω to 1 MΩ and SD of gain and the output resistance is shown in Figs. 7 and 8. The highest error occurs when R_D is too large which replicates close results with the amplifier in the intrinsic gain mode; however, for the smaller values of R_D, the results obtained from the proposed algorithm are in better agreement with the atomistic simulation results.

4.2 Common drain amplifier

The second type of basic amplifiers studied here is the common drain or source follower amplifier. Unlike common Source amplifier which has a large gain, this configuration has a gain below one and usually is used as a buffer in analogue circuits. A source follower amplifier with an active load is shown in Fig. 9, where the element values and parameters of the amplifier are presented in Table 4.

The mean and SD of the transconductance, output resistance and gain are presented in Table 5(a). The comparison of obtained values with respect to most accurate atomistic simulation results gives less than 5% error in all cases. Moreover, number of computational cycles and time to reach less than 10% error in the first stage and less than 5% error in the second stage of the proposed algorithm is represented in Table 5(b). This is while the required time for the MC simulations using atomistic library modelcards is approximately 20 min. For implementation of the proposed algorithm in this circuit a Gaussian voltage source

Table 6 Common gate amplifier parameters

Parameters	Value	Dimension
V_{com}	400	mV
V_{DD}	1.2	V
R_D	200	kΩ
R_S	1	kΩ
I_{DS}	2.71	μA
g_{m1}	24.8	$\mu\Omega^{-1}$
R_{out}	136	kΩ
A_v	4.23	–

Table 7 (a) Results of the proposed mismatch model for the common gate amplifier. (b) Number of computational cycles and time to reach less than 10% error in the first stage and less than 5% error in the second stage of the proposed algorithm

	Atomistic simulation		Proposed model		SD error %
	Mean	SD	Mean	SD	
(a)					
g_m ($\mu\Omega^{-1}$)	27.6	5.08	26.5	4.84	4.72
R_{out} (kΩ)	130	19.954	132	20.691	3.69
A_v	4.127	0.5336	4.001	0.5154	3.41

	Number of computational cycles	Computational time (s)
(b)		
First stage	5	412
Second stage	4	526
Total	9	938

with 6.1 nm SD in series with the transistor's gate in addition of 82 nA SD current source in parallel with the drain current are used. In comparison to the results achieved from atomistic model, the average error stays less than 1% while the SD error will be less than 5%. Moreover, the histogram graphs of the desired parameters including transconductance (g_m), output resistance (R_{out}), and voltage gain (A_v) are illustrated in Fig. 10.

4.3 Common gate amplifier

The final configuration studied here is the common gate amplifier. Unlike common source and source follower amplifiers where the input signal triggers the gate, in this configuration, the input signal triggers the source and the output is taken from the drain. Meanwhile, this configuration is used in complex amplifiers like chain configuration that improves the bandwidth.

Sample circuit in Fig. 11(a) is used to study the mismatch in this amplifier. Drain current is adjusted with V_{com} in the gate. Based on the small signal circuit shown in Fig. 11(b), the circuit gain will be given by:

$$A_V = \frac{(g_m + g_{mb})r_{ds1} + 1}{r_{ds1} + (g_m + g_{mb})r_{ds1}R_s + R_s + R_D}R_D \tag{9}$$

where g_m is transistor transconductance, g_{mb} is transconductance of transistor bulk and r_{ds1} is drain-source resistance of transistor M_1. The parameter and element values are presented in Table 6.

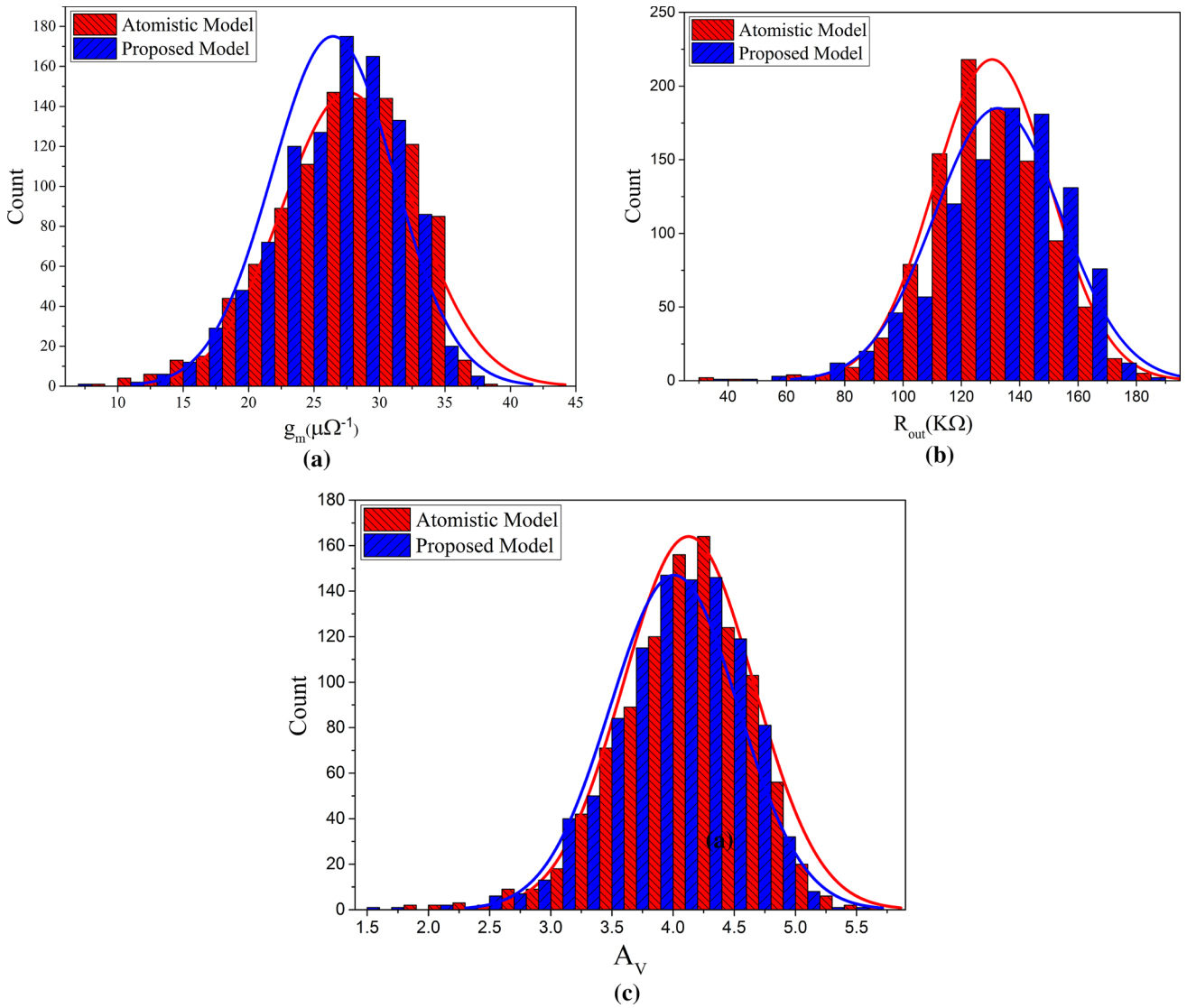

Fig. 12 Histogram graph of variations of **a** transconductance (g_m), **b** output resistance (R_{out}), and **c** voltage gain (A_v) of common gate amplifier. The red bins represent most accurate results from 'Atomistic' model and blue bins are obtained from the proposed model (Color figure online)

Modeling is carried out with a 5.82 nm SD Gaussian source along transistor length and a 45.5 mV SD Gaussian source in series with the gate. The results are compared with the most accurate atomistic model and it can be concluded again that the error values are less than 5%, as presented in Table 7(a). Moreover, number of computational cycles and time to reach less than 10% error in the first stage and less than 5% error in the second stage of the proposed algorithm is represented in Table 7(b). This is while the required time for the MC simulations using atomistic library modelcards is approximately 20 min. Note that the voltage gain has a very low error and it is basically one of parameters that are usually close to desired value in atomistic model. This is due to the fact that this parameter is used as a target parameter in the proposed algorithm. Figure 12 shows the histogram graphs related to the variation of transconductance (g_m), output resistance (R_{out}), and voltage gain (A_v) of the common gate amplifier.

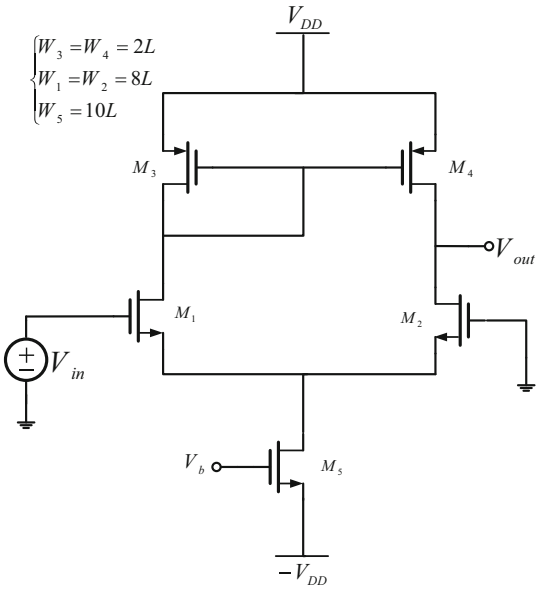

Fig. 13 Schematic of a 5-transistor Op-Amp with active load

Table 8 (a) Results of the proposed mismatch model for the Op-Amp. (b) Number of computational cycles and time to reach less than 10% error in the first stage and less than 5% error in the second stage of the proposed algorithm

	Atomistic simulation		Proposed model		SD error %
	Mean	SD	Mean	SD	
(a)					
g_m ($\mu\Omega^{-1}$)	129	9.2	134	8.95	2.7
R_{out} (kΩ)	74.7	12.8	71.78	13.2	3.1
A_v	8.10	1.63	8.08	1.64	0.1
	Number of computational cycles			Computational time (s)	
(b)					
First stage	4			481	
Second stage	4			492	
Total	8			973	

5 Case study

In order to evaluate the performance of mismatch algorithm, case studies are common practice as presented in [32, 33]. However, since our proposed algorithm is suitable for replicating AC parameter variations of analogue amplifiers, we perform two case studies in more complicated cases. First, we investigate a 5-transistor Op-Amp with active load and second, we study the phenomenon when the number of matched transistors increases.

Figure 13 illustrates the schematic of a 5-transistor CMOS OP-Amp with active load. Modeling is carried out with a 3.8 nm SD Gaussian source along transistor length and a 48 mV SD Gaussian source in series with the gate. The results are compared with the most accurate atomistic model and it can be concluded again that the error values are less than 4%, as presented in Table 8(a). Moreover, number of computational cycles and time to reach less than 10% error in the first stage and less than 5% error in the second stage of the proposed algorithm is represented in Table 8(b).

Figure 14 depicts the schematic of a common source amplifier consisting of a higher width nMOS transistor. To evaluate its performance in respect to mismatch, we convert the wider transistor to a number of parallel basic width transistors as shown in this figure. Then, we investigate the error introduced in the mean and SD of this amplifier using our proposed algorithm in respect to MC atomistic simulations. It can be seen that by increasing the number of

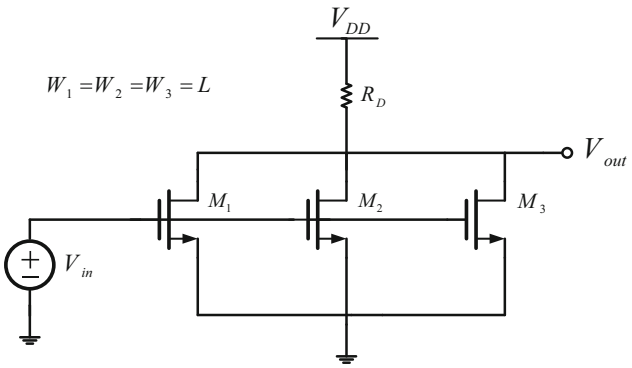

Fig. 14 Schematic of a common source amplifier employing wider width nMOS transistor equal to parallel combination of basic width transistors

Table 9 Results of the proposed mismatch model for the circuit shown in Fig. 14

Number of parallel transistors	Atomistic		Proposed model		SD error %
	Gain mean	Gain SD	Gain mean	Gain SD	
1	1.177	0.148	1.12	0.144	2.7
2	1.98	0.146	1.89	0.150	2.7
3	2.49	0.145	2.41	0.144	1

matched transistors, the gain variability (SD/mean) is decreased as the fluctuations of parallel transistors compensate each other. Moreover, the introduced error in the SD of gain remains less than 3% as presented in Table 9.

6 Conclusion

Previous researches in the field of mismatch models have been focused on the modeling of DC parameters of the device with the aid of approaches such as addition of an offset voltage in series with the gate of the MOSFET transistors. Although these approaches could be used in a specific technology and results in modeling of electrical parameters with high precision, but for the purpose of replicating variations in AC parameters, there cause large errors particularly in deca-nanometer and ultra-short channel regime. Using accurate statistical BSIM4 modelcards, we have been able to extract distributions for the AC parameters such as transconductance (g_m), output resistance (R_{out}), and the voltage gain (A_v) of a single stage amplifier. The results demonstrated that the accuracy of the algorithm is high and the introduced error stays less than 5% compared with the most accurate Monte Carlo atomistic simulations. Two circuits have been investigated as case studies to confirm the applicability of our proposed algorithm in more complicated circuits including an OP-amp and an amplifier employing parallel combination of basic width transistors.

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References

1. Hong, F., Cheng, B., Roy, S., & Cumming, D. (2011). An analytical mismatch model of nano-CMOS device under impact of intrinsic device variability. In *Circuits and systems (ISCAS), 2011 IEEE international symposium on* (pp. 2257–2260).
2. Cijan, G., Tuma, T., & Burmen, A. (2007). Modeling and simulation of MOS transistor mismatch. In *Proceedings of the 6th Eurosim* (pp. 1–8).
3. Wason, V., An, J., Goo, J.-S., Wu, Z.-Y., Chen, Q., Thuruthiyil, C., et al. (2006). Statistical compact modeling and Si verification methodology. In *Solid-state and integrated circuit technology, 2006. ICSICT'06. 8th international conference on* (pp. 1198–1201).
4. Drennan, P. G., & McAndrew, C. C. (2003). Understanding MOSFET mismatch for analog design. *IEEE Journal of Solid-State Circuits, 38,* 450–456.
5. Pelgrom, M. J., Tuinhout, H. P., & Vertregt, M. (1998). Transistor matching in analog CMOS applications. In *Electron devices meeting, 1998. IEDM'98. Technical digest, International*, (pp. 915–918).
6. Kuhn, K. J., Giles, M. D., Becher, D., Kolar, P., Kornfeld, A., Kotlyar, R., et al. (2011). Process technology variation. *IEEE Transactions on Electron Devices, 58,* 2197–2208.
7. Gummalla, S., Subramaniam, A. R., Cao, Y., & Chakrabarti, C. (2012). An analytical approach to efficient circuit variability analysis in scaled CMOS design. In *Thirteenth international symposium on quality electronic design (ISQED)* (pp. 641–647).
8. Bult, K., & Buchwald, A. (1997). An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm/sup 2. *IEEE Journal of Solid-State Circuits, 32,* 1887–1895.
9. Shyu, J.-B., Temes, G., & Yao, K. (1982). Random errors in MOS capacitors. *IEEE Journal of Solid-State Circuits, 17,* 1070–1076.
10. Shyu, J.-B., Temes, G. C., & Krummenacher, F. (1984). Random error effects in matched MOS capacitors and current sources. *IEEE Journal of Solid-State Circuits, 19,* 948–956.
11. Pelgrom, M. J. M., Duinmaijer, A. C. J., & Welbers, A. P. G. (1989). Matching properties of MOS transistors. *IEEE Journal of Solid-State Circuits, 24,* 1433–1439.
12. Serrano-Gotarredona, T., & Linares-Barranco, B. (2000). A new five-parameter MOS transistor mismatch model. *IEEE Electron Device Letters, 21,* 37–39.
13. Pelgrom, M. J., Rens, A. V., Vertregt, M., & Dijkstra, M. (1994). A 25-Ms/s 8-bit CMOS A/D converter for embedded application. *IEEE Journal of Solid-State Circuits, 29,* 879–886.
14. Lovett, S. J., Gibbs, G. A., & Pancholy, A. (2000). Yield and matching implications for static RAM memory array sense-amplifier design. *IEEE Journal of Solid-State Circuits, 35,* 1200–1204.
15. Bastos, J., Marques, A. M., Steyaert, M. S., & Sansen, W. (1998). A 12-bit intrinsic accuracy high-speed CMOS DAC. *IEEE Journal of Solid-State Circuits, 33,* 1959–1969.
16. Brito, J. P. M., & Bampi, S. (2009). A DC offset and CMRR analysis in a CMOS 0.35 µm operational transconductance amplifier using Pelgrom's area/accuracy tradeoff. *Microelectronics Journal, 40,* 1281–1292.
17. Mutlu, A. A., & Rahman, M. (2005). Statistical methods for the estimation of process variation effects on circuit operation. *IEEE Transactions on Electronics Packaging Manufacturing, 28,* 364–375.
18. Yelten, M. B., Franzon, P. D., & Steer, M. B. (2011). Surrogate-model-based analysis of analog circuits—Part II: Reliability analysis. *IEEE Transactions on Device and Materials Reliability, 11,* 466–473.

19. Jooypa, H., & Dideban, D. (2017). Impact analysis of statistical variability on the accuracy of a propagation delay time compact model in nano-CMOS technology. *Journal of Computational Electronics*. https://doi.org/10.1007/s10825-017-1108-2.
20. Kinget, P. R. (2005). Device mismatch and tradeoffs in the design of analog circuits. *IEEE Journal of Solid-State Circuits, 40,* 1212–1224.
21. Yuan, X., Shimizu, T., Mahalingam, U., Brown, J. S., Habib, K. Z., Tekleab, D. G., et al. (2011). Transistor mismatch properties in deep-submicrometer CMOS technologies. *IEEE Transactions on Electron Devices, 58,* 335–342.
22. Johnson, J. B., Hook, T. B., & Lee, Y.-M. (2008). Analysis and modeling of threshold voltage mismatch for CMOS at 65 nm and beyond. *IEEE Electron Device Letters, 29,* 802–804.
23. Keyes, R. W. (1975). Effect of randomness in the distribution of impurity ions on FET thresholds in integrated electronics. *IEEE Journal of Solid-State Circuits, 10,* 245–247.
24. Asenov, A., Kaya, S., & Brown, A. R. (2003). Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness. *IEEE Transactions on Electron Devices, 50,* 1254–1260.
25. Brown, A. R., Roy, G., & Asenov, A. (2007). Poly-Si-gate-related variability in decananometer MOSFETs with conventional architecture. *IEEE Transactions on Electron Devices, 54,* 3056–3063.
26. Ye, Y., Liu, F., Chen, M., Nassif, S., & Cao, Y. (2011). Statistical modeling and simulation of threshold variation under random dopant fluctuations and line-edge roughness. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 19,* 987–996.
27. International Technology Roadmap for Semiconductors. (2006). Retrived from http://www.itrs2.net/.
28. Bernstein, K., Frank, D. J., Gattiker, A. E., Haensch, W., Ji, B. L., Nassif, S. R., et al. (2006). High-performance CMOS variability in the 65-nm regime and beyond. *IBM Journal of Research and Development, 50,* 433–449.
29. Magnone, P., Crupi, F., Mercha, A., Andricciola, P., Tuinhout, H., & Lander, R. J. P. (2010). FinFET mismatch in subthreshold region: Theory and experiments. *IEEE Transactions on Electron Devices, 57,* 2848–2856.
30. Razavi, B. (2001). *Design of analog CMOS integrated circuits*. New York: McGraw-Hill.
31. Taur, Y., & Ning, T. H. (2013). *Fundamentals of modern VLSI devices*. Cambridge: Cambridge University Press.
32. Conti, M., et al. (2003). An integrated CAD methodology for yield enhancement of VLSI CMOS circuits including statistical device variations. *Analog Integrated Circuits and Signal Processing, 37,* 85–102.
33. Crippa, P., et al. (2002). A statistical methodology for the design of high-performance CMOS current-steering digital-to-analog converters. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 21,* 377–394.

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