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A subthreshold low-power CMOS LC-VCO with high immunity to PVT variations

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Abstract Internet of things is a topic of rising interest and intensive research, where power consumption is one of its most relevant challenges. This article presents a new radiofrequency subthreshold ultra low power LC voltage controlled oscillator (VCO). A graphical inductor optimization approach has been proposed and used to design the LC VCO leading to high performances in terms of power consumption, chip area and phase noise. It uses the adaptive body biasing technique to ensure high immunity to process, voltage and temperature variations. Realized in a 130 nm CMOS technology, the VCO occupies a total area of 0.234 mm^2. The measured frequency varies between 2.34 and 2.43 GHz. The post-layout simulation results show a phase noise of −116.1 dBc/Hz @1 MHz offset frequency, while the measured phase noise is −107.36 @1 MHz due to noisy measuring environment. The presented VCO provides a measured power consumption of only 168 μW from 0.6 V supply voltage, making it suitable for ultra low power applications.

Keywords VCO · Subthreshold · Adaptive body biasing · Optimization · Low power · PVT

1 Introduction

The rapid growth of Internet of things (IoT) applications and wireless sensor networks (WSN) boosts the necessity to design low power and reconfigurable integrated circuits [1, 2]. Indeed, autonomy is one of the main crucial characteristics of these applications. Designers have suggested many circuit techniques to reduce the power consumption, but it is still a limiting factor.

Moreover, IoT devices and connected objects are expected to be used at highly sensitive locations. Thus, it is necessary to design integrated circuits with high immunity to process, voltage, and temperature (PVT) variations in order to guarantee stable operation over these variations.

The wireless transceiver is one of the key elements of IoT systems. It allows transmission and reception of information using radiofrequency (RF) connectivity. The 2.4 GHz ISM (Industrial, Scientific and Medical) band is become very popular and is used for many wireless standards such as, ZigBee, WiFi Bluetooth and BLE (Bluetooth Low Energy). These different standards can be used in the wireless communication systems for IoT applications. The challenge is then to design ultra-low power transceivers suitable for multi-standard RF operation with high immunity to PVT variations regarding fundamental requirements of IoT applications: autonomy, stability and frequency agility.

The voltage-controlled oscillator (VCO) is an essential building block of RF transceivers. Design tradeoffs of VCO have been very stringent in terms of power consumption, phase-noise, area and tuning range [3]. The subthreshold region operation is a key technique that has been taken under consideration to decrease the power consumption. In this context, the purpose of this work is to propose a design method and some techniques aiming to

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reduce the power consumption of VCO and to improve its performances. A novel LC-VCO topology has been designed with MOS transistors biased in the subthreshold region while operating with low voltage headroom which results in low supply voltage. The VCO is also using the body biasing technique for PVT immunity.

This paper is organized as follows: Sect. 2 presents the Sub-1mW voltage-controlled oscillator operation together with PVT variations effect on the circuit performance. Section 3 investigates the proposed VCO topology and introduces the optimization methodology used to choose the optimum inductor. Section 4 describes the measurement results of the LC-VCO and compares them with existing oscillators in the literature. Finally, Sect. 5 concludes the paper.

2 Sub-1mW RF LC VCO design

The LC-VCO consists on an active circuit and an LC resonator, also referred as LC tanks. This tank element is made up of an inductor L and varactor C. Several topologies of the active circuit have been proposed in literature that provide the negative resistances to overcome the loss due to the parasitic tank resistance. The three most popular topologies are NMOS cross-coupled, PMOS cross-coupled and cross-coupled CMOS (complementary pair). The selection of any topology usually depends on the features of VCO design. For low power applications, the cross-coupled CMOS topology is recommended. Moreover, this topology can provide the same negative resistance with only the half current compared to other topologies. The CMOS cross-coupled structure presents another configuration based on current reused technique [4]. This configuration uses two PMOS and NMOS transistors. In the positive half cycle of oscillation, the operation of the traditional cross-coupled CMOS VCO and current reused VCO topologies is similar. However, in the next half cycle, the current reused topology does not need to provide current. Consequently, the same negative transconductance can be achieved with half current consumption. The current reuse is a very effective technique implemented in analog RF circuits to improve the power consumption. However, it suffers from asymmetrical outputs in terms of amplitude and phase [5, 6]. This suggests that a traditional cross-coupled CMOS topology is better for output stability and symmetry than the current reuse VCO. Reducing the supply voltage is another method to improve the power consumption, but it requires using of subthreshold MOS devices which present a high sensitivity to PVT variations.

2.1 The subthreshold operation

To implement ultra-low power analog circuits, the need of reducing the supply voltage pushed designers to use special approaches, such as employing subthreshold MOS transistors. The subthreshold regime (also known as weak inversion) exhibits high transconductance g_m for a given bias current and comparable noise performance with the superthreshold. In the subthreshold region, the gate source voltage V_{gs} is slightly below the threshold voltage V_{th} of the transistor and the concentration of carriers is very low but not negligible. The current is due to the diffusion, which is called subthreshold current. The drain current Ids is exponentially related to V_{gs} [7, 8].

2.2 Effect of PVT variations on MOS transistors biased in subthreshold regime

Relation between the transconductance g_m and the subthreshold current I_d is given as follows:

$$g_m = \frac{I_d}{nV_T} \tag{1}$$

Due to the exponential dependence of current I_d on V_T (thermal voltage), the MOS transistors biased in subthreshold region present a high sensitivity to PVT variations compared to the other regimes. In order to guarantee stable operation over these variations, designers should consider the variations of the threshold voltage and of the transconductance. These variations should be minimized especially for worst-case conditions.

Generally, for an NMOS transistor, the threshold voltage decreases when the temperature increases, while the thermal voltage increases when increasing the temperature [9, 10]. The relation between V_{th} and temperature can be approximated as:

$$V_{th}(T) = V_{th}(T_0) - KT(^T/_{T_0} - 1) \tag{2}$$

where KT is positive and T_0 is the reference temperature.

Moreover, the process variations can affect the gate oxide thickness and dopant concentrations. The variations of oxide thicknesses will contribute to vary the gate oxide capacitor as well as the threshold voltage. For example, in fast corners, all MOS transistors have a thinner gate oxide thickness and lower threshold voltage than typical corners.

2.3 Threshold voltage and body effect

The threshold voltage of a MOSFET is related to source-bulk voltage (V_{sb}) which changes the width of the depletion layer. This results in a modified charge in the depletion region as well as the voltage across the oxide. When the bulk voltage decreases, the threshold voltage increases due

to the excess of charges. This variation in threshold is called "body effect". For NMOS and PMOS devices, the change in threshold voltage can be given as a function of bulk potential V_{sb} [11].

$$V_{thn}(V_{sb}) = V_{th0} + \gamma \left(\sqrt{2\phi_F + V_{sb}} - \sqrt{2\phi_F} \right) \qquad (3)$$

$$V_{thp}(V_{sb}) = V_{th0} - \gamma \left(\sqrt{-2\phi_F - V_{sb}} - \sqrt{-2\phi_F} \right) \qquad (4)$$

where γ and V_{th0} present the body effect coefficient (also known as body factor) and the zero bias threshold voltage respectively when $V_{sb} = 0$.

Therefore, it can be deduced that controlling the body effect is necessary in order to avoid the high sensitivity to PVT. In this work, an adaptive body biasing technique has been proposed, since it can adjust automatically the threshold voltage of MOS transistors as well as the transconductance.

3 LC-VCO design

3.1 Proposed LC-VCO topology

The proposed VCO architecture is based on LC tank with CMOS cross-coupled structure as shown in Fig. 1. It is composed by a PMOS cross-coupled pair (M1, M2) and an NMOS cross-coupled pair (M7, M8). This topology is used to double the negative resistance value and then to decrease the power consumption. For a same bias, the transconductance is twice larger compared to that of NMOS (or PMOS) cross-coupled topology. The CMOS differential pair compensates the tank losses and provides the negative resistance G_{m_CMOS} that can be expressed as:

$$G_{m\_CMOS} = -\frac{G_{m\_NMOS} + G_{m\_PMOS}}{2} \qquad (5)$$

where G_{m_NMOS} and G_{m_PMOS} are the transconductances of NMOS and PMOS pairs respectively. The startup condition can be expressed as:

$$G_p = g_v + g_L + g_{ds,p} + g_{ds,n} \leq |G_{m\_CMOS}| \qquad (6)$$

where G_p is the passive element loss of the LC tank. g_v and g_L present the effective parallel equivalent conductances of the varactor and inductor respectively. $g_{ds,n}$ and $g_{ds,p}$ are output conductances of the NMOS and PMOS transistors respectively.

Furthermore, the adaptive body biasing technique is used in our circuit. It is known that this technique allows a high immunity to PVT variations and can improve the startup constraint. It can also decrease the MOS drain-source current. Thus, the power consumption can be decreased by tuning the threshold voltage.
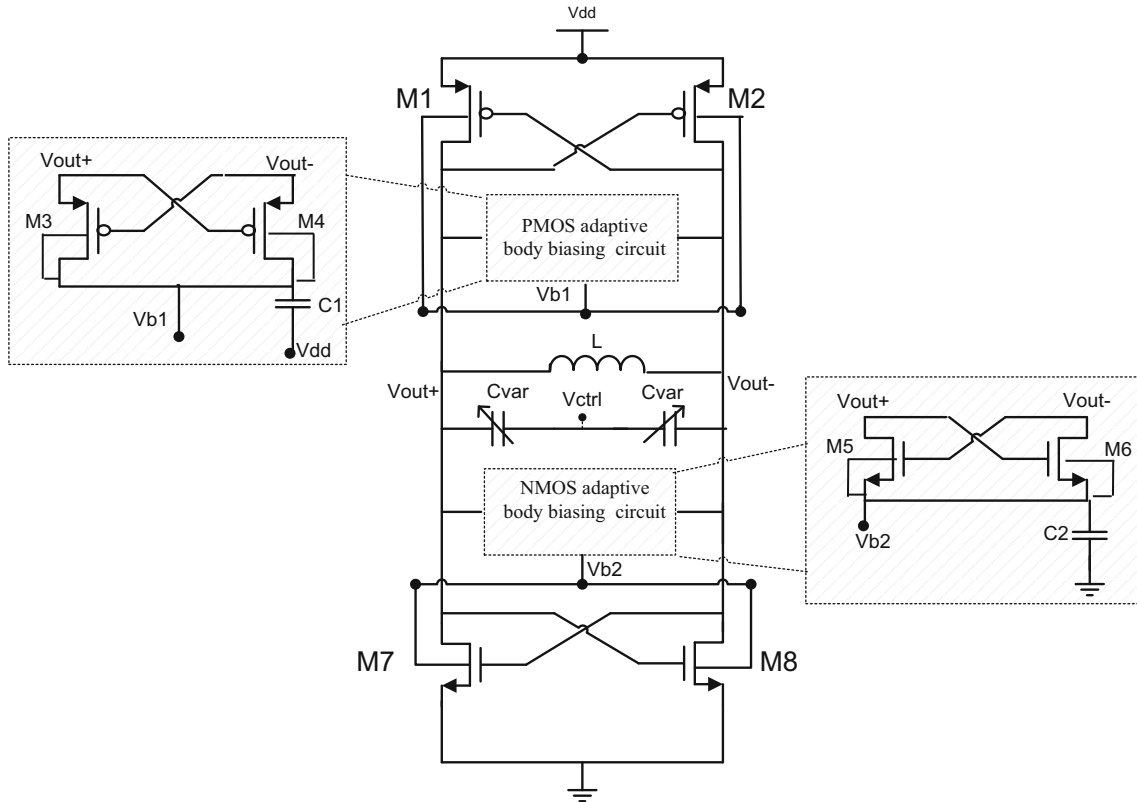

Fig. 1 Proposed LC-VCO topology

The novelty in the proposed VCO in this work consists in using adaptive body biasing blocs for both PMOS and NMOS cross-coupled pairs that are biased in the subthreshold regime. The basic idea of the adaptive blocs is to detect the output amplitude ($Vout_+$ and $Vout-$) and to feed it back to the body bias of the transconductance (G_{m_NMOS} and G_{m_PMOS}). When the output amplitude of the VCO varies, the bulk voltages of G_{m_NMOS} and G_{m_PMOS} are self-adjusted in order to stabilize the whole transconductance value and to maintain the oscillation. Concerning the NMOS cross-coupled pair, the adaptive body biasing circuit consists on a symmetric NMOS transistor pair (M5 and M6) and a grounded capacitor C_2 as shown in Fig. 1. This adaptive bloc detects the lowest magnitude and stores the obtained source voltage V_{b2} into the capacitor C_2. If the output amplitude decreases, V_{b2} increases, which lowers the threshold voltage of G_{m_NMOS} [12]. In this case, the negative transconductance increases, as well as the output amplitude. Concerning the PMOS cross-coupled pair, the adaptive body biasing circuit is similar to the first one. The NMOS transistors are replaced by PMOS transistors (M3 and M4) and the capacitor C_1 is connected to Vdd. If the output amplitude decreases, the voltage V_{b1} is reduced which implies increasing the negative transconductance of G_{m_PMOS} and thereby the output amplitude. In this case, the bulk voltage control is reversed compared to the body of transconductance G_{m_NMOS}.

In order to verify the operation of the used adaptive body-biasing technique, simulations of both G_{m_NMOS} and G_{m_PMOS} versus the supply voltage ($Vdd = 0.6\ V \pm 10\%$) have been performed using Cadence® tool with Spectre-RF simulator. Figure 2(a) shows the obtained G_{m_NMOS} for different values of V_{b2} (with constant body bias $V_{b1} = 0.6$ V), while Fig. 2(b) illustrates the variation of G_{m_PMOS} for different values of V_{b1} (with constant $V_{b2} = 0$ V). It can be seen that when $V_{b2} = 0$ V, G_{m_NMOS}

significantly decreases by 70% when Vdd increases from 0.54 to 0.66 V. Nevertheless, this decrease of G_{m_NMOS} can be adjusted by increasing V_{b2} as depicted in Fig. 2(a). Besides, it can be seen from Fig. 2(b), for $V_{b1} = 0.6$ V for example, a decrease of G_{m_PMOS} by 78% when varying Vdd from 0.66 V to 0.54 V. In this case, it can be noticed that the diminution of G_{m_PMOS} can be compensated by the decrease of V_{b1}. It can be noted that the control of both voltages V_{b2} and V_{b1} is made in a complementary way. Therefore, the adaptive body-biasing technique ensures the stabilization of the G_{m_CMOS} value and to improve the immunity to PVT variations.

According to (6), the negative transconductance G_{m_CMOS} should be high enough to maintain oscillation. Initially, G_{m_CMOS} is not sufficient and then the condition of oscillation is not satisfied. Then, adaptive body biasing circuits can be used to help the oscillation start-up. In the NMOS adaptive body circuit, the gate and drain voltages of M_5 and M_6 are initially set to Vdd/2. When these transistors are turned on, V_{b2} increases. Then, the threshold voltage of the G_{m_NMOS} decreases, resulting in higher value of G_{m_NMOS}. The PMOS adaptive body circuit operation is similar to the NMOS one. The source and gate voltages of M3 and M4 are initially set to Vdd/2. When these transistors are turned on, V_{b1} decreases. G_{m_NMOS} is then increased. Therefore, the oscillation condition defined in (10) is satisfied and the LC-VCO starts oscillating as shown in Fig. 3(b). In this case, the circuit auto-detects the output voltage of the VCO and adjusts the body bias voltages (lowers V_{b2} and increases V_{b1}). That reduces the transconductance and the power consumption.

Note that the adaptive body biasing technique requires the use of a triple well technology that offers the possibility of biasing the p-well independently from the p substrate. Hence, PMOS and NMOS bodies can be independently biased [13].
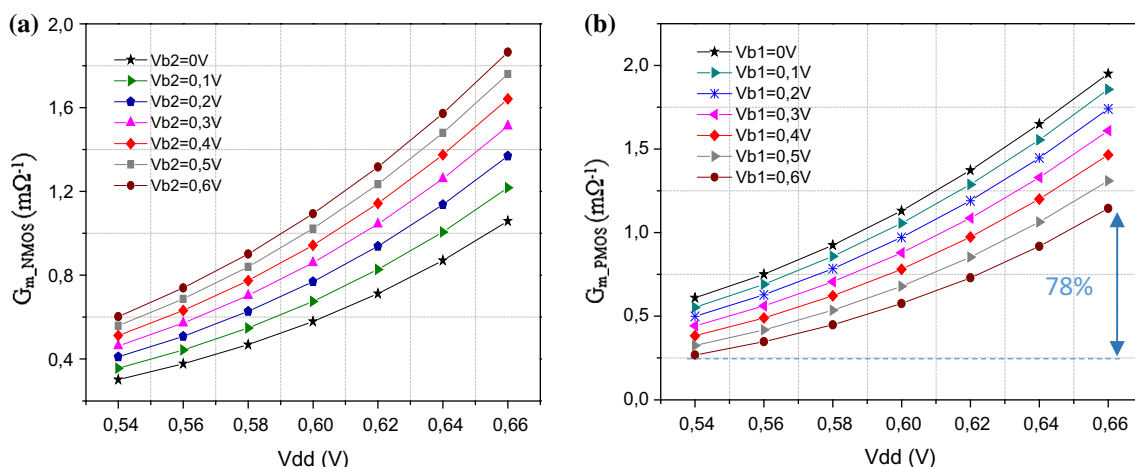
Fig. 2 Variations versus supply voltage of **a** G_{m_NMOS} for different values of V_{b2} and of **b** G_{m_PMOS} for different values of V_{b1}
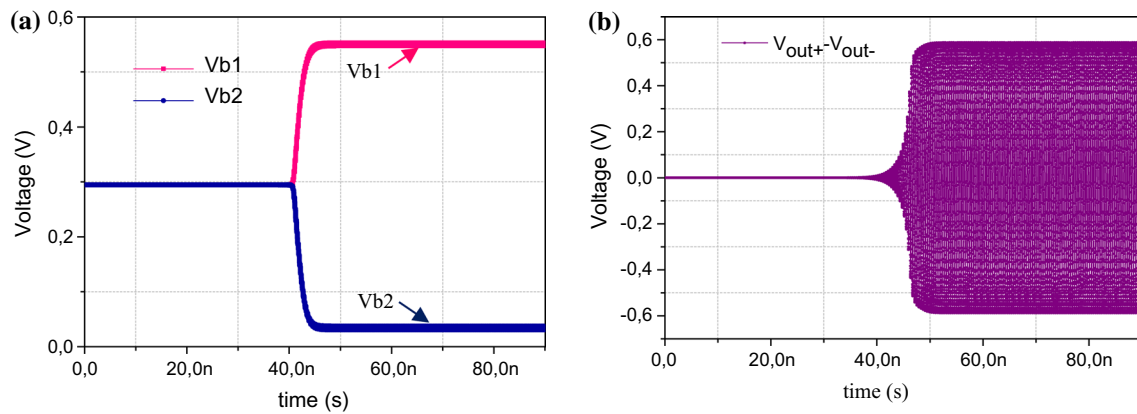
Fig. 3 Transient simulations of **a** both voltages V_{b2} and V_{b1}, and **b** of the output voltage of VCO

3.2 LC-VCO optimization approach

Designing LC-VCOs requires a great attention when considering the LC-tank since it determines the whole VCO performance. In this work, varactor diode has been used since it presents a good compromise between quality factor (Q_v), effective parallel equivalent conductance (g_v) and frequency tuning range. Moreover, its capacitance value varies linearly with *Vctrl* comparing to MOS varactors. Concerning the inductor, it is the most vital component in LC-tanks, since its quality factor (Q_L) affects the phase noise and its resistive loss (g_L) determines the power consumption.

Recent requirements of IoT applications boosts the need to design low-power, low-cost and multi-band oscillators. In order to optimize the LC-VCO design and to respect the various constraints, it is necessary to use convenient design methodologies. In this context, an optimization approach based on the study of the relationship between VCO's components and constraints is proposed (cf. Fig. 4).

The first step of the design optimization approach consists on the investigation of the VCO specifications before determining the type and the size of each component.

VCO's design constraints are studied essentially in terms of power consumption, phase noise, immunity to PVT variations, area occupation and frequency tuning range. It can be seen that the inductor does not influence on tuning range and immunity to PVT variations, but it affects directly the power consumption, area occupation and phase noise. The tuning range is affected mainly by the varactor, while the CMOS differential pair affects the phase noise and the power consumption of the VCO.

The next step of the design optimization approach is based on the study of the principal characteristics of LC-VCO's components (cf. Table 1). Concerning the spiral inductor, the most important parameters that must be taken into consideration are the quality factor (Q_L), the resistive losses (g_L), the self-resonant frequency (*SRF*) and the area occupation. For MOS transistors, the studied parameters are the number of gate fingers (N_F) and the dimensions (*W* and *L*). For the varactors, the most important parameters are the quality factor (Q_v), the resistive losses (g_v) and the tuning range capacity.

The effective parallel equivalent conductance of the varactor and of the inductor are respectively given by the following formulas:
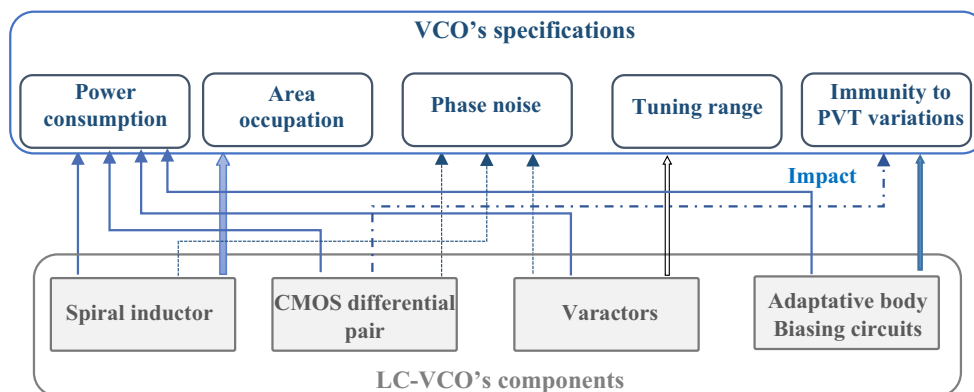
Fig. 4 Impact of the VCO's components on its specifications

Table 1 Characteristics of the LC-VCO's components

Components	Parameters
Spiral inductor	L, g_L, Q_L, SRF, area
Varactors	C_v, g_v, Q_v, tuning range
Transistors	W, L, N_F

$$g_V = \frac{1}{R_v} = \frac{C_v \omega}{Q_v} \qquad (7)$$

$$g_L = \frac{1}{R_p} + \frac{R_s}{(\omega L)^2} \approx \frac{1}{R_p} \qquad (8)$$

where R_v and R_s are respectively the parasitic serial resistances of the varactor diode and the inductance. R_p is the parasitic parallel resistance of L which can be written as:

$$R_p = Q_L^2 R_s \qquad (9)$$

where $\quad Q_L = \frac{\omega L}{R_s}$. $\qquad (10)$

Table 2 summarizes the design strategy for a low power consumption oscillator and its impact on other performances. For CMOS devices, a high number of gate fingers (NF) contributes to lower the gate resistance. This will improve the noise and power consumption performances. Besides, minimizing the varactor value C_v will lead to a low power and low phase noise. However, it will reduce the frequency tuning range.

Concerning the spiral inductor, when its value increases, the power consumption and the phase noise decrease while the occupation area increases. However, increasing the value of a passive inductor is not often evident and straightforward. The next sub-section will present the proposed optimization method in order to choose the optimum inductance.

3.2.1 Inductance optimization strategy

In this work, the proposed LC-VCO has been implemented in a 130 nm CMOS technology, which is a triple well technology that allows using the body biasing technique.

Table 2 Impact of LC-VCO components on LC-VCO performances

	LC-VCO performances			
	Power	Phase noise	Area	Tuning range
Maximizing L	++	+	− −	
Minimizing C_v	++	+	+	−
Maximizing NF	+	+	+	

$^{+ +}$ Very good , $^+$ good, $^{- -}$ very bad, $^-$ bad

Various types of inductor are proposed in the technology design kit (such as 'Ind_Sym_mf', 'Ind_Sym_la' and 'Ind_Sym_nw', etc.). A technological study of these different types has been first conducted in order to compare their specifications. S-parameters simulations have been achieved using Spectre-RF simulator of Cadence®. The obtained results have demonstrated that the 'Ind_Sym_la' inductor type gives a better compromise between SRF, g_L, occupation area, tuning range and Q_L than the other types.

Generally, different geometrical parameters are considered to optimize the inductor quality such as the inductor track width (W), number of turns (N), inductor shape (Nside), track-to-track spacing (S) and internal and external diameter (d_{in}, d_{out}). The influence of both parameters, N and W, has been reported. In the literature, inductors with large track width have been used aiming to lower the resistance and consequently to increase Q_L. However, they present some drawbacks such as increasing the substrate coupling and then the resonance frequency will be decreased. The inductors with minimum number of turns (Nmin) decrease the resistive losses g_L. However, regarding to the technological constraints, designers should occasionally increase the number of turns to increase the inductance value.

In this work, investigations on the inductor behavior begin by using both minimum number of turns (Nmin) and maximum track width (Wmax). Then, L has been varied and the inductance parameters in terms of quality factor, area occupation and resistive losses have been studied. For a fixed operation frequency, s-parameters simulations have been performed. The obtained results are depicted in Fig. 5. It can be noticed that increasing L improves the resistive losses g_L and reduces the quality factor Q_L. A compromise ought to be taken into account between achieving less quality factor and high resistive losses.

As shown in Fig. 5, the resistive losses vary from 0.65 to 6.7 mΩ^{-1}, when changing the inductance value from 1 to 10 nH. However, a high value of inductance (L = 10 nH) contributes to a high area occupation and high resistance that can degrade Q_L. Moreover, it can be seen that when L varies from 1 to 10 nH, the quality factor decreases from 9.6 to 1.6 while the area occupation increases from 0.2 to 0.1 mm^2.

Therefore, it is important to choose a high value of inductance to reduce g_L since it is the principle element responsible of the VCO's loss. For this value, the quality factor should be as high as possible by adjusting the inductor's geometrical parameters taking into account the technology constraints. Since the proposed design optimization approach considers both independent parameters, N and W, the idea consists to find the best combination of the couple [N, W]. Four combinations comprising both parameters have been fixed as follows:

Fig. 5 Impact of the inductance value on its quality factor, resistive losses and area
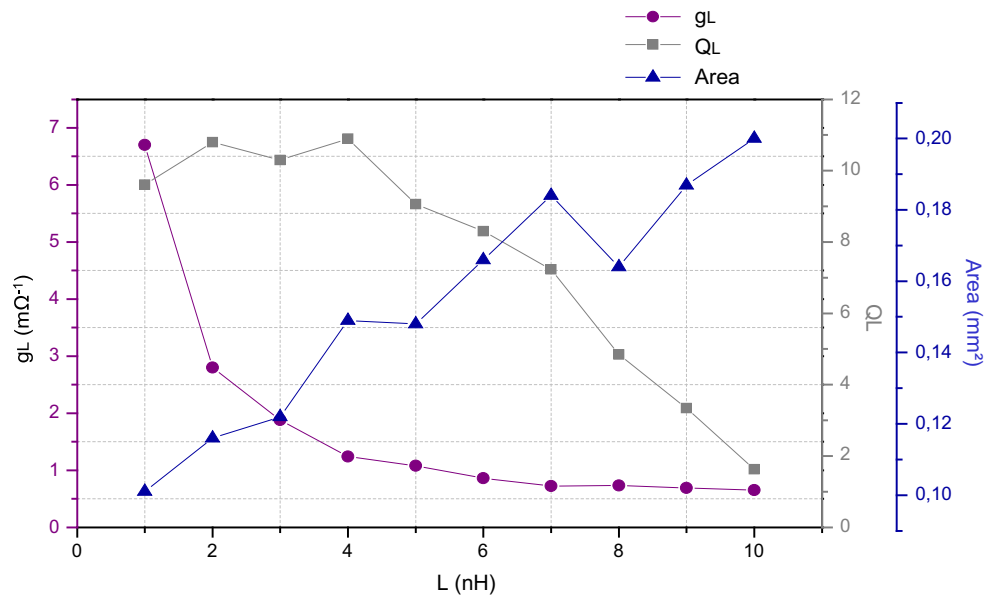
- First set: [Nmin, Wmax]
- Second set: [Nmax, Wmax]
- Third set: [Nmin, Wmin]
- Fourth set: [Nmax, Wmax]

The frequency of operation is chosen around 2.4 GHz. The track width can be adjusted between 5.01 and 11.99 μm in the used technology. For each inductance value, the maximum and minimum numbers of turns are fixed by technology.

Figure 6(a) presents the resistive losses variation for different [N, W] combinations for each inductance value, while Fig. 6(b) illustrates the quality factor variations. As shown in Fig. 6(a), for a 1 nH inductance value, the obtained resistive losses are approximately equal to 11 and 6.7 mΩ^{-1} with the first and fourth sets respectively. So a reduction around 39% in g_L is achieved. The maximum value of quality factor is approximately equal to 10, when using the first set, as shown in Fig. 6(b). So when using small inductance values, the best set is the first combination [Nmin, Wmax]. However, for a high inductance value (8 nH for example), the third set is the best combination that presents the best quality factor and lowest resistive loss.

Moreover, increasing the inductance value is strongly limited by the self-resonance frequency. Figure 7 depicts the impact of the SRF on the quality factor and the series resistance versus L for different [N, W] sets. In fact, when the SRF becomes close to the operation frequency, the quality factor is degraded (Fig. 7(a)) and the series resistance is increased (Fig. 7(b)). For this reason, it is necessary to consider a margin between these two frequencies. A variation of L around 30% is acceptable. Using the minimum track width Wmin is then necessary in order to

increase the resonance frequency. In this case, the [Nmin, Wmin] presents the optimum couple.

4 LC-VCO implementation and measurement results

A 2.4 GHz LC-VCO has been realized in 0.13 μm CMOS technology. Its layout and microphotograph are shown in Fig. 8. It occupies an area of 0.234 mm^2 without PADs (0.354 mm^2 with PADs). It is obvious that the spiral inductor occupies more than 2/3 of the total surface.

Based on the proposed optimization approach, a 7 nH inductance value using [Nmin, Wmin] has been used since it presents a good compromise between quality factor, resistive losses and area. The characteristics of this inductance are presented in Table 3.

In this work, low-leakage transistors with minimum channel length ($L_{min} = 0.13$ μm) have been used to reduce the power. Since the 0.13 μm CMOS technology is a triple well, it has been possible to separate substrate voltages of PMOS and NMOS transistors and then to use the proposed auto-biasing circuits.

In order to verify the reliability, the oscillator has been simulated with Spectre-RF simulator of Cadence taking into account the parasitic elements under various PVT conditions. The latters are usually combined as follows:

- Process (FF: Fast Fast SS: Slow Slow FS: Fast Slow SF: Slow Fast)
- Temperature (high temperature, low Temperature)
- Voltage (high voltage: Vdd +10%, low voltage: Vdd-10%).
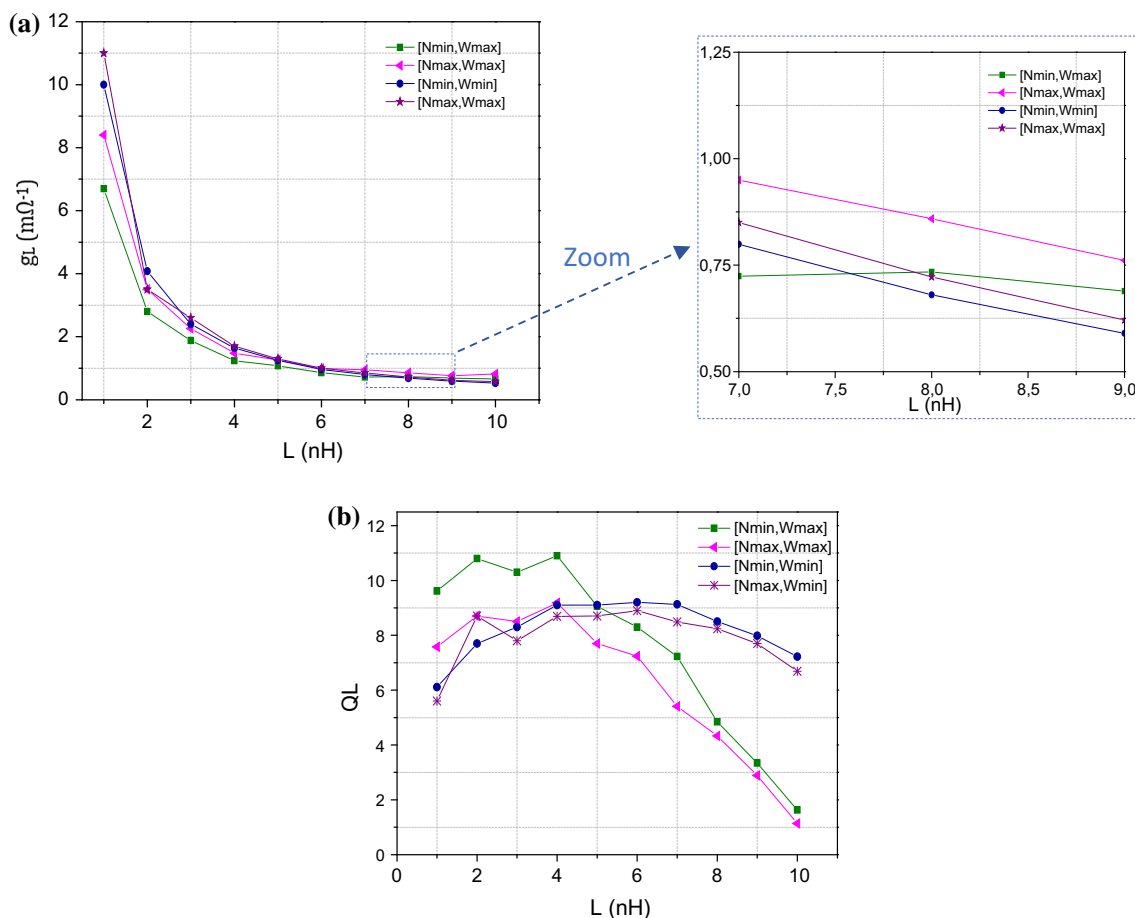
Fig. 6 **a** Resistive losses and **b** quality factor variations for different [N, W] combinations versus L

The VCO has been biased in the subthreshold regime with 0.6 V supply voltage. It has been post-layout simulated in three state corners. The first state combines the typical process and moderate temperature as well as moderate supply voltage (TT, 0.6 V, 27 °C). The second state combines best PVT corners (FF, 0.66 V, −40 °C). Finally, the third state combines worst PVT corners (SS, 0.54 V, 125 °C). In order to evaluate the VCO's immunity to PVT variation, it is essential to calculate the percentage of change versus the typical case. The obtained results are summarized in Table 4. It can be seen that the oscillation is maintained even in the worst case. Let us note also the small variation of the oscillation frequency by only 0.08 and 0.8%, as well as the phase noise by 1.8 and 1.2% compared to the typical condition. That confirms the robustness of the adaptive body biasing circuits used in our oscillator.

In order to assess the performance of this circuit, several measurements have been conducted. First, a very low power consumption of only 168 μW has been measured. Then, the VCO's frequency has been characterized (cf.

Figure 9). It varies between 2.34 and 2.43 GHz with a control voltage changing from 0.01 to 0.6 V.

The obtained results (in measurement and PLS) are depicted in Fig. 10. It presents the variation of the oscillation frequency versus Vctrl. As shown in Fig. 10, there is a small shift of 100 MHz between measurement and PLS results. This shift was predictable. In fact, in the PLS simulations, the performances of VCO have been evaluated using the RCc extraction mode from Virtuoso Analog Design Environment of Cadence and therefore does not take into account the inductive parasitic elements.

The phase noise has been also measured using the spectrum analyzer as depicted in Fig. 11(a). Note that this measurement has been performed at nominal operating conditions (room temperature, noise and interferences all around the measuring station). Figure 11(b) gives a comparison between the PLS and measured phase noise at 1 MHz frequency offset as a function of Vctrl. A phase noise of −106 dBc/Hz at 1 MHz offset with Vctrl = 0.5 V has been achieved, while it is about −116 dBc/Hz at 1 MHz with PLS. A slight degradation of the phase noise is
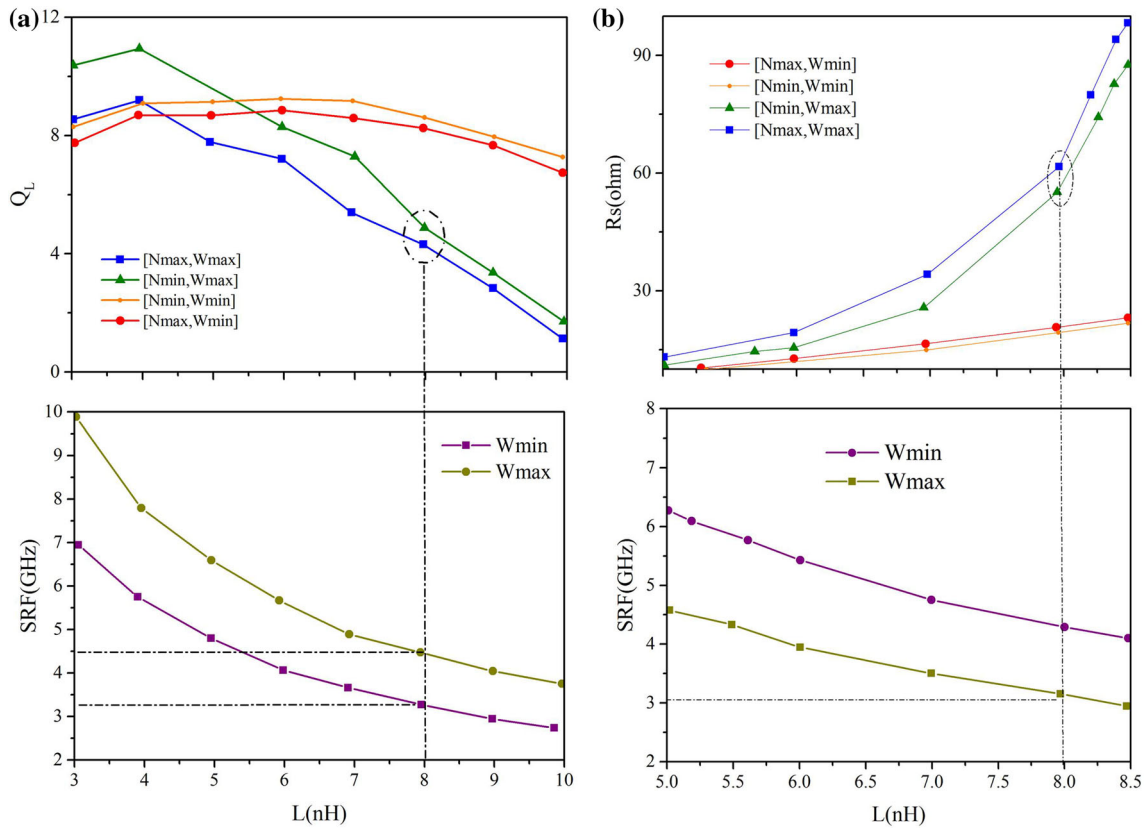
Fig. 7 Impact of the self-resonance frequency on **a** the quality factor and **b** the series resistance versus L for different [N, W] sets
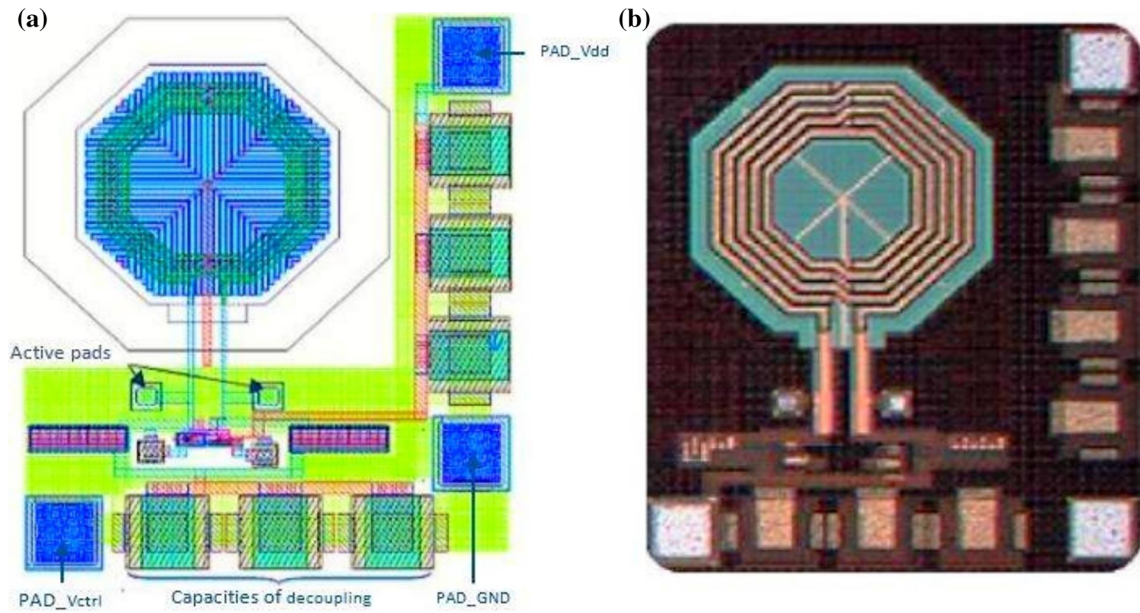

Fig. 8 **a** Layout and **b** microphotograph of the proposed LC-VCO

then observed but it can be noticed that it is almost steady versus *Vctrl* which is certainly due to the measure under noisy environment. RF circuit characterization such as noise measurement is usually done with shielded chamber.

Nevertheless, the VCO designed should be re-measured in a low-noise environment (shielded room, Faraday cage) with improved accuracy measurement to address the correct phase noise.

Table 3 Characteristics of the used spiral indutcor

Spiral inductor	Characteristics
$L = 7$ nH	$g_L = 0.799$ mΩ^{-1}, $Q_L = 9.13$,
[$Nmin, Wmin$] = [5, 5.01] μm	$Rs = 14\ \Omega$, Area = 0.124 mm^2

Table 5 summarizes the obtained performances of the circuit in measure and PLS. The LC-VCO can be characterized using two figures of merit considering the important performances of RF oscillator such as power consumption (P_{DC}), area, and phase noise and oscillation frequency. These two figures of merit can be defined as:
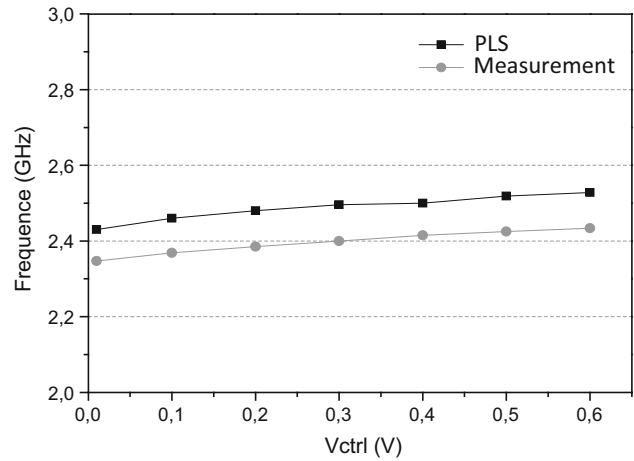
$$FoM = L\{\Delta f\} + 10\log(P_{DC}(mW)) - 20\log\left(\frac{Fosc}{Foffset}\right) \tag{11}$$

$$FoM_a = FOM + 10\log\left(\frac{\text{Area}(\text{mm}^2)}{1\ \text{mm}^2}\right) \tag{12}$$

Table 5 also compares the performances of the proposed LC-VCO with other similar oscillators biased in the sub-threshold regime. It can be seen that our VCO has the lowest power consumption for approximate frequencies.


Fig. 10 Variation of the oscillation frequency versus Vctrl

5 Conclusion

A design methodology using an optimization approach to size LC-VCO's components and to ensure high performances has been proposed in this work. It has been applied to design a 2.4 GHz ultra low-power LC-VCO based on the CMOS cross-coupled topology and biased in the

Table 4 LC-VCO performances under PVT variations

	TT, 0.6 V, 27 °C	SS, 0.54 V, 125 °C		FF, 0.66 V, −40 °C	
Frequency of oscillation (GHz)	2.528	2.518	0.08%	2.499	0.8%
Power consumption (μW)	157	118	24%	221	40%
Phase noise @1 MHz (dBc/Hz)	−116.1	−114.1	1.8%	−114.7	1.2%
Peak-to-Peak output voltage (mV)	591	440	25%	700	18%
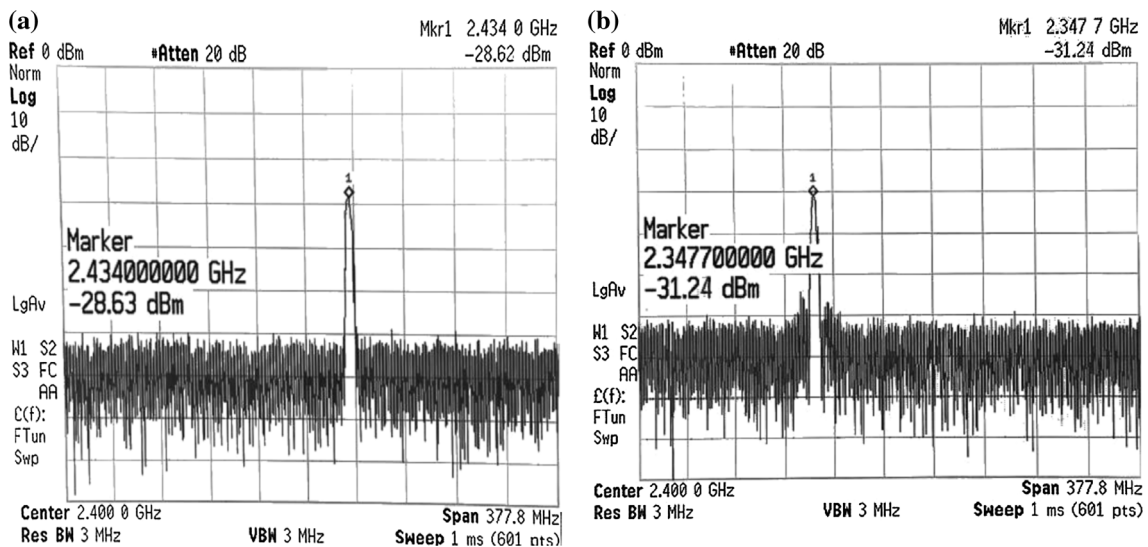
Fig. 9 Output frequency spectrum of the LC-VCO for **a** Vctrl = 0.6 V and **b** Vctrl = 0.01 V
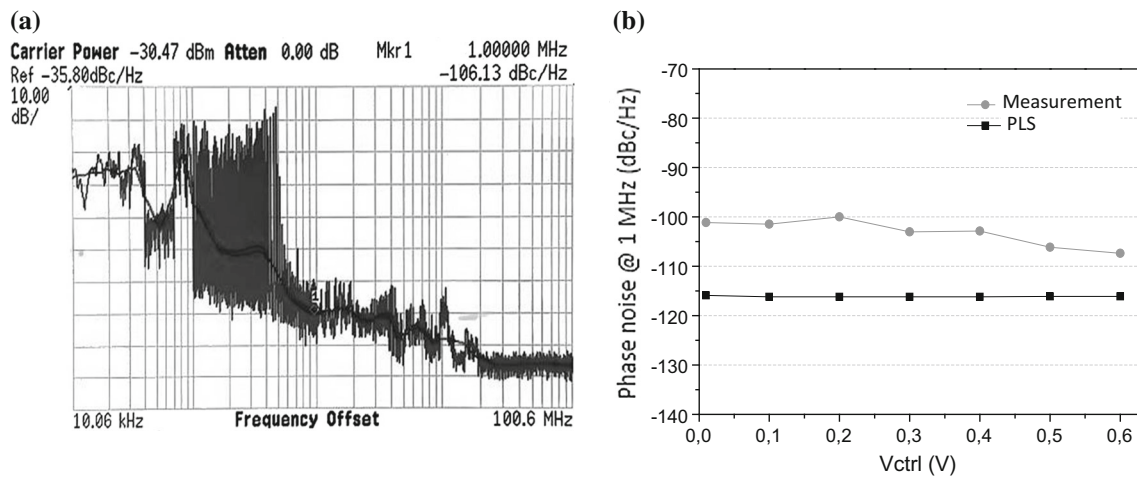
Fig. 11 **a** Measured phase noise profile for Vctrl = 0.5 V and **b** comparison between measure and PLS results versus Vctrl

Table 5 Performance comparison of the proposed subthreshold LC-VCO with similar oscillators in the literature

	[12]	[14]		[15]	[16]	This work	
	Measure	Measure		Measure	Measure	Measure	PLS
CMOS process (μm)	0.18	0.18	0.18	0.18	0.18	0.13	0.13
Supply voltage (V)	0.5	0.45	0.5	0.5	0.6	0.6	0.6
Power consumption(μW)	365	430	630	200	650	168	157
Frequency (GHz)	2.41	2.63	2.645	2.42	2.43	2.43	2.528
Phase noise (dBc/Hz)	−117.3 @1 MHz	−105.9 @400 kHz	−106.4 @400 kHz	−115.8 @1 MHz	−114 @1 MHz	−107.38@1 MHz	−116.1 @1 MHz
FoM (dBc/Hz)	−190	−185.9	−184.81	−190.5	−183.4	−182.81	−192.1

subthreshold regime. It has been implemented and fabricated in 0.13 μm CMOS technology. It achieves a low power consumption of only 168 μW from 0.6 V supply voltage. The occupied area is 0.234 mm^2 while the measured phase noise is −107 dBc/Hz at 1 MHz offset frequency in a nominal condition (a room environment with noise and interferences around the measuring station). Further measurements will be done to address the correct phase noise in low-noise environment.

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