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MIXED SIGNAL LETTER

LSB split capacitor SAR ADC with 99.2% switching energy reduction

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Abstract A highly energy efficient capacitor switching technique in a successive approximation register (SAR) analog to digital converter (ADC) for biomedical applications is presented. The proposed scheme based on new switching method, which combine the LSB split capacitive technique and monotonic method can reduce the average switching energy by 99.2% compared to the conventional SAR architecture. Besides reducing energy in each comparison cycle, the suggested method also achieves an 8× reduction in total capacitance used in the digital to analog converter over the conventional one with the same resolution. The proposed ADC can find application in biomedical engineering systems and other fields which low power consumption is needed.

Keywords Analog-to-digital converter · Successive approximation analog-to-digital converter (SAR ADC) · Digital-to-analog converter (DAC) · LSB split capacitive technique · Switching energy · Ultra low power

1 Introduction

SAR ADC is a very attractive choice for low power analog to digital conversion. Digital to analog converter, comparator and digital control logic are basic parts of this type of ADC. Since the DAC capacitive array dominates the overall power consumption compared with other parts, in recent years, different switching techniques have been used to improve the power efficiency of this block. Capacitive DAC in conventional SAR ADC [1] has good energy efficiency in the case of right initial guess, otherwise will cause a large energy penalty. The split capacitor method in [1] achieves a 37% reduction in switching energy compared with the conventional one. The monotonic switching technique of [2] reduces average energy by 81.2%, while the reduction achieved by Vcm-based method of [3] is 87.54%. The switching schemes in [1–3] consume considerable energy during identification of the significant bits, since large capacitors should change their states. The energy saving achieved by the V_{CM}-based monotonic switching (VMS) technique of [4] is 97.66%. The Charge redistribution method in [5] and the hybrid capacitor switching technique in [6] achieve 97.66 and 98.83% reduction in switching energy, respectively. However, most of these reported schemes still consume considerable energy, especially during identification of the first few bits. Moreover, in most prior work the effect of parasitic capacitors are not considered for analyzing the switching energy. In this letter, a new energy-efficient switching technique, with an energy saving of 99.2% is presented. In the proposed scheme with different switching sequence based on split capacitor technique and monotonic method, no energy is drawn from the reference voltage source during the first two clock cycles in the proposed method the LSB capacitor has been split into two equal sub capacitors C/2. Splitting the LSB capacitor into two equal sub capacitors C/2 result in 8× reduction in total capacitance of the ADC in compare with conventional scheme with same resolution since two least bits of the output is determined only by LSB capacitor. Moreover, the proposed technique ensure that the power dissipated in driving the switches is

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also reduced in compare with previously published works since it has only one switching event per cycle [7].

In Sect. 2, the proposed novel switching technique for reducing energy is explained. Simulation results and energy analysis are presented in Sect. 3. Discussion on noise is given in Sect. 4. Finally, conclusion is made in Sect. 5.

2 Capacitor switching technique

Benefiting least significant bit split capacitor structure, reducing power loss in first comparison cycles and also total capacitance reduction, are the main methods to decrease energy consumption due to capacitors switching in the proposed scheme. Power consumption in order to charge the MSB capacitor from V_{ref} to ground in second comparison cycle, forms notable energy in switching of capacitors [Fig. 1(a)]. E is the energy drawn from V_{ref} and can be calculated as

$$V_y = V_x - \frac{V_{ref}}{2} \tag{1}$$

$$E = \left(V_x - V_y\right) C V_{ref} = \frac{C V_{ref}^2}{2} \tag{2}$$

However as shown in Fig. 1(b), MSB capacitor state changes from ground to V_{ref} causes zero energy drawn from the voltage source during the second comparison cycle and thus a considerable energy saving achieved.

$$V_y = V_x + \frac{V_{ref}}{2} \tag{3}$$

$$E = \left(2\left(V_x - V_y\right) + V_{ref}\right) C V_{ref} = 0 \tag{4}$$

Considering the maximum energy waste in the first two bits determination, in the proposed DAC based on new switching scheme, the bottom plate of most significant bit capacitor in the sampling phase is connected to the ground and rest of them to V_{ref}. Displayed in Fig. 2, since first comparison is done immediately after the sampling phase due to top plate sampling, no switching energy is used in determination of the first bit [7]. After that, the bottom plate of capacitors in the lower voltage level side of arrays is converted to {1,1,1} while the bottom plate of capacitors in the higher voltage level side of arrays is remain unchanged. Where '1' and '0' represent V_{ref} and ground (Gnd), respectively. Figure 2 shows zero switching energy consumption along this stage.

Changing in the bottom plates state of capacitors to create new voltage level for comparison and determination of the remaining bits is done regarding to the previous outcome. To further understand the concept of energy saving as well as reducing capacity in various comparison stages, Fig. 2 shows the proposed method for a 4-bit SAR ADC.

During the determination of third bit for up transition (state A and D in Fig. 2), the bottom plate of capacitors are converted from {0,1,1} to {0,0,1} while for down transition (state B and C in Fig. 2) the bottom plate of capacitors are converted from {1,1,1} to {0.5,1,1}. Where '0.5' represents V_{cm} that equals $V_{ref}/2$. Changing the bottom plate of capacitors from {1,1,1} to {0.5,1,1} or keeping the bottom plate of capacitor C_i at V_{ref} and changing the bottom plate of capacitor C_{i+1} from V_{ref} to V_{cm} is equivalent to keeping the bottom-plate of C_{i+1} at V_{ref} and instead discharging the bottom-plate of C_i from V_{ref} to 0 same as monotonic method {1,0,1} [2]. However, the first approach which the bottom-plate of C_{i+1} is discharged to V_{cm} instead of discharging the bottom-plate of C_i to '0' is shown much less switching energy consumption. This technique has been incorporated in the proposed switching scheme. Note that i is the index of capacitor in the capacitor array.

Least bit is determined same as monotonic method [2]. In this cycle, the bottom plate of only one capacitor is switched from V_{ref} to $V_{ref}/2$ based on the previous outcome of the comparator.

It should be noted that a negative switching energy in some comparison cycles means that the capacitive array gives energy back to the reference voltage source and no extra energy is used which causes considerable energy saving in switching of capacitors [7]. Although, some authors, like [8, 9], do not take it into account by average power consumption calculations (the negative energy is considered as zero by them), in reality the effect of the negative energy has to be considered with the reference source configuration [10].

Demonstrated in Fig. 2, using split structure in least significant bits and also two unit capacitors is series to achieve $\frac{C}{2}$, cause an 8× reduction in total capacitance. As shown in Fig. 2 the least two bits of the ADC are determined only by this split capacitor which this is an advantage in compare with previously published works.

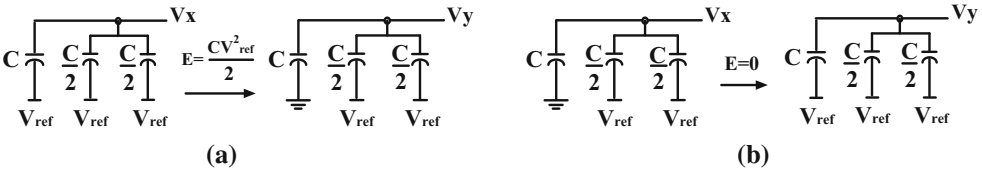

Fig. 1 Initial switching sequence after sampling phase

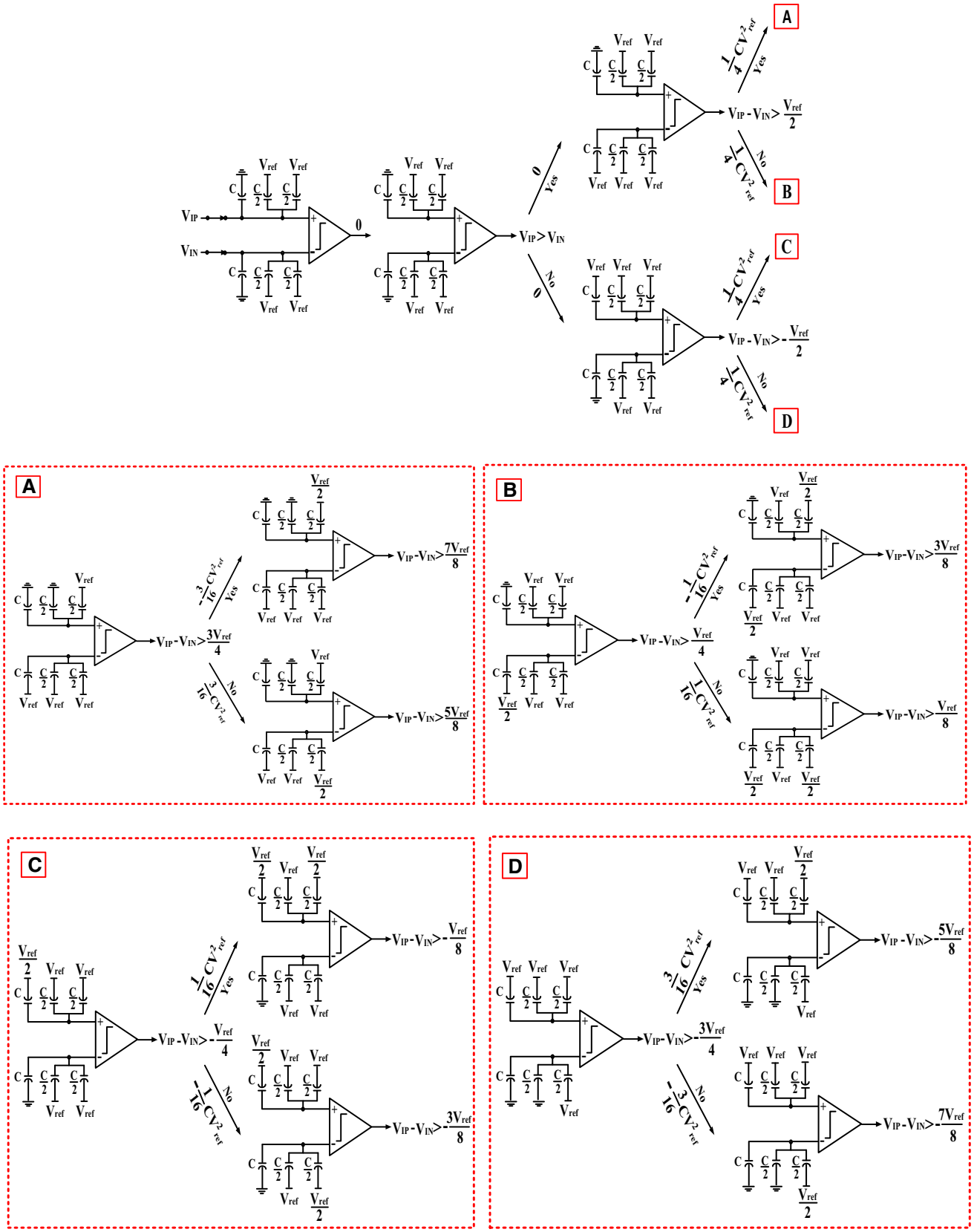

Fig. 2 Proposed switching scheme for a 4-bit SAR ADC

3 Switching energy analysis

Figure 3 shows convergence of common mode voltage to V_{cm} after determining final digital code in a 4-bit SAR ADC. Note that the common mode voltage at the comparator input in this method is independent from the input code and this is one of the advantages of this method.

The average energy consumption of conventional SAR ADC is 1363.3 CV^2_{ref}, while for the proposed scheme, it is only 10.8 CV^2_{ref} which achieves 99.2% reduction.

Table 1 shows the average energy consumption of different methods for 4, 8 and 12 bits SAR ADC simulated in MATLAB.

As displayed in Table 1, our method shown minimum switching energy for 4, 8 and 12 bits in compare with other switching methods.

3.1 Effects of parasitic capacitance

Since parasitic capacitance exists in reality between the capacitor plates and substrate, the effect of these parasitic capacitors should be taken into consideration for analyzing the switching energy consumption and the linearity of SAR ADCs.

A simple model for analyzing the effect of parasitic capacitors is shown in Fig. 4 [8].

For fair comparison with [8–10], the parasitic capacitance is also set to $C_{pt} = 10\%C_t$, $C_{pb} = 15\%C$, where C_t is the total capacitance of the ideal capacitor array; C is the capacitance of the unit capacitor; C_{pt} is the top-plate parasitic capacitance of the capacitor array and C_{pb} is the bottom-plate parasitic capacitor of the unit capacitor.

For investigating the effect of parasitic capacitors on nonlinearity of the DAC, the output voltage of DAC is calculated. The below equation express the output voltage of the DAC:

$$\begin{aligned} V_{out} &= V_p - V_n \\ &= \frac{\sum_{i=2}^{N-2} 2^{i-1} Cb_i^p + Cb_1^p + \frac{C}{2} b_0^p}{C_t} \\ &\quad - \frac{\sum_{i=2}^{N-2} 2^{i-1} Cb_i^n + Cb_1^n + \frac{C}{2} b_0^n}{C_t} \end{aligned} \tag{5}$$

where b_i^p represents the voltage value at the bottom plate of the capacitor in the upper capacitor array, b_i^n represents the voltage value at the bottom plate of the capacitor in the

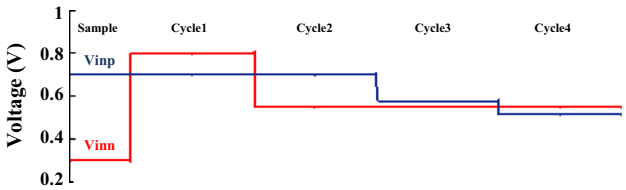

Fig. 3 Waveform of proposed scheme

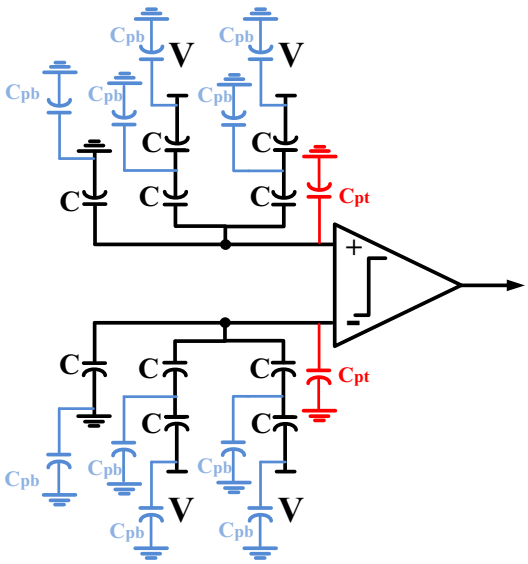

Fig. 4 Simple model for analysis of parasitic capacitance

Table 1 Comparison of switching scheme for 4, 8 and 12 bit SAR ADC

Switching technique	Average switching energy for 4 bit ADC (CV^2_{ref})	Average switching energy for 8 bit ADC (CV^2_{ref})	Average switching energy for 12 bit ADC (CV^2_{ref})
Conventional [1]	19.4	339.3	5459
Split capacitor [1]	11.5	211.3	3411
Monotonic [2]	4.5	64.5	1024
Vcm-based [3]	2.18	42.17	682
VMS [4]	0.38	7.9	127.9
Charge redistribution method [5]	0.125	7.9	127.9
Hybrid capacitor [6]	0.125	3.9	63.9
Sanyal and Sun [7]	0.0667	5.3	85.3
Tong and Ghovanloo [8]	0.0667	3.9	63.9
This work	0.0667	2.9	42.9

bottom capacitor array and i represents the index of the capacitors. Ct is the sum of all matrix capacitors in the upper or bottom part of the array.

By using proper common centroid layout design, the value of the C_{pb} capacitors in the bottom and upper part of the array should be identical. Consequently, the values of C_{pb} capacitors affect only on the C_t and according to Eq. (5) the linearity of the DAC is not affected by these parasitic capacitors. C_{pt} Capacitors are also affect only on the C_t and do not have direct influence on the linearity of the DAC. Note that these parasitic capacitors introduce the gain error in the DAC and affecting on the settling speed of the DAC.

The parasitic capacitors should also be charged during the conversion cycle, which raises the power consumption of the matrix.

Figure 5 shows the switching energy of proposed scheme and [7] after taking the parasitic capacitance into consideration. The average switching energy of the proposed scheme by considering parasitic capacitor is 16.78 CV^2_{ref} which is superior to other schemes that previously are reported [1–10].

3.2 Effect of capacitor mismatch

To simulate the influence of capacitors non-idealities random Gauss variations with standard deviation of 1% were added to capacitors values and 50,000 Monte-Carlo runs were performed for the proposed schemes. The simulation results are shown in Fig. 6. It can be seen that the maximum value of DNL and INL is 0.29 LSB and 0.25 LSB respectively.

3.3 Reset energy

After completing the evaluation of all the bits the capacitors arrays should be reset to the initial state [0,1,1,…,1]. That operation also consumes energy, which is not considered in most of the published switching schemes [10]. The reset energy is dependent on the state of the capacitor matrix at the end of the conversion phase. The behavioral simulation of the reset energy for the proposed switching schemes was accomplished in MATLAB. The reset energy for the proposed scheme is 48.12 CV^2_{ref} which is significantly lower than previously published switching scheme.

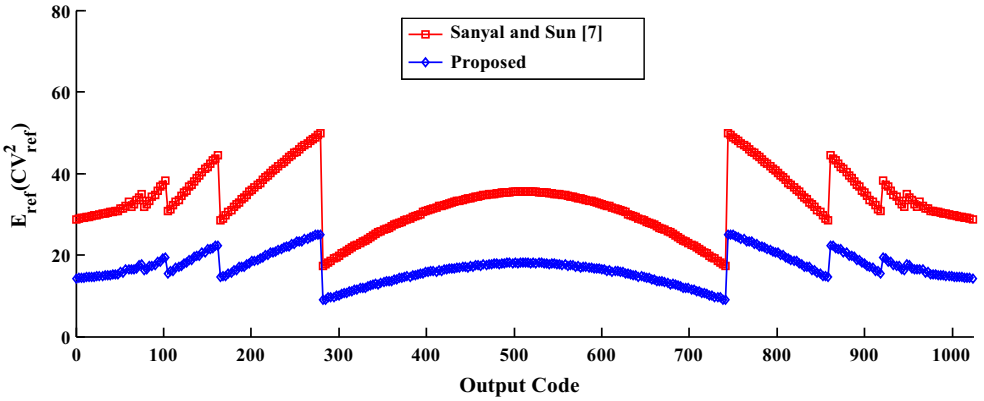

Fig. 5 Switching energy comparison for 10-bit SAR ADC in presence of parasitic capacitor (Cpt = 10%Ct, Cpb = 15%C)

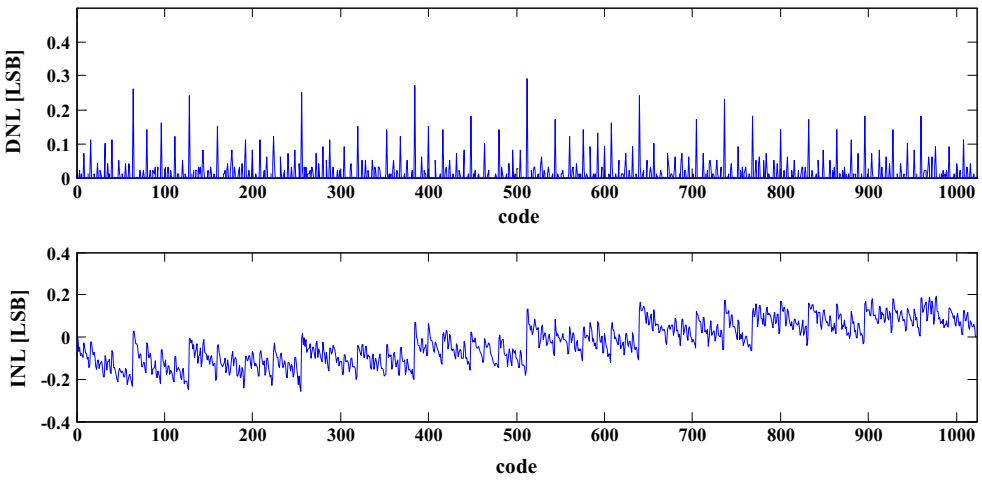

Fig. 6 INL and DNL of proposed scheme based on 50,000 Monte-Carlo runs

Figure 7 displays the average switching energy of most existing techniques by considering reset energy versus the output code simulated in MATLAB.

Table 2 shows the quantitative comparison between the proposed method and the previously published works.

The switching method which is proposed here shows 99.2% switching energy reduction in compare with the conventional switching method. Although in [10] 99.36% reduction in switching energy is reported, the parasitic capacitor is not considered in this method. By considering the parasitic capacitor the proposed method shows the average switching energy of 16.78 CV^2_{ref} which is significantly lower than previously published methods. Moreover, the suggested method achieves an 8× reduction in total capacitance used in the digital to analog converter (DAC) over the conventional one with the same resolution and sum of all matrix capacitor in the bottom and upper part of capacitor array is only 256 C for 10 bit resolution. Finally, the reset energy in the proposed method is only 48.12 CV^2_{ref} and by considering total energy (Switching Energy + Reset Energy) the proposed circuit shows lowest total energy in compare with other methods.

4 Discussion on noise

The proposed technique reduces total capacitance (C_t) by 8× compared with the conventional SAR ADC, which might raise concerns about the increase in the kT/C noise. So, the KT/C noise for all the previously published

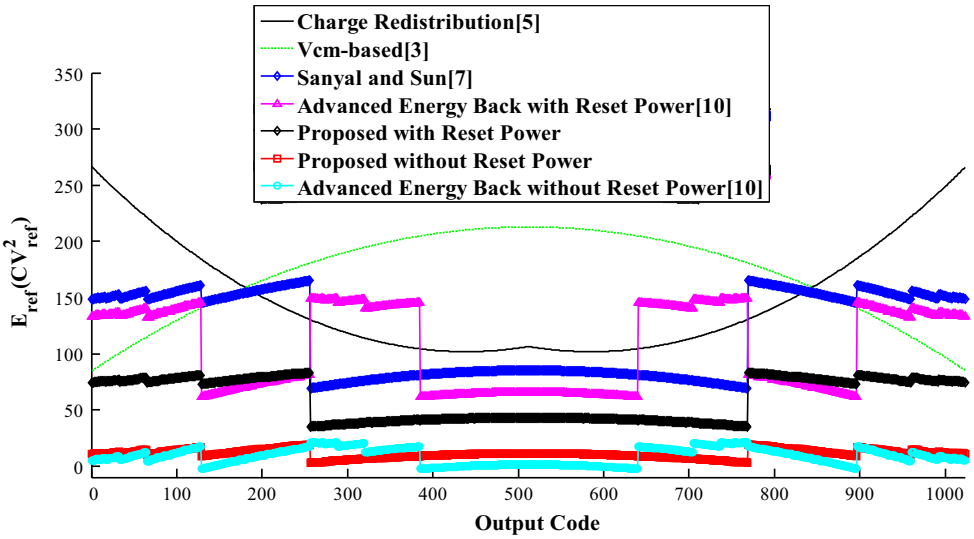

Fig. 7 Switching energy for 10 bit SAR ADC by considering reset energy

Table 2 Comparison of different switching methods for a 10-bit SAR ADC

Switching technique	Switching energy (CV^2_{ref})		Energy saving (%)	Area (C)	Common-mode input signal dependence	Reset energy	Total energy (switching energy + reset energy)
	Cpt = 0 Cpb = 0	Cpt = 0.1Ct Cpb = 0.15C					
Conventional [1]	1363.3	1686.1	Reference	2048	No	0	1363.3
Split capacitor [1]	852.3	1021.2	37	2048	No	0	852.3
Monotonic [2]	255.5	255.5	81.2	1024	No	0	255.5
Vcm-based [3]	170.17	209.2	87.54	1024	No	0	170.17
VMS [4]	31.88	56.3	97.66	512	No	105.4	137.28
Charge redistribution [5]	31.88	38.86	97.66	512	No	117.2	149.08
Sanyal and Sun [7]	21.3	33.15	98.4	512	No	95.75	117.05
Tong and Ghovanloo [8]	15.88	43.7	98.83	512	Slightly	50.84	66.72
Xie [9]	21.2	26.7	98.44	512	No	121.2	142.4
Osipov and Paul [10]	8.63	27.04	99.36	512	Slightly	111.75	120.38
This work	10.8	16.78	99.2	256	No	48.12	58.92

methods considering 2 fF as unit capacitor is calculated. The KT/C noise value for the conventional method [1] is 31 μV while this value for the monotonic [2] and proposed method is 44 and 89 μV respectively.

For more investigating on this KT/C noise value, the total input-referred noise $\sigma^2_{\text{tot,ADC}}$ of the proposed SAR ADC is calculated by [11]:

$$\sigma^2_{tot,ADC} = \sigma^2_{th} + \sigma^2_{comp} + \sigma^2_{qi} \quad (6)$$

where σ^2_{th} is the thermal noise from capacitor array, σ^2_{comp} is the input-referred noise from the comparator and σ^2_{qi} is the quantization noise.

Equation (6) is a key equation for SAR ADC design. To illustrate the impact of each parameters σ^2_{th}, σ^2_{comp} and σ^2_{qi} on the total input-referred noise $(\sigma^2_{\text{tot,ADC}})$ a SAR ADC with reference voltage of 1 V and an SNR of 56 dB is considered. The rms signal voltage, assuming sinusoidal, is 0.5 V/$\sqrt{2}$ and the 56-dB SNR translates to an ADC noise voltage of $\sigma^2_{\text{tot,ADC}} = 0.560$ mV.

Considering 10 bit SAR ADC, resulting in LSB = (1/1024) = 0.977 mV, $\sigma_{\text{qi}} = \left(\frac{\text{LSB}^2}{12}\right)^{1/2} = 0.282\,\text{mV}$, $\sigma_{\text{th}} = 89\,\mu\text{V}$ and $\sigma_{\text{comp}} \approx 0.69\,\text{mv}$.

Figure 8 shows value of different noises in the proposed SAR ADC.

As shown in Fig. 8, The achieved KT/C noise value for the proposed method is much smaller than comparator noise for 10 bit ADC with 1 V supply which indicates that the KT/C noise is not the limiting problem for the proposed method.

Moreover, 8× reduction of total capacitance is an advantage in compare with other methods since the use of the proposed switching technique allows the unit capacitance to be increased by 8× compared with the conventional technique when designed for the same kT/C noise. This eases the implementation issue involving fabrication of very small capacitors in silicon.

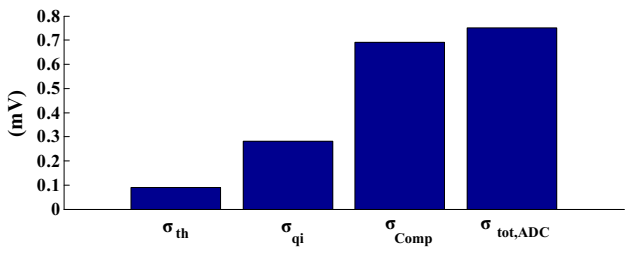

Fig. 8 Noise value in the proposed SAR ADC

5 Conclusion

A highly energy efficient capacitor switching technique for a SAR ADC is proposed. Top plate sampling, zero switching energy in first and second stage and also negative switching energy in several comparison cycles result in energy saving of 99.2% over the conventional one. Furthermore, using LSB split capacitor structure and serial unit capacitors for two least significant bits, achieve an 8× reduction in total capacitance. Finally, the proposed method uses only 48.12 CV^2_{ref} as the reset energy which shows the functionality of the proposed method. The proposed ADC can find application in biomedical engineering systems and other fields which low power consumption is needed.

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