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A 0.18μm CMOS voltage multiplier arrangement for RF energy harvesting

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Abstract This work presents a two-stage voltage multiplier (VM) useful in RF energy harvesting based applications. The proposed circuit is based on the conventional differential drive rectifier, in which the input RF signal has been level shifted using a simple arrangement. This signal is then used to drive the next stage, which has been formed by using gate cross-coupled transistors. As a result, the load driving capability of the proposed architecture increases. The load in this work has been emulated in terms of a parallel RC circuit. The architecture has been implemented using standard 0.18 μm CMOS technology. The measurements of the two-stage conventional VM (CVM) and proposed VM circuits were performed at ISM frequencies 13.56, 433, 915 MHz and 2.4 GHz for R_L of values 1, 5, 10, 3 and 100 KΩ with a fixed value of C_L equal to 20 pF. The performance evaluation has been done in terms of the power conversion efficiency (PCE) and average output DC voltage. The measured results show an improvement in PCE of 5% (minimum) for 13.56, 433 and 915 MHz frequencies, and up to 2% improvement for a frequency value of 2.4 GHz at the targeted load condition of 5 KΩ||20 pF, when compared with the measured results of the CVM circuit.

Keywords Energy harvesting · Rectifiers · ISM frequencies · RF to DC converter · Voltage multiplier

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1 Introduction

RF-energy harvesting is considered as an enabling technology for wireless sensor nodes used in applications based on the Internet of Things (IoT). It is useful where battery replacement is highly impractical either due to a large number of nodes or due to an inaccessible location of a node. Some of the examples where RF-energy harvesting is widely used are radio identification systems (RFID), biomedical implants, structural-monitoring and home automation [1–3]. As the name indicates, in RF energy harvesting, the energy required for the working of a system is extracted from the propagating radio waves. The device which converts the received RF into an usable DC power is commonly known as the rectifier [4]. This rectified energy is generally stored in a capacitor or rechargeable battery by the use of a power management unit [5]. In an RF energy harvesting based system, the usage of industrial, scientific and medical (ISM) frequencies is the most convenient. However, in the ISM band, the maximum effective isotropic radiated power (EIRP) permitted by the regulatory bodies is only 36 dBm (4 W) [6] which, restricts the coverage area and therefore a high RF sensitivity is desirable in the rectifier. This RF sensitivity is defined as the minimum incident RF power that is required by the rectifier to obtain a usable DC power [7].

In the literature, various rectifier architectures have been proposed that primarily utilize the Schottky diode. This preference for selecting the Schottky diode is mainly due to its low forward voltage and very high switching speed [8, 9]. However, owing to the ease of its fabrication process, the Complementary Metal Oxide Semiconductor (CMOS) technology is currently most widely used for on-chip implementation [10].

One of the commonly known limitations in CMOS-based implementations is the threshold voltage (V_{th}) of the Metal Oxide Field Effect Transistor (MOSFET) which, is the minimum gate-to-source voltage required by a transistor for the conduction [11]. Practically, an RF harvester is implemented through a multi-stage rectifier which is commonly known as a Voltage Multiplier (VM). In practice, the increased number of stages in VM architecture results in a decrease in RF sensitivity, which is mainly controlled by the threshold voltage of the switching transistors [12].

To overcome this issue, various threshold cancellation schemes have been proposed in the literature that are either technology-based [13] or circuit-based solutions [14].

The differential drive rectifier [15, 16] is a widely used rectifier architecture due to its ability to achieve the active threshold voltage cancellation of the switching transistors and, hence, results in higher power conversion efficiency. Various architectures, that are based on the differential rectifier, have been proposed in the literature [17, 18].

The proposed architecture is a two-stage voltage multiplier circuit, based on the differential drive rectifier and also is an extension of the works published in [19, 20]. These extensions are in terms of additional results and circuit topology. The issue of threshold voltage in the voltage multiplier circuit [16] has been addressed by deriving a DC voltage from the input RF signal and using it as the DC biasing voltage for switching transistors. As a result, it exhibits higher RF sensitivity and power conversion efficiency when compared with a two-stage conventional voltage multiplier circuit.

The paper is organized as follows. Section 2 provides an overview of the conventional differential drive rectifier and introduces the proposed solution with the implementation details. The measured performances of the conventional and proposed voltage multipliers are discussed in Sect. 4 and conclusions are drawn in Section V.

2 Voltage multiplier circuits

2.1 Conventional voltage multiplier

The conventional voltage multiplier circuit, formed by cascading two differential-drive rectifiers, is shown in Fig. 1. In the circuit, N and P are the N-type MOSFET (NMOSFET) and P-type MOSFET (PMOSFET) based switching transistors, C_P is the fly-capacitor, C_L and R_L represent the load capacitor and resistor respectively.

It has been mentioned in [16] that due to the development of a common mode DC voltage in the circuit, a low ON-resistance during the forward conduction mode and small leakage current during the reverse conduction mode has been attained. Due to these characteristics the architecture is widely used for RF energy harvesting. A rectifier is a highly non-linear circuit and hence, to obtain a detailed mathematical description of the circuit, a careful modeling in each region of MOSFET operation is required [21]. Therefore, in this work, to obtain a first order mathematical description of the circuit the following assumptions were made:

1. The peak amplitude of the applied RF signal is greater than the threshold voltage of the switching transistors.

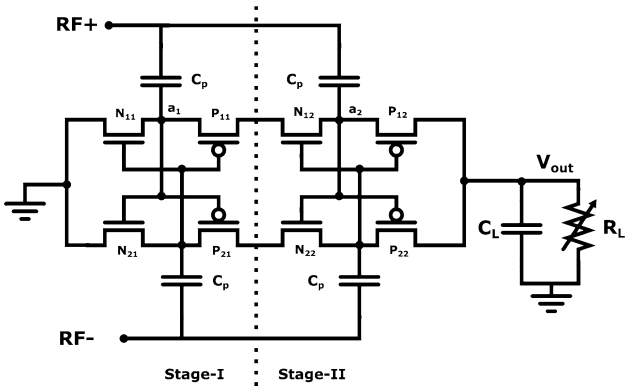


Fig. 1 Conventional differential drive rectifier based two-stage voltage multiplier circuit

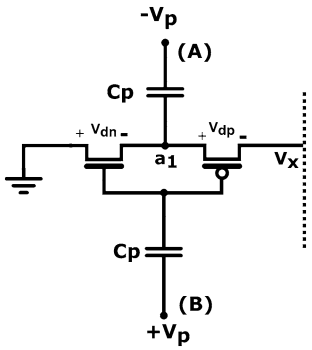


Fig. 2 Conceptual working diagram of stage-I

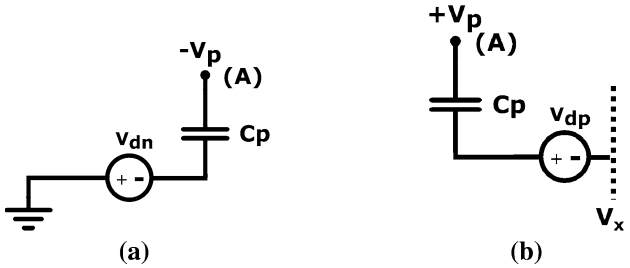


Fig. 3 Equivalent circuits for the **a** charging and **b** Discharging phases of stage-I

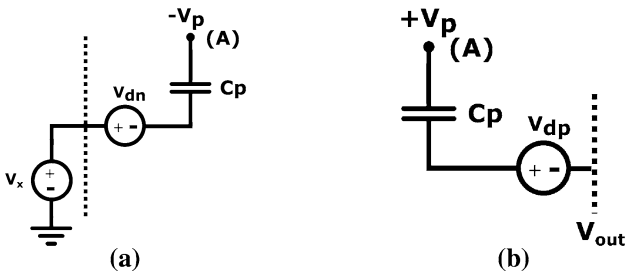


Fig. 4 caption equivalent circuits for the **a** Charging and **b** Discharging phases for stage-II

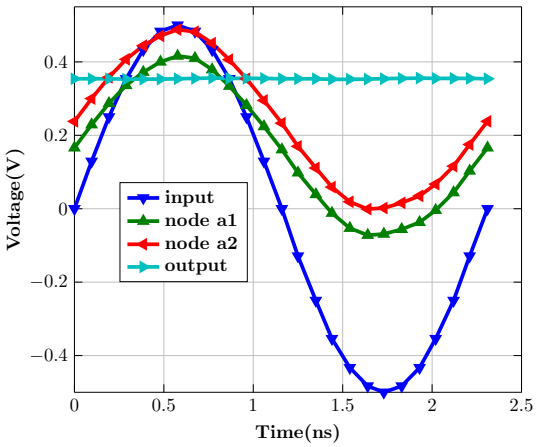


Fig. 5 Simulation results of conventional differential drive rectifier based two-stage voltage multiplier circuit

2. The only source of losses in the system is the drain-source voltage drop across the switching transistors.

The differential drive rectifier is a full-wave topology that is formed by using two voltage doublers. Thus, using the aforementioned assumptions the conceptual diagram of stage-I (see Fig. 1) can be represented in terms of the voltage doubler as :

Consider that when applying a single tone continuous RF wave (see Fig. 2) in the circuit, a negative peak amplitude $-V_p$ and a positive peak amplitude $+V_p$ appears at nodes (A) and (B) respectively.

As a result, the voltage doubler enters in the charging phase (see Fig. 3a) and thus, applying Kirchoff's voltage law (KVL) in the charging path, results in:

$$V_{cp} = -V_p + V_{dn} \tag{1}$$

where V_{cp} is the voltage developed across capacitor C_p and V_{dn} is the voltage drop across NMOSFET N_{11}. Since, the capacitor is assumed to be ideal, therefore the charge equivalent to the voltage V_{cp} will only be transferred to the next stage during the discharging phase. The discharging phase will start when the polarity of the input signal reverts as shown in Fig. 3b. Thus, by applying KVL in the discharging path:

$$V_x = 2V_p - (V_{dn} + V_{dp}) \tag{2}$$

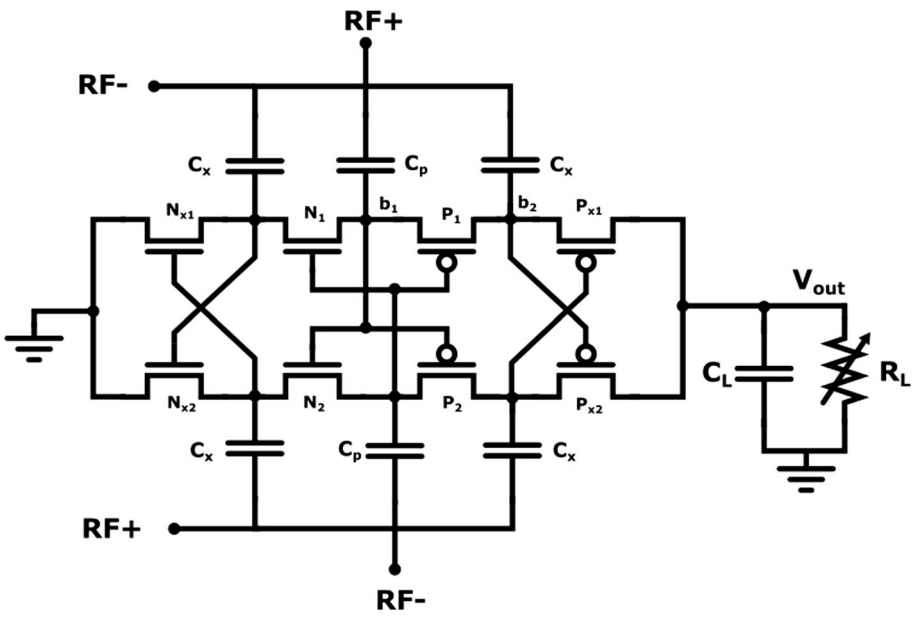
where V_x is the DC voltage that appears after the first stage. It can be seen in (2), that the loss (V_{dn}, V_{dp}) across the transistors is one of the causes of the reduced deliverable DC voltage V_x.

When the voltage multiplier architecture is formed, the voltage V_x acts as the DC voltage source for the next stage. Thus, equivalent circuits for charging and discharging phases for the second stage can be modeled as:

By applying the KVL first for the charging phase and then for the discharging phase (Fig. 4) will result in:

$$V_{out} = 4V_p - 2(V_{dn} + V_{dp}) \tag{3}$$

Fig. 6 Proposed two-stage voltage multiplier circuit



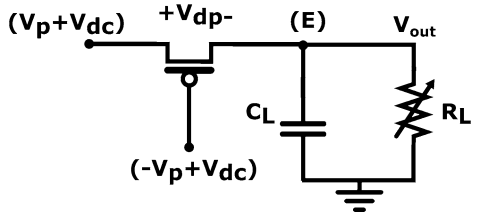


Fig. 7 Discharging path of gate cross-coupled switch

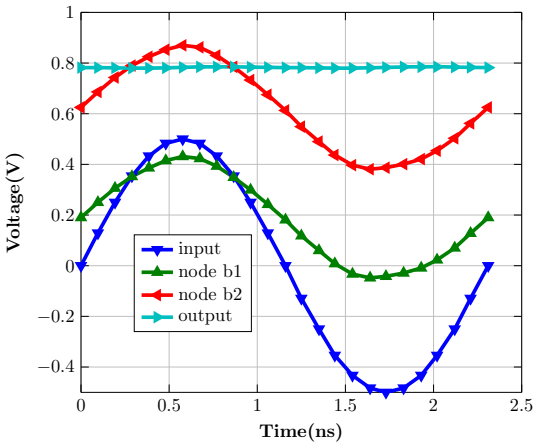


Fig. 8 Simulation results of proposed rectifier

Table 1 Simulation environment to determine device dimensions

S. no.	Parameter	Value
1	Load	5 kΩ|| 20 pF
2	Input signal	Single tone continuous wave RF signal of 500 mV (peak amplitude)
3	Frequency	13.56 MHz, 433 MHz, 915 MHz, 2.4 GHz
4	Reference performance metric	Output DC voltage, power conversion efficiency

To verify the first order expressions derived above of the circuit, simulations were done using the Spectre simulator in the Cadence environment using standard 0.18 μm CMOS technology. In these simulations, a single tone continuous wave RF signal of ISM 433 MHz frequency with peak amplitude of 500 mV was used with 5 KΩ||20 pF as a load. The simulation results of the conventional voltage multiplier are shown in Fig. 5 where it can be seen that the voltage signal of node a1 has been shifted by $\approx$ 150 mV. This DC shift is basically the voltage developed across the fly capacitor C_p during the charging phase [see Fig. 3a and Eq. (1)]. After the discharging phase of the first stage, the rectified DC output voltage V_x with a value of 300 mV was obtained. As mentioned earlier (see Fig. 4a), V_x acts as a DC source for the next stage. Thus, the DC-level of the voltage signal at node-a2 is higher than the voltage signal at node-a1. Finally, after the discharging phase of the second stage, an output DC voltage level of 350 mV has been achieved across the load.

Thus, it can be concluded from the simulation results that to get an acceptable level of the output DC voltage *i.e* = $3V_{th}$ under the given load condition, a high amplitude input RF signal would be required.

However, as mentioned earlier, a limit on the maximum transmitted power level has been set by the regulatory bodies [6]; therefore the use of this solution is restricted. As a result, in the literature, various alternate solutions have been proposed such as the use of a zero V_{th} MOSFET [22], pre-charging of the gate terminal during switching [23] *etc*. To date, none of these methods have been tested for heavy load conditions. Therefore, the proposed work is targeted towards the development of a multistage rectifier or VM with higher driving capability at the smaller received RF amplitude.

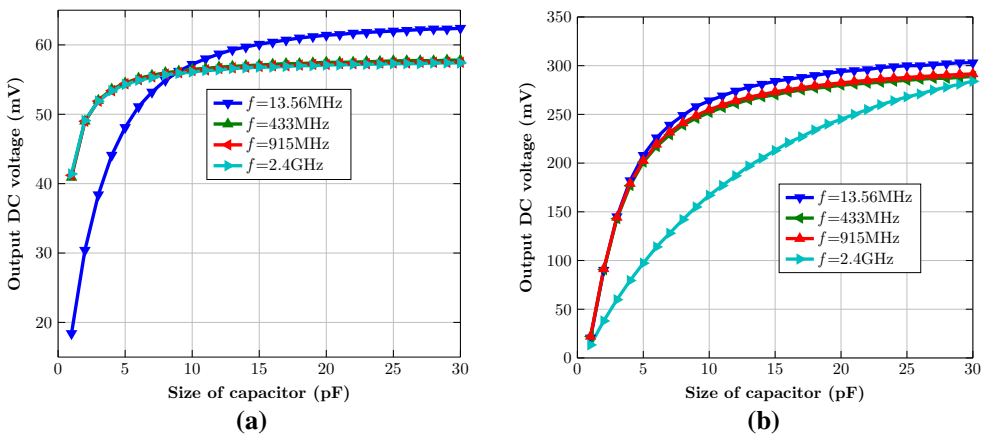


Fig. 9 Output DC voltage at **a** width = 10 μm **b** width = 100 μm

2.2 Proposed voltage multiplier

In the proposed work (Fig. 6), two strategies have been simultaneously used for reducing the losses in the rectifier. The first is a reduction in the number of switching transistors in the rectifying chain. Therefore, the voltage doubler has been realized using a gate cross-coupled switching arrangement; which, is widely used in oscillators, clock-doublers, comparators *etc.*, [11].

The second strategy is to shift the incoming RF signal by the DC level generated from stage-I. When this DC-shifted RF signal is fed to the gate cross-coupled switches, the switching action becomes effective. However, these improvements are only for heavy load-conditions *i.e.* $R_L \leq 10\,K\Omega$. To understand this phenomenon, consider the discharging path shown in Fig. 7 for one of the gate cross-coupled switches.

Referring to the simulation results of the proposed rectifier for a 500 mV peak RF input amplitude of frequency ISM 433 MHz for a load value of 5 KΩ||20 pF, the DC voltage level at the node b2 is 700 mV (see Fig. 8). Thus ideally, the voltage swing at the node b2 ranges from 1.2 V to 200 mV and similarly from 200 mV to 1.2 V at the gate-terminal of the transistor during one cycle of the incoming RF signal. As a result, the transistor works in a linear region during the discharging mode and is completely switched OFF during the charging mode if load ($R_L||C_L$) with a low time constant, *i.e.* heavy load conditions (5 KΩ||20 pF), is used. On the contrary, if the time constant is high, *i.e.* light load conditions, then the operating conditions of the transistor will tend towards the cut-off region. This phenomenon occurs because of the development of effective gate-source voltage due to the incoming DC-biased RF signal and the stored output DC voltage for the switching transistor.

Table 2 Device sizes used in implementation of proposed rectifier

S. no.	Transistors	Size
1	PMOSFET	4×30 μm/0.18 μm
2	NMOSFET	4×30μm/0.18 μm
3	Fly-capacitor	4×5 pF

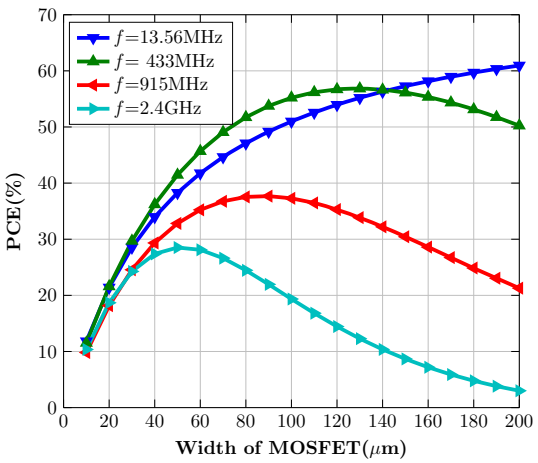


Fig. 10 Simulated power conversion efficiency at different transistor widths for C_p, C_x = 20 pF

2.3 Device sizing

In the literature, it can be noticed that the rectifier consists of only two components which are a MOSFET and capacitor. If the architectures are based on classical

Table 3 Performance comparison with state-of-the-art rectifiers

Ref.	CMOS tech (nm)	Operating frequency (MHz)	No.of stages and topology	Max.PCE (%)	at Pin (dBm)	Load condition (R_L)
[26]	65	13.56	1 (differential)	94.6	+17†	1 KΩ
[27]	350	13.56	1 (differential)	91.4	+21†	0.5 KΩ
[28]	180	433	1 (differential)	65.3	−15.2	50 KΩ
[29]	180	433	Multi-stage (single ended)	34	−7	50 KΩ
[7]	180	915	3 (differential)	28.8	−9	100 KΩ
[30]	130	915	16 (single ended)	22.6	−16.8	1 MΩ
[31]	180	2.4	3 (differential)	47	8.9	2 KΩ
[32]	Discrete	2.4	4 (single ended)	43	16	12 KΩ
This work	180	13.56	2 (differential)	65.5	−10	5 KΩ
This work	180	433	2 (differential)	43	−9	5 KΩ
This work	180	915	2 (differential)	31	−8	5 KΩ
This work	180	2.4	2 (differential)	16	−4	5 KΩ

† Calculated from the statistics provided in the work

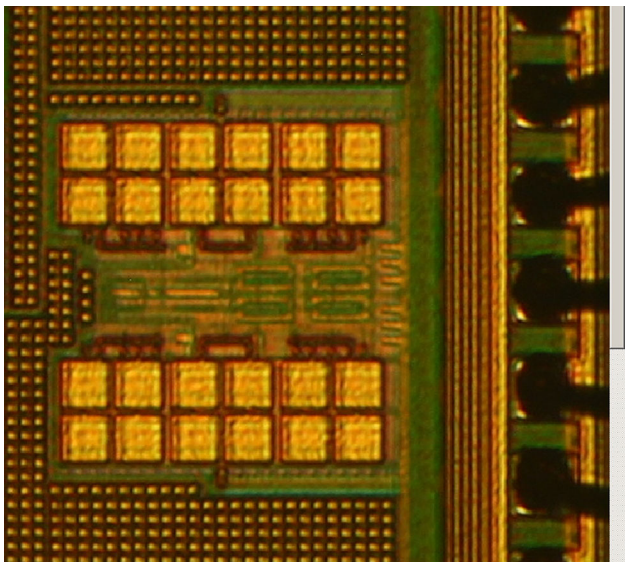


Fig. 11 Microphotograph of proposed voltage multiplier circuit

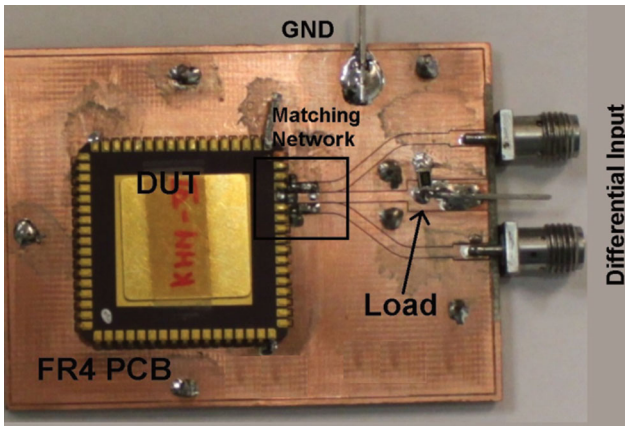


Fig. 12 Printed circuit board

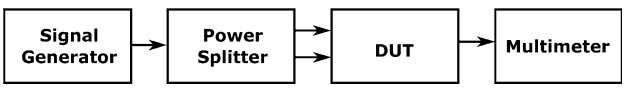


Fig. 13 Block diagram of measurement setup

Dickson topology [24], then either the PMOSFETs or NMOSFETs are used for switching and the capacitors for the pumping actions. On the contrary, if the rectifier is based on differential architecture then both PMOSFET and NMOSFET of the same aspect ratio are used to perform the switching action. Thus, it is noteworthy that for both design approaches the design variables are always two because only two components are being used.

In this work, to determine the device dimensions, a simulation based strategy was used. These simulations were done using the Spectre simulator in the Cadence environment with standard 0.18 μm CMOS technology for the simulation-environment listed in Table 1. Firstly, the transient simulations were performed by varying the size of the pumping capacitors (C_p and C_x) for different transistors widths. The simulation results for the minimum length (0.18 μm) transistors (PMOSFET, NMOSFET) for the width equal to 10 and 100 μm are shown in Fig. 9a, b. The performance of the rectifier was evaluated by using the maximum DC output voltage for the given RF signal amplitude. This is because it is an essential condition to obtain minimum acceptable DC amplitude level ($\approx 3V_{th}$) across the load. It can be observed from Fig. 9 that any value of the capacitor which is greater than 10 pF can be selected for the given operating frequencies irrespective of transistor width. Hence, the value of the pumping capacitors was selected as 20 pF (Table 1).

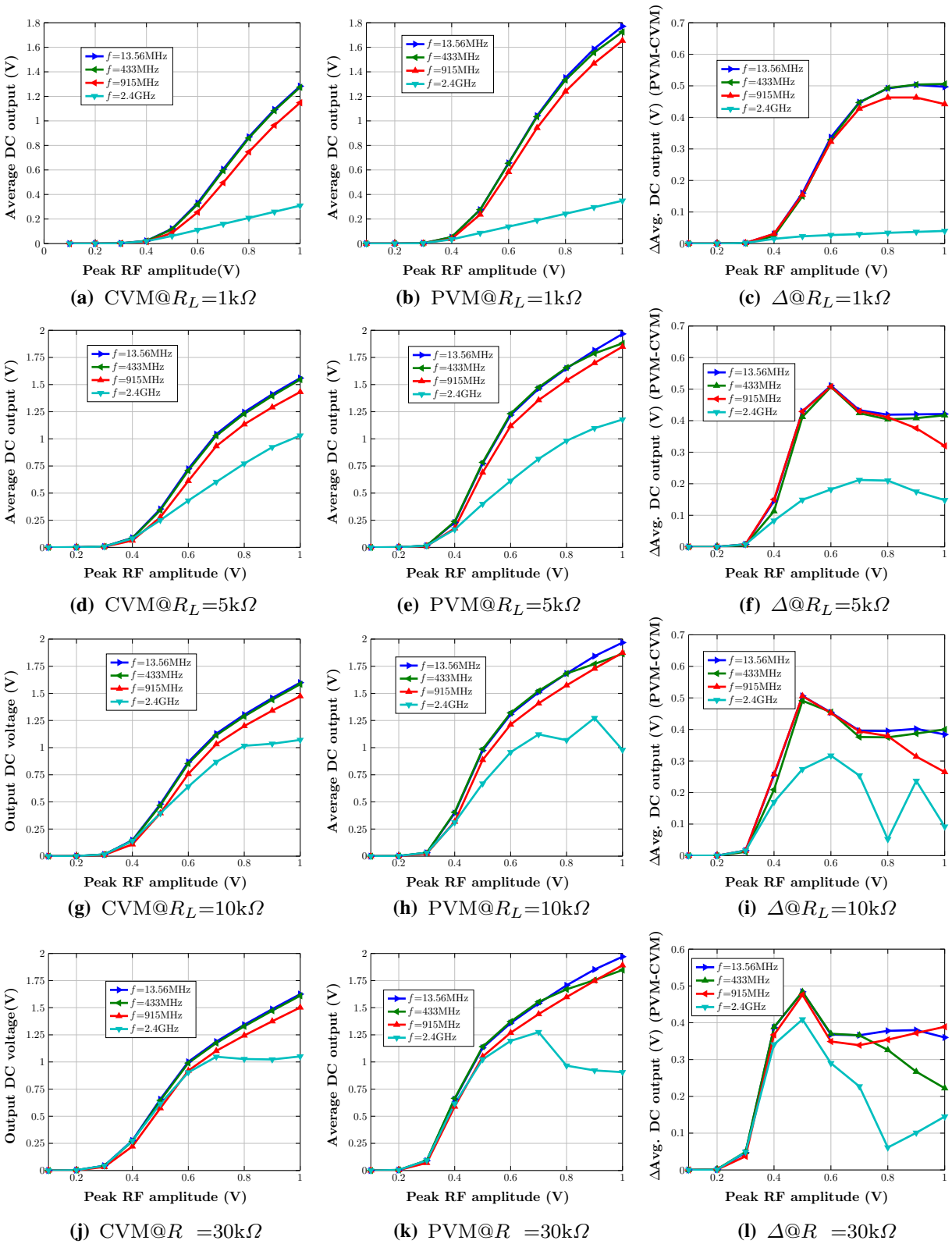
To determine the transistor size for the second stage, the power conversion efficiency was selected as the performance metric. The simulation results are shown in Fig. 10 where it can be observed that to obtain a moderate value of PCE for the given operating frequencies (except 2.4 GHz), the width of the transistors should be selected between 100 and 150 μm.

The final device dimensions used in the proposed implementation are mentioned in Table 2.

3 Measurement results

The proposed architecture was fabricated using a standard 0.18 μm CMOS technology. The microphotograph of the design is shown in Fig. 11. The total implementation area of the architecture is 0.137mm^2. A Printed Circuit Board (PCB), with a standard FR4 substrate that is used in the measurements, was milled in the laboratory (Fig. 12).

The length of the RF signal feed lines used in the PCBs were determined by using the Agilent ADS simulator. The packaged-IC was soldered directly onto the PCB as shown in the figure in order to minimize the parasitic effects during the measurements. The Agilent 8722ES network analyzer was used to measure the single port S-parameters by using the port extension feature. To obtain the differential input impedance value, the measured S-parameters were converted into the mixed mode S-parameters by using a Matlab program. In the next step, the Agilent ADS simulator was used to determine the discrete component values required to design the matching network for the



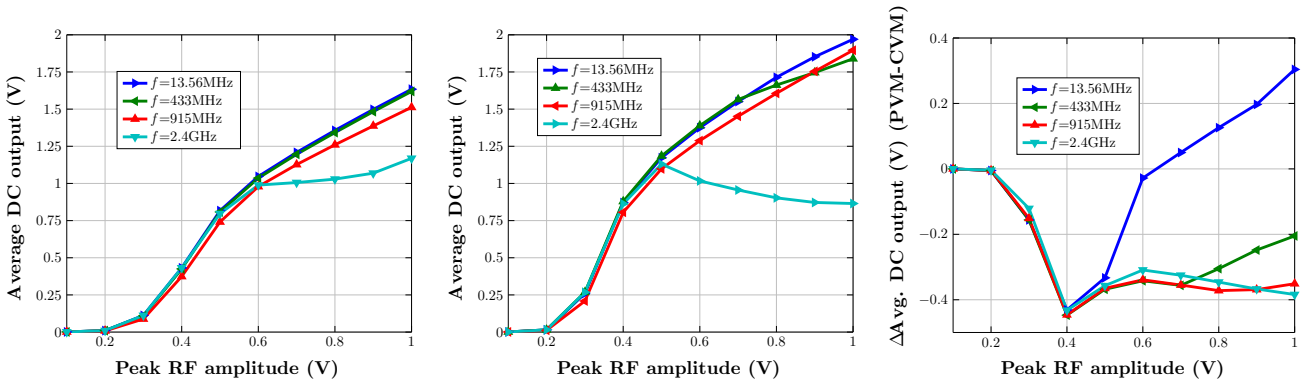
(a) CVM@R_L=1kΩ **(b)** PVM@R_L=1kΩ **(c)** Δ@R_L=1kΩ

(d) CVM@R_L=5kΩ **(e)** PVM@R_L=5kΩ **(f)** Δ@R_L=5kΩ

(g) CVM@R_L=10kΩ **(h)** PVM@R_L=10kΩ **(i)** Δ@R_L=10kΩ

(j) CVM@R =30kΩ **(k)** PVM@R =30kΩ **(l)** Δ@R =30kΩ

Fig. 14 Measured output DC voltage of **a** Conventional rectifier (CVM) **b** Proposed rectifier and (PVM) **c** their difference (Δ) and various ISM frequencies at different load conditions, **d** CVM@R_L = 5 kΩ, **e** PVM@R_L = 5 kΩ, **f** Δ@R_L = 5 kΩ, **g**, CVM@R_L = 10 kΩ, **h** PVM@R_L = 10 kΩ, **i** Δ@R_L = 10 kΩ, **j** CVM@R_L = 30 kΩ, **k** PVM@R_L = 30 kΩ, **l** Δ@R_L = 30 kΩ, **m** CVM@R_L = 100 kΩ, **n** PVM@R_L = 100 kΩ, **o** Δ@R_L = 100 kΩ



(m) CVM@R_L=100kΩ **(n)** PVM@R_L=100kΩ **(o)** Δ@R_L=100kΩ

Fig. 14 continued

circuit at ISM 13.56, 433, 915 MHz and 2.4 GHz frequencies.

The block diagram of the measurement setup is shown in Fig. 13 where the single tone continuous wave RF signal was provided by the signal generator R&HSMIQ06B. This signal was split into the differential signal using a 2-way-180°, DC to 4200 MHz, 50 Ω balun [25]. This differential signal was fed into the device under test (DUT) and the rectified DC output values were measured using the multimeter HP34401A.

The performance of the rectifier was characterized in terms of the power conversion efficiency (PCE) and maximum DC output voltage. The parameter power conversion efficiency [16] is defined as:

$$PCE(\%) = 100 \cdot \frac{Pout}{Pin} = \frac{\frac{V_{out}^2}{R_L}}{Ps(1 - |S_{dd11}^2| - |S_{cd11}|^2)} \quad (4)$$

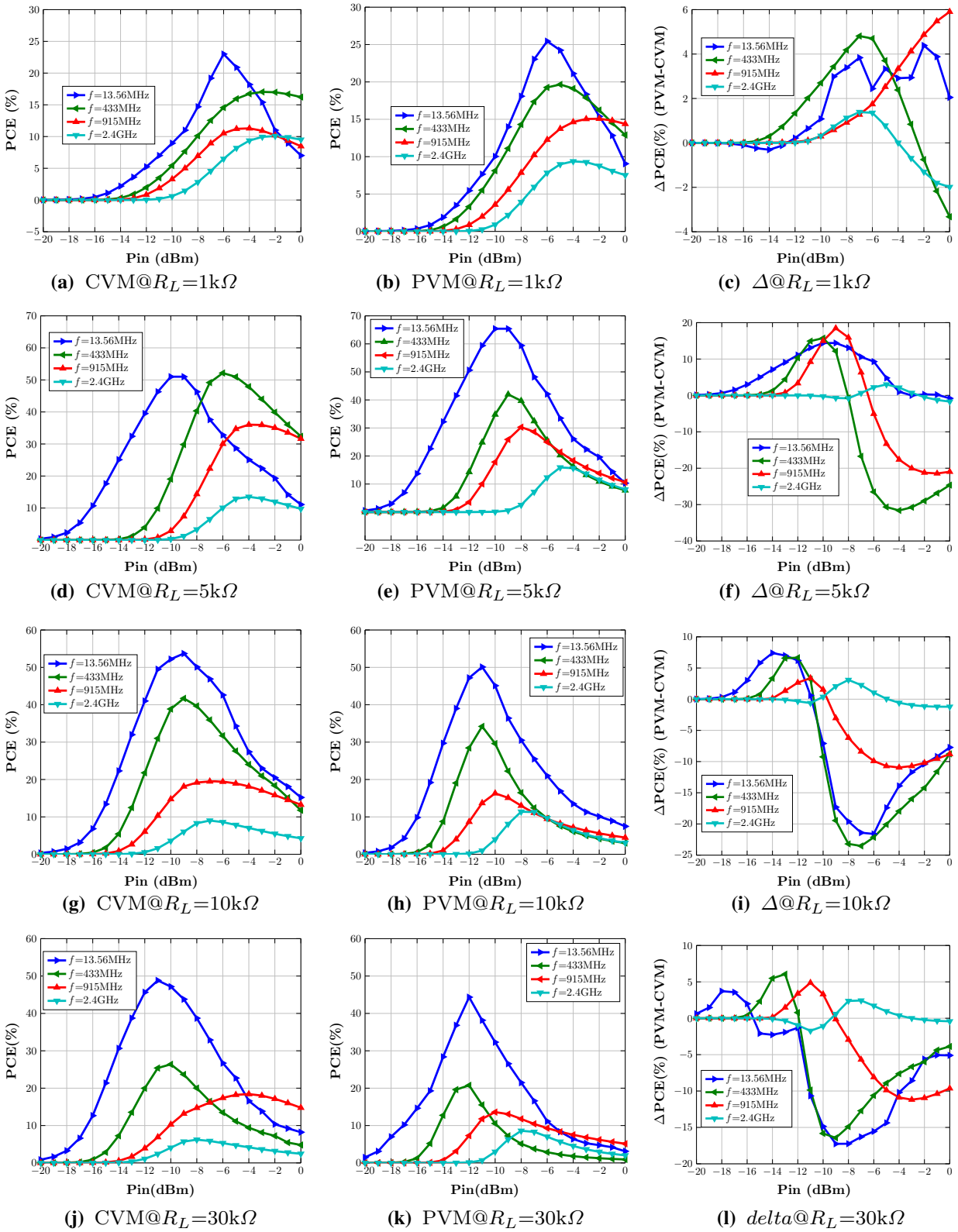
where *Pout* and *Pin* are the output-power and input-power respectively, and V_{out} is the output DC voltage measured across the load resistor R_L. The input power to the rectifier was calculated by using the mixed mode S-parameters [16]. Hence in (4), P_s is the source power, S_{dd11} is the differential-to-differential and S_{cd11} is the differential-to-common mode reflection coefficients, respectively. The measured output DC voltage and the power conversion efficiency for different resistive loads at different frequencies of the conventional two-stage voltage multiplier (CVM) and the proposed voltage multiplier (PVM) are shown in Figs. 14 and 15 respectively. A comparison of the performance of the present work with the state-of-the-art work on rectifier designing is presented in Table 3.

The following observations can be derived from the measured results:

- Proposed rectifier offers a minimum improvement of 300 mV in the output DC voltages for heavy load conditions *i.e.* $R_L \leq 30\,K\Omega$.
- Under light load condition *i.e.* $R_L = 100\,K\Omega$, the output DC voltages from the proposed rectifier are less than those of the conventional rectifier.
- Power conversion efficiency under heavy load conditions is at-least 5 % higher compared with the conventional rectifier for ISM frequencies of value 13.56, 433 and 915 MHz.
- Measured performance at ISM 2.4 GHz frequency is poor because the device dimensions used in implementation were not appropriate for this frequency (see Fig. 10).
- The measured performance decreases with increasing operating frequency because of the increase in losses induced by the PCB tracks, bonding wires, type of package and associated discrete components.

4 Conclusion

This work proposed a strategy for improving the driving capability of the voltage multiplier circuit used in RF energy harvesting. The proposed topology has been experimentally evaluated for various ISM frequencies at different load conditions. When compared with the conventional voltage multiplier the proposed solution requires additional capacitors which inherently increases the overall area. The proposed rectifier arrangement offers a moderate power conversion efficiency for heavy load conditions that makes it suitable for various RF energy harvesting based applications.



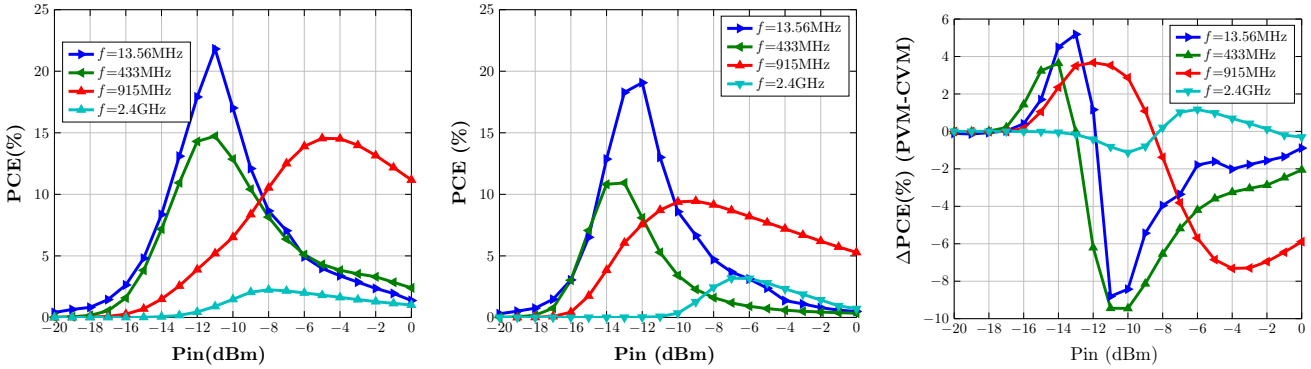
(a) CVM@R_L=1kΩ **(b)** PVM@R_L=1kΩ **(c)** Δ@R_L=1kΩ

(d) CVM@R_L=5kΩ **(e)** PVM@R_L=5kΩ **(f)** Δ@R_L=5kΩ

(g) CVM@R_L=10kΩ **(h)** PVM@R_L=10kΩ **(i)** Δ@R_L=10kΩ

(j) CVM@R_L=30kΩ **(k)** PVM@R_L=30kΩ **(l)** *delta*@R_L=30kΩ

Fig. 15 Measured power conversion efficiency of **a** Conventional rectifier (CVM) **b** Proposed rectifier and their (PVM) **c** difference (Δ) at various ISM frequencies for different load conditions, **d** CVM@R_L = 5 kΩ, **e** PVM@R_L = 5 kΩ, **f** Δ@R_L = 5 kΩ, **g**, CVM@R_L = 10 kΩ, **h** PVM@R_L = 10 kΩ, **i** Δ@R_L = 10 kΩ, **j** CVM@R_L = 30 kΩ, **k** PVM@R_L = 30 kΩ, **l** Δ@R_L = 30 kΩ, **m** CVM@R_L = 100 kΩ, **n** PVM@R_L = 100 kΩ, **o** Δ@R_L = 100 kΩ



(m) CVM@R_L=100kΩ **(n)** PVM@R_L=100kΩ **(o)** Δ@R_L=100kΩ

Fig. 15 continued

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