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A low load- and cross-regulation SIDO converter using an adaptive current sensor and LDO regulator with a selectable charge pump for mobile devices

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Abstract In this paper, a single-inductor dual-output (SIDO) converter is proposed to generate stable output voltages with low load- and cross-regulations for mobile applications. The proposed converter, which operates in the buck–boost or boost mode, employs an adaptive current sensor and a low-dropout regulator with a selectable charge pump to achieve low load- and cross-regulations. In addition, an error amplifier and comparators are implemented to provide stable dual output voltages of 1.8 and 3.3 V at an input voltage range of between 1.0 and 3.2 V. The proposed SIDO converter was fabricated using a 0.18-µm CMOS process technology and occupies a chip area of 1568 µm × 728 µm. The measurement results show that the maximum power efficiency, load-regulation, and cross-regulation are 89.2%, 0.120 and 0.088 mV/mA, respectively, when the load current changes from 10 to 50 mA.

Keywords Buck–boost converter · Cross-regulation · Current sensor · DC–DC converter · Load transient · Single-inductor multiple-output (SIMO)

1 Introduction

With the increasing use of smart mobile devices such as wireless sensor devices, smart phones, smart watches, and smart glasses, various technologies have been developed to extend the battery life and reduce the chip area [1–3]. To achieve a longer battery life, the power management integrated circuit (PMIC), which generates multiple supply voltages, requires a high power efficiency and needs a wide voltage range for the battery. For compact power management systems, the PMIC should have fewer power transistors and external components, such as inductors and capacitors.

To meet the aforementioned requirements, single-inductor multiple-output (SIMO) and single-inductor dual-output (SIDO) converters have been researched [4–13]. In [4–7], the time-multiplexing and time-sharing methods regulated the multiple output voltages of the converter, but showed poor ripple and cross-regulation characteristics. In [8], the power-distributive control method with free-wheeling switching achieved reasonable cross-regulation, but was still limited in lowering cross-regulation further because the cross-regulations of all outputs were interdependent. In [9], the hybrid converter using the current sensor and a low-dropout (LDO) regulator improved cross-regulation, but only when the input voltage was higher than the output voltage. The extended-PWM control method in [10] only employs the current sensor without using the LDO, thereby performing poor load- and cross-regulations. Furthermore, it occupies a large area due to many power switches needed to implement a buck and boost topology. The SIMO converter controlled by the freewheel charge pump in [11] uses the current sensor with the charge-pump, but the charge pump is only used for generating the additional output voltage, not for improving the regulation characteristic. Thus, it occupies a large area due to many power switches and requires a large output capacitor for the charge pump, and shows a poor regulation of the final output. Moreover, its power efficiency would be estimated to be low due to many switches and diodes, and charge pump operation at steady state.

In this paper, a SIDO converter is proposed to generate stable output voltages and achieve low load- and cross-

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regulations while minimizing the chip area; this is accomplished by using a fewer number of power switches with a small-sized freewheeling switch at a zero inductor current. The proposed converter using an error amplifier and comparators generates stable step-up and step-down output voltages, which are greater and less than the input voltage of the battery, respectively. The adaptive current sensor, which accurately detects the inductor current, and the LDO regulator with selectable charge pump is implemented in the proposed converter to achieve low load- and cross-regulations in both the buck–boost and boost modes. In Sect. 2, we describe the detailed architecture and operation principle of the proposed SIDO converter with an adaptive current sensor. In addition, the LDO regulator with a selectable charge pump is explained in detail. In Sect. 3, the experimental results are analyzed and compared with prior works. Finally, conclusions are given in Sect. 4.

2 The proposed SIDO converter

2.1 Architecture and operation principles

Figure 1 shows the block diagram of the proposed SIDO converter with four power switches (M_{FR}, M_N, M_{OP1}, and M_{OP2}), of which the main power switches (M_{FR} and M_N) control the inductor current (I_L) to adjust the load currents (I_{OUT1} and I_{OUT2}), and the output power switches (M_{OP1} and M_{OP2}) deliver I_{OUT1} and I_{OUT2} to the dual outputs (V_{OUT1} and V_{OUT2}), respectively. The proposed converter operates in the buck–boost or boost mode according to the mode selection signals (V_B) generated from the mode selector by comparing the input voltage (V_{IN}) with the target dual output voltages (V_{REF1} and V_{REF2}).

An adaptive current sensor detects I_L, then scales down and mirrors the peak I_L. The sensor subsequently generates the sensing voltage (V_{SEN}), which is used in the power delivery control block to improve the regulation characteristics using the current-programmed control [12–14]. A 4-input folded cascade error amplifier compares V_{OUT1} and V_{OUT2} with V_{REF1} and V_{REF2}, respectively, and generates an output error voltage (V_{ERR}) by accumulating all output errors. The comparators (CMP_1 and CMP_2) compare V_{OUT1} and V_{OUT2} with V_{REF1} and V_{REF2}, and generate V_{CM1} and V_{CM2}, which control V_{OP1} and V_{OP2}, respectively, to prevent the dual outputs from the over-voltage. The power delivery control block then generates the non-overlapping gate driving signals (V_{FR}, V_N, V_{OP1}, and V_{OP2}) according to V_{SEN} and V_{ERR} in order to adjust the energizing and de-energizing periods of the inductor. V_{FR} controls the freewheeling switch (M_{FR}) at a zero inductor current to avoid a reversely flowing inductor current, whereas V_N, V_{OP1}, and V_{OP2} control the switches (M_N, M_{OP1}, and M_{OP2}, respectively) to energize and de-energize I_L. The energizing and de-energizing periods, along with V_{CM1} and V_{CM2},

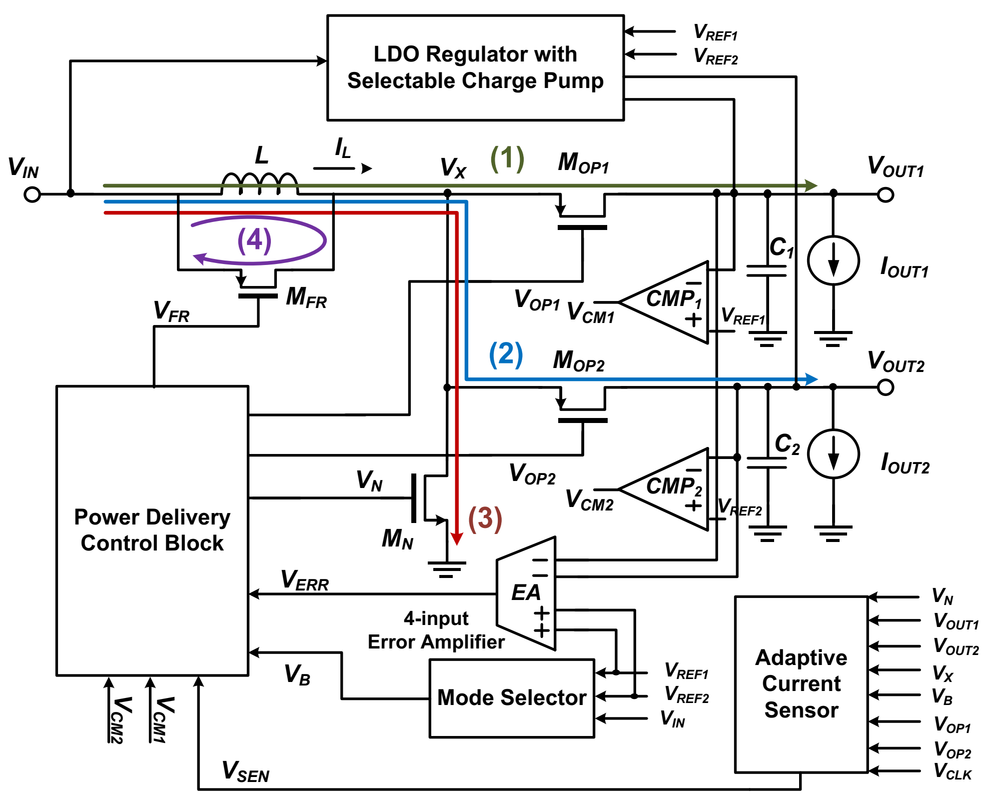

Fig. 1 Block diagram of the proposed SIDO converter

determine the amount of power to be delivered to the dual outputs so that V_{OUT1} and V_{OUT2} can be regulated to V_{REF1} and V_{REF2}, respectively. In addition, the LDO regulator with a selectable charge pump having a high bandwidth is implemented to improve the regulation characteristics of the proposed converter, while rapidly regulating the dual outputs by activating the charge pump for a step-up voltage, which will be explained in detail in Sect. 2.3.

Figure 2(a–c) respectively show the input voltage of the proposed converter, the timing diagram of the operation of switches (M_{OP1}, M_{OP2}, and M_N), and I_L in the buck–boost and boost modes.

When V_{IN} is between V_{REF1} and V_{REF2}, the proposed SIDO converter operates in the buck–boost mode, in which the I_L flows through paths (3), (1), and (2) in sequence, where the inductor is energized in paths (3) and (1), and de-energized in path (2). First, when M_{OP1} and M_{OP2} are turned off and M_N is turned on, I_L flows through path (3) and increases with a slope of V_{IN}/L. Second, when M_{OP2} and M_N are turned off, and M_{OP1} is turned on, I_L flows through path (1) and increases with a slope of $(V_{IN} - V_{OUT1})/L$. Last, when M_{OP1} and M_N are turned off, and M_{OP2} is turned on, I_L flows through path (2) and decreases with a slope of $(V_{IN} - V_{OUT2})/L$.

When V_{IN} is less than V_{REF1} and V_{REF2}, the proposed SIDO converter operates in the boost mode, in which I_L flows through paths (3), (1), and (2) in sequence, where the inductor is energized in path (3), and de-energized in paths (1) and (2). First, when M_{OP1} and M_{OP2} are turned off, and M_N is turned on, I_L flows through path (3) and increases with a slope of V_{IN}/L. Second, when M_{OP2} and M_N are turned off, and M_{OP1} is turned on, I_L flows through path (1) and decreases with a slope of $(V_{IN} - V_{OUT1})/L$. Last, when M_{OP1} and M_N are turned off, and M_{OP2} is turned on, I_L flows through (2) and decreases with a slope of $(V_{IN} - V_{OUT2})/L$. Thus, in the buck–boost and boost modes, the energizing and de-energizing periods are adjusted differently by controlling the flowing path of I_L using V_N, V_{OP1}, and V_{OP2}, and thereby V_{OUT1} and V_{OUT2} are regulated to V_{REF1} and V_{REF2}, respectively.

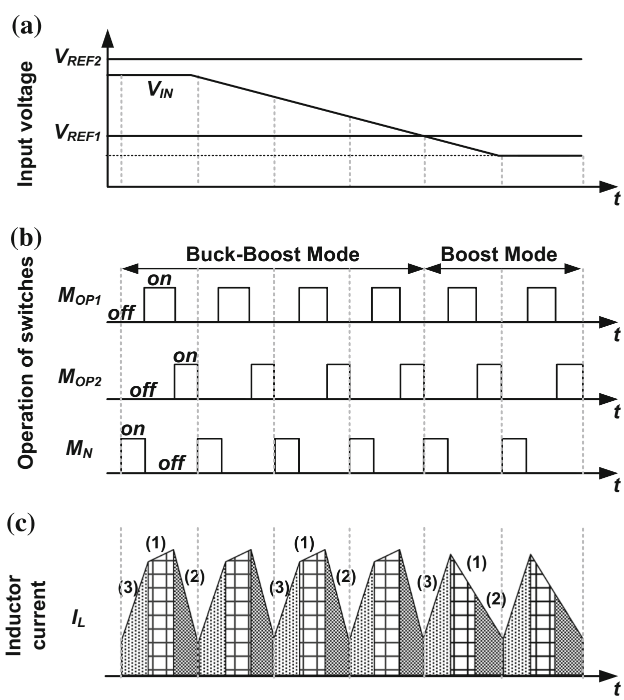

Fig. 2 **a** Input voltage of the proposed SIDO converter, **b** timing diagram of the switches (M_{OP1}, M_{OP2}, and M_N), and **c** inductor current (I_L) in the buck–boost and boost modes

2.2 Proposed adaptive current sensor

Figure 3(a) shows the schematic of the proposed adaptive current sensor, which consists of a current_sensor1, a current_sensor2, and a summing circuit.

In the current_sensor1, when I_L flows through path (3), the peak I_L is scaled down by 1/K, where K is the scaling ratio of the transistor size between M_N and M_{SC1}, and then flows through M_{SC1}. The scaled current (I_{SC1}) is mirrored to the currents of switches (M_{N1}–M_{N5}) (I_{SEN}) through OTA_1, where M_{N5} and OTA_1 are used to achieve a high current accuracy by minimizing the channel length modulation effect [15].

In the current_sensor2, when I_L flows through path (1) [or path (2)], the peak I_L is scaled down by 1/K, where K is the scaling ratio of the transistor size between M_{OP1} (or M_{OP2}) and M_{SC2} and then flows through M_{SC2} and M_{K1}. The scaled current (I_{SC2}) is mirrored to the currents of switches (M_{K1}–M_{K6}) (I_{SEN}) through OTA_2, where M_{K1} and OTA_2 are also used to achieve a high current accuracy. To have an accurate scaling ratio, K, the source-drain voltage of M_{SC2} is designed to be equal to that of M_{OP1} and M_{OP2}, assuming that M_{S1} and M_{S2} have a large size so that their resistance values can be ignored.

In the summing circuit, I_{SEN} is converted to the summing voltage (V_S) via the sensing resistor (R_{SEN}). However, when M_N and M_{OP1} (or M_{OP2}) are simultaneously turned on, glitches such as switching noise and voltage drop at V_S occur during the transition. Thus, to remove these glitches, a diode (D_1) and a capacitor (C_1) are used in the summing circuit, and M_{K7} periodically refreshes V_{SEN} using a reset signal (V_{CLK}) synchronized at the operating clock of the converter.

Since I_{SC1} and I_{SC2} of the current sensor should be regulated within a minimum on-time of V_N and V_{OP1} (or V_{OP2}), respectively, the required bandwidth of the current sensor should be greater than 1/[minimum on-time of V_N and V_{OP1} (or V_{OP2})]. The minimum on-time of V_N and V_{OP1} (or V_{OP2}) can be obtained by the product of the minimum

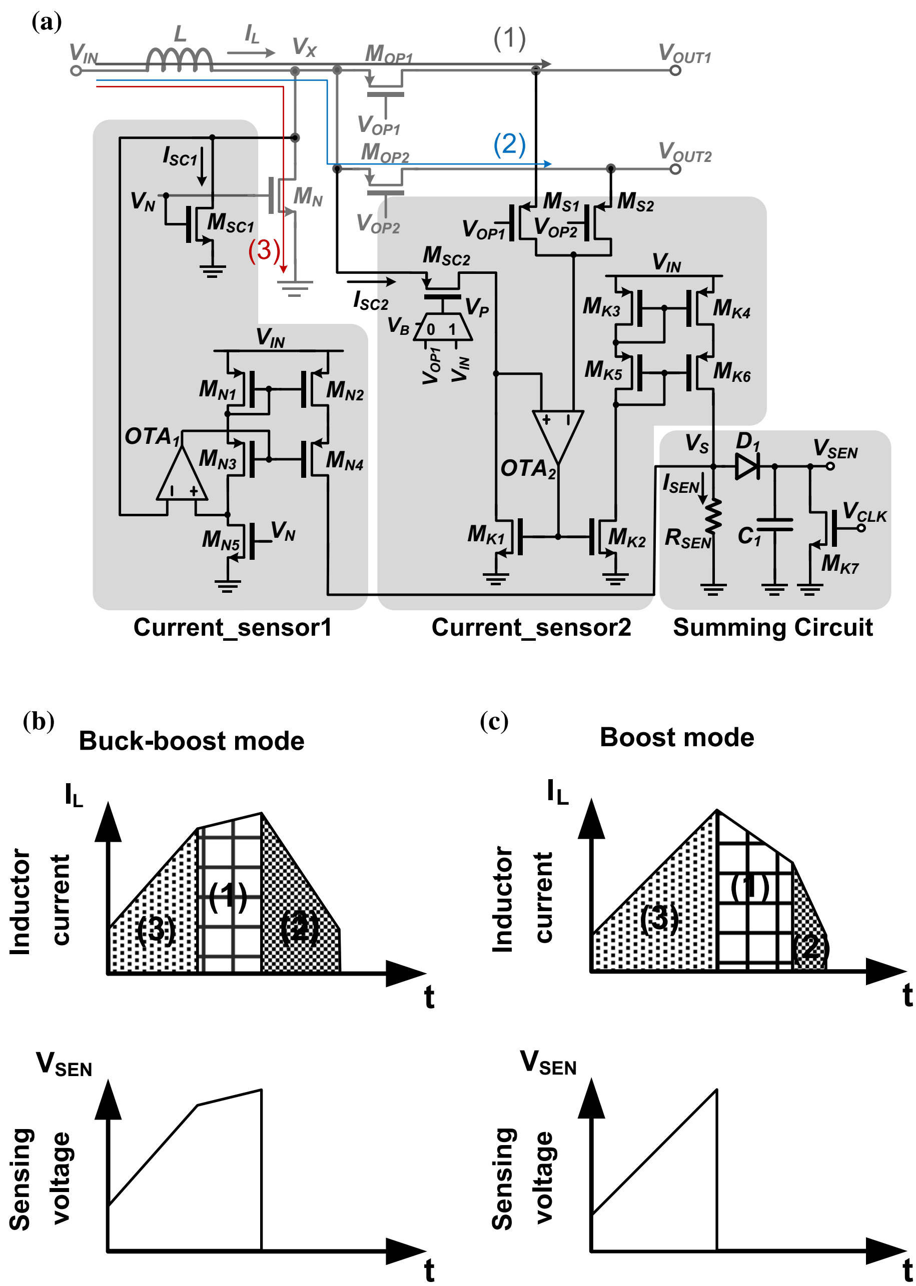

Fig. 3 **a** Schematic of the proposed adaptive current sensor, and timing diagrams of I_L and V_{SEN} and **b** in buck–boost mode and **c** in boost mode

on-duty of V_N and V_{OP1} (or V_{OP2}), and the operating period of the proposed converter, respectively [14]. In addition, the tolerable error of I_{SEN} can be determined according to an acceptable variation in V_{OUT}.

Figure 3(b, c) show the timing diagrams of I_L and V_{SEN} in the buck–boost and boost modes, respectively. In the buck–boost mode, the peak I_L in paths (3) and (1) is sequentially sensed by enabling both current_sensor1 and current_sensor2, and I_{SEN} is then converted to V_{SEN} through the summing circuit. In the boost mode, the peak I_L in path (3) is sensed by enabling current_sensor1 and disabling current sensor2, and I_{SEN} is converted to V_{SEN}. Therefore, the proposed adaptive current sensor accurately detects the peak I_L and generates V_{SEN}, which is used in the power delivery control block to improve the regulation characteristics.

2.3 LDO regulator with selectable charge pump

When the load current of the proposed SIDO converter abruptly changes, the LDO regulator is used to achieve a fast transient response by compensating for the insufficient inductor current of the switching converter because the bandwidth of the LDO regulator is greater than that of

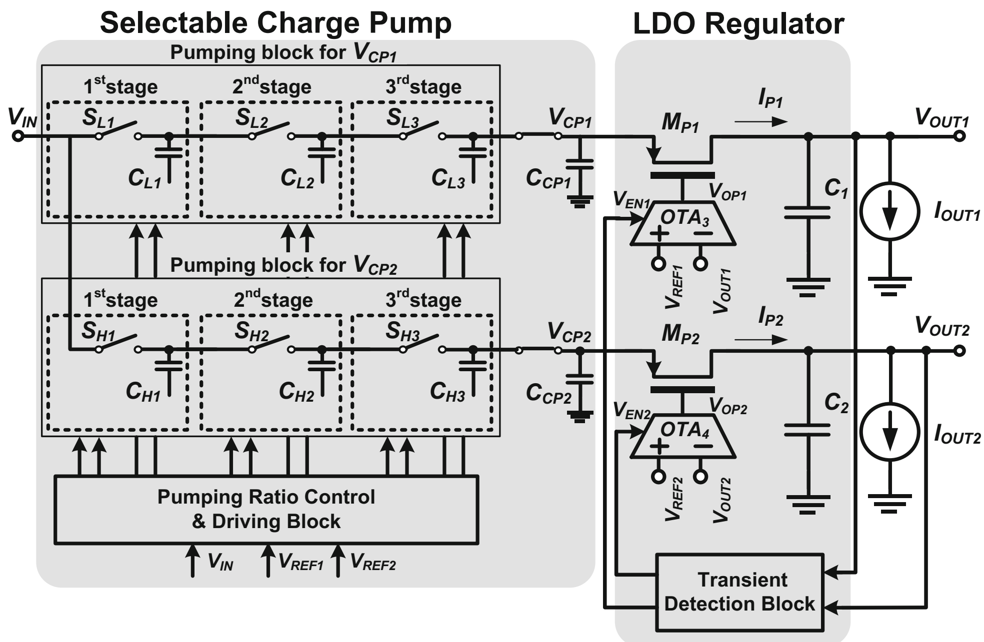

Fig. 4 Structure of the LDO regulator with a selectable charge pump

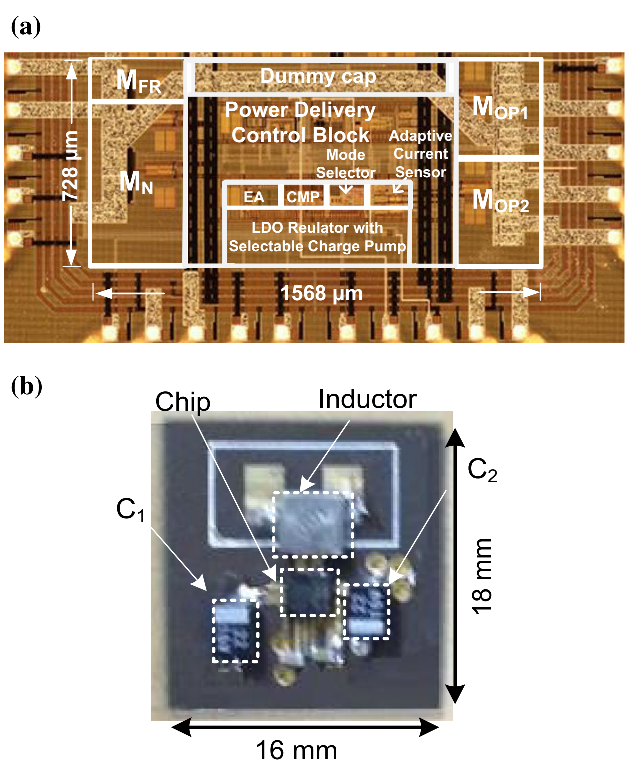

Fig. 5 **a** Chip microphotograph of the proposed SIDO converter and **b** photograph of the PCB

the switching converter [16–20]. The selectable charge pump, which is used to generate two step-up voltages of V_{CP1} and V_{CP2} according to the input and output voltages, always operates both in the steady state and in the load transient, whereas the LDO regulator only operates in the load transient. The LDO regulator with selectable charge pump is designed with smaller-sized power transistors compared with the switching converter [21, 22], thereby achieving low load- and cross-regulations without degrading power efficiency.

Figure 4 shows the structure of the LDO regulator with a selectable charge pump. The selectable charge pump consists of a pumping ratio control and driving block, and pumping blocks for V_{CP1} and V_{CP2}. Each pumping block has three stages, which are used to sufficiently pump up V_{CP1} and V_{CP2} to regulate V_{OUT1} and V_{OUT2}, respectively. The LDO regulator, which consists of two error amplifiers (OTA_3 and OTA_4), pass transistors (M_{P1} and M_{P2}), and a transient detection block, has a dropout voltage (V_{LDO}). In the selectable charge pump, a pumping ratio control and driving block determines the pumping ratios according to V_{IN}, V_{REF1}, and V_{REF2} by enabling or disabling each stage using the driving switches and capacitors. When a stage is enabled, its output voltage increases by V_{IN}, whereas when a stage is disabled, its output voltage remains at its input voltage.

When V_{IN} is greater than $V_{REF1} + V_{LDO}$, considering the dropout voltage of the LDO regulator, the proposed SIDO converter operates in the buck–boost mode. In this case, the selectable charge pump enables only one stage for V_{CP2} and disables the rest of the stages for V_{CP1} and V_{CP2}, and so V_{CP1} and V_{CP2} become V_{IN} and $2 \times V_{IN}$, resulting in being greater than $V_{REF1} + V_{LDO}$ and $V_{REF2} + V_{LDO}$, respectively. When V_{IN} is less than $V_{REF1} + V_{LDO}$, the proposed SIDO converter operates in the boost mode. In this case, the selectable charge pump enables one, two, or three stages among stages in the

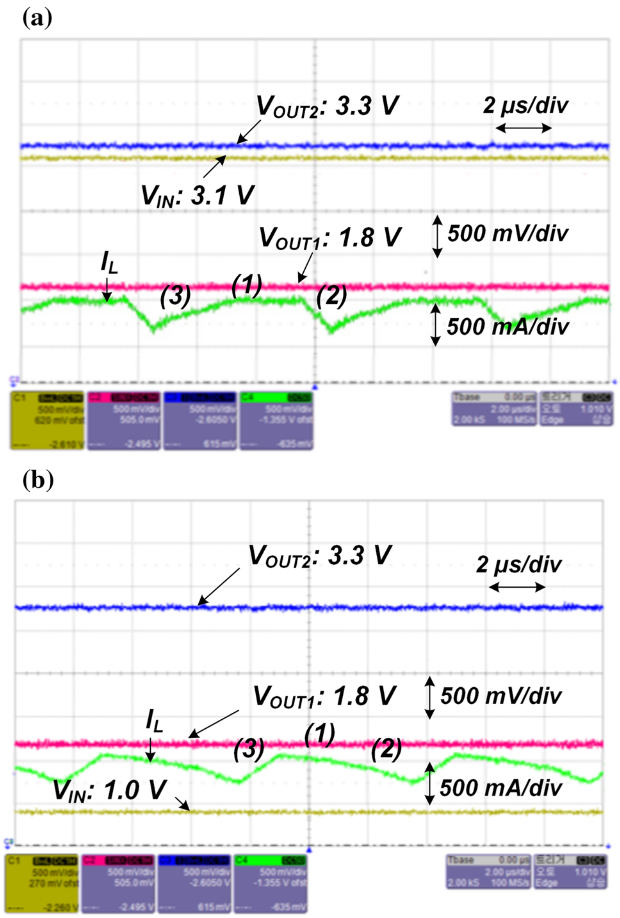

Fig. 6 Measured input/output voltages and I_L at $V_{OUT1} = 1.8$ V, $V_{OUT2} = 3.3$ V, $I_{OUT1} = 100$ mA, and $I_{OUT2} = 100$ mA **a** when $V_{IN} = 3.1$ V in the buck–boost mode and **b** when $V_{IN} = 1.0$ V in the boost mode

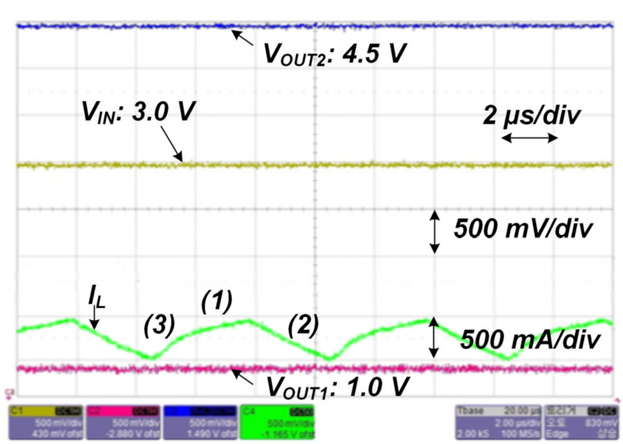

Fig. 7 Measured input/output voltages and I_L at $V_{OUT1} = 1.0$ V, $V_{OUT2} = 4.5$ V, $I_{OUT1} = 200$ mA, and $I_{OUT2} = 200$ mA when $V_{IN} = 3.0$ V in the buck–boost mode

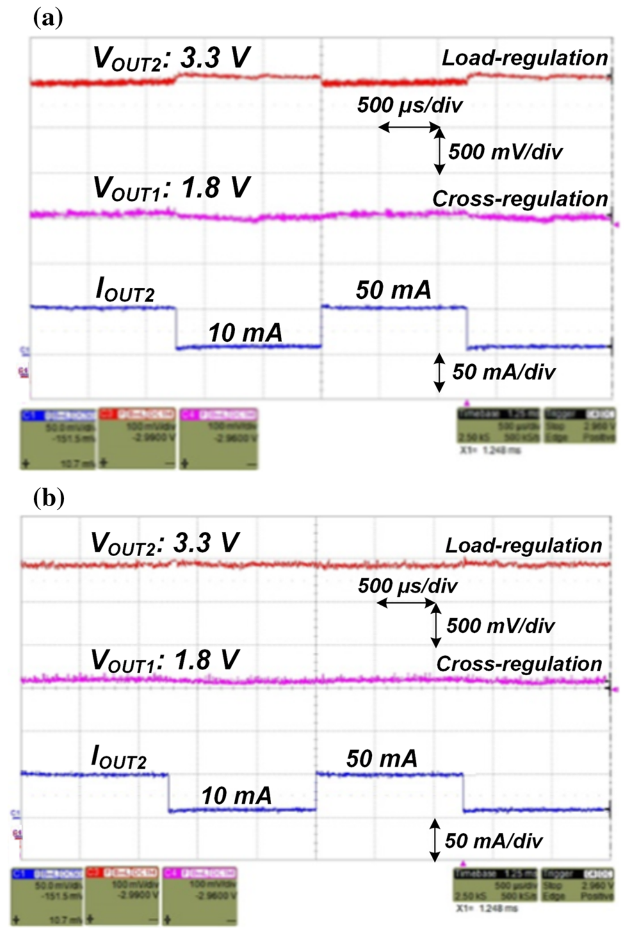

Fig. 8 Measured load-regulation of V_{OUT2} and cross-regulation of V_{OUT1} when I_{OUT2} is changed from 10 to 50 mA and vice versa **a** without and **b** with the LDO regulator and selectable charge pump

pumping blocks according to V_{IN}, V_{REF1}, and V_{REF2}, thereby generating 2×, 3×, or 4 × V_{IN}, respectively, for both V_{CP1} and V_{CP2}. Thus, V_{CP1} and V_{CP2} can be sufficiently pumped up to be greater than $V_{REF1} + V_{LDO}$ and $V_{REF2} + V_{LDO}$, respectively. The sizes of the pumping capacitors for V_{CP1} and V_{CP2} (C_{Ln} and C_{Hn}) are determined given that the supplied charge to the charge pump should be larger than or equal to the released charge from the charge pump. Furthermore, the sizes of the load capacitors for V_{CP1} and V_{CP2} (C_{CP1} and C_{CP2}) are determined by considering the output ripple voltage [23].

In the LDO regulator, the transient detection block detects the load transition at V_{OUT1} and V_{OUT2}, and enables OTA_3 and OTA_4 to convert V_{CP1} and V_{CP2} to V_{REF1} and V_{REF2} through M_{P1} and M_{P2}, respectively, with a voltage drop of V_{LDO}. Therefore, V_{OUT1} and V_{OUT2} can be rapidly regulated to V_{REF1} and V_{REF2}, respectively.

3 Experimental results

Figure 5(a) shows the chip microphotography of the proposed SIDO converter, which is fabricated using a 0.18-μm CMOS technology and occupies an area of 1142 mm^2

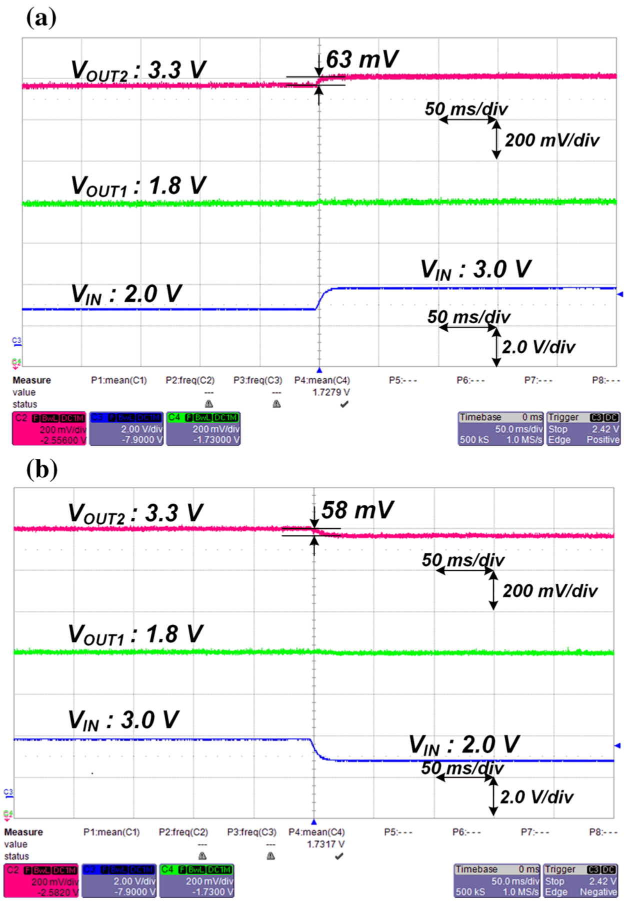

Fig. 9 Measured line-regulation of V_{OUT1} and V_{OUT2} when V_{IN} is changed **a** from 2.0 to 3.0 V and **b** from 3.0 to 2.0 V

(1568 μm × 728 μm). Figure 5(b) shows the photograph of the printed circuit board (PCB) with a module size of 18 mm × 16 mm, including the proposed chip, an inductor, and capacitors. To verify the performance of the proposed converter, an input voltage ranging between 3.2 and 1.0 V is used and two output voltages are designed to be 1.8 and 3.3 V with a maximum output current of 200 mA at an operating frequency of 500 kHz.

Figure 6 shows the measured input and output voltages, and I_L at $V_{OUT1} = 1.8$ V, $V_{OUT2} = 3.3$ V, $I_{OUT1} = 100$ mA, and $I_{OUT2} = 100$ mA: (a) when $V_{IN} = 3.1$ V in the buck–boost mode and (b) when $V_{IN} = 1.0$ V in the boost mode. Figure 7 shows that the dual output voltages can be regulated in an extended range of between 1.0 and 4.5 V.

Figure 8 shows the measured load-regulation of V_{OUT2} and cross-regulation of V_{OUT1} when I_{OUT2} changes from 10 to 50 mA and vice versa. Without the LDO regulator and selectable charge pump, the load- and cross-regulations are 0.375 and 0.264 mV/mA, respectively, as shown in Fig. 8(a). With the LDO regulator and selectable charge pump, the load- and cross-regulations are 0.120 and 0.088 mV/mA, respectively, as shown in Fig. 8(b), showing that the voltage fluctuation is not noticeable. When V_{IN} changes from 2.0 to 3.0 V and from 3.0 to 2.0 V as shown in Fig. 9(a, b), respectively, V_{OUT2} varies by less than 63 mV, and thereby the proposed converter has a line regulation of less than 0.063 mV/mV. On the other hand, V_{OUT1} varies unnoticeably. These measurement results demonstrate that the output voltages of the proposed SIDO converter are well regulated using the LDO regulator with selectable charge pump regardless of the changes in the load current and input voltage.

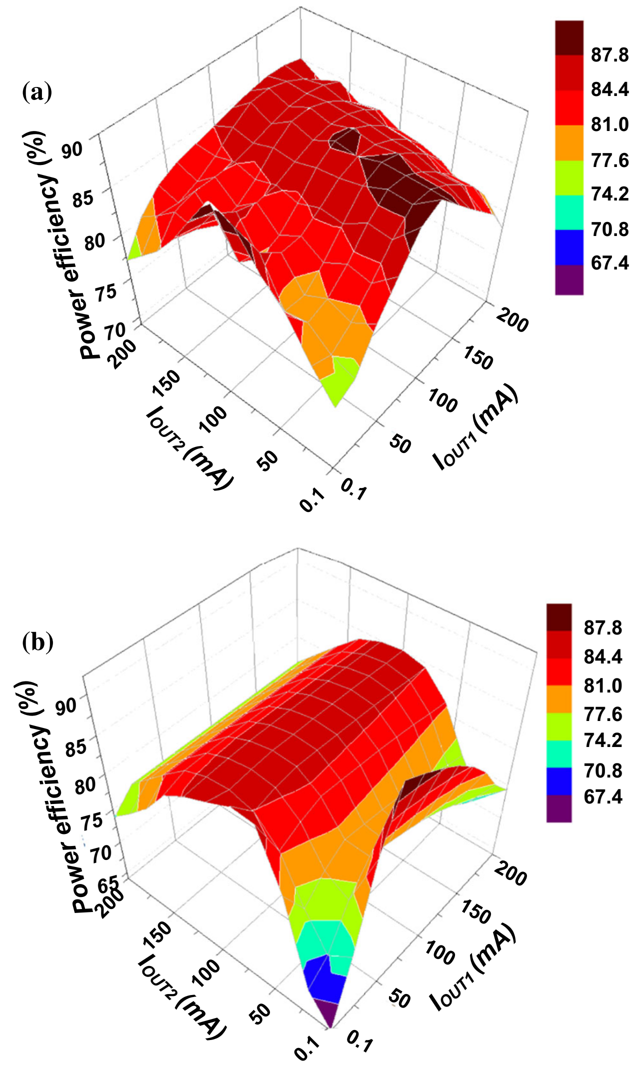

Fig. 10 Power efficiency according to the load currents at $V_{OUT1} = 1.8$ V and $V_{OUT2} = 3.3$ V **a** when $V_{IN} = 3.1$ V in buck–boost mode and **b** when $V_{IN} = 1.0$ V in boost mode

Figure 10(a, b) show the power efficiencies according to the load currents at $V_{OUT1} = 1.8$ V and $V_{OUT2} = 3.3$ V, where the maximum efficiencies are 89.2% in the buck–boost mode at the I_{OUT1} and I_{OUT2} of 100 mA, and 88.3% in the boost mode at a I_{OUT1} of 100 mA and a I_{OUT2} of 0 mA, respectively. Although the proposed converter

Table 1 Comparison and performance summary

Specification	[10]	[11]	[21]	This work
Technology	0.25-μm CMOS	0.18-μm CMOS	65-nm CMOS	0.18-μm CMOS
V_{IN} (V)	2.5–5.0	1.6–2.5	0.85–3.6	3.2–1.0
Area (mm^2)	7.540	1.690	3.000	1.142
Max. load current (mA)	364	170	10	400
Current density (mA/mm^2)[a]	48.27	100.59	3.33	350.00
Output voltage (V) of V_{OUT1}	1.8	2.1	1.2	1.8
Output voltage (V) of V_{OUT2}	5.0	2.8	1.0	3.3
Output voltage range (V)	1.8–5.0	2.1–2.8	0.1–1.9	1.0–4.5
Buck–boost type	Buck–boost	Buck–boost	Buck–boost	Buck–boost
Inductor (μH)	2.2	1.0	–	4.7
Output capacitor (μF)	40.0	66.0	1.0	9.4
Value of the LC product (μH × μF)	88.0	66.0	–	44.2
Switching frequency (MHz)	2.0	1.0	0.01	0.5
Load-regulation (mV/mA)	0.816	0.050–1.900	1.000	0.120
Cross-regulation (mV/mA)	0.240	–	–	0.088
Max. power efficiency (%)	90.0	–	95.8	89.2

[a] Current density = Ratio of maximum load current (mA) to chip area (mm^2)

achieves small-area and high current density, the maximum power efficiency was limited to 89.2% mainly due to the conduction and switching losses of power switches, having 5.490 and 4.476%, respectively.

Table 1 shows the performance summary of the proposed converter compared with prior works. The proposed SIDO converter achieves the low load- and cross-regulations of 0.120 and 0.088 mV/mA, respectively. Moreover, it has the highest current density of 350.00 mA/mm^2, which is represented as the ratio of the maximum load current to the chip area and the smallest value of the product of LC, compared with prior works.

4 Conclusions

In this paper, a SIDO converter that operates in the buck–boost and boost modes is proposed to generate stable output voltages and achieve low load- and cross-regulations. The proposed adaptive current sensor detecting the peak inductor current without glitches and an LDO regulator with a selectable charge pump are adopted to achieve low load- and cross-regulations. The proposed SIDO converter was fabricated using a 0.18-μm CMOS process technology and occupies an area of 1568 μm × 728 μm. The regulated dual output voltages are 1.8 and 3.3 V and can be extended to be between 1.0 and 4.5 V. The measured load- and cross-regulations of the proposed SIDO converter are reduced to 0.120 and 0.088 mV/mA when the load current changes from 10 to 50 mA. In addition, the proposed SIDO converter achieves a high current density and the smallest value for LC product compared with prior works. Therefore, the proposed SIDO converter is suitable for mobile devices, which require low load- and cross-regulations, a high current density, and a small form factor.

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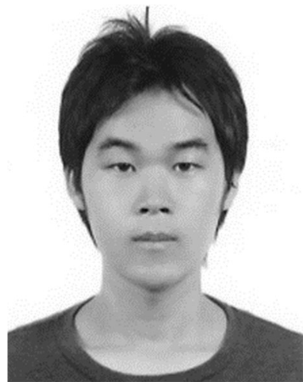

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