Analog Integr Circ Sig Process (2017) 91:491–495
DOI 10.1007/s10470-017-0957-8

MIXED SIGNAL LETTER

Ultra-low-power capacitor-splitting switching algorithm with minus energy for SAR ADCs

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Received: 23 October 2016 / Revised: 21 January 2017 / Accepted: 21 February 2017 / Published online: 20 March 2017

Abstract In this letter, an ultra-low-power capacitor-splitting switching algorithm for successive approximation register analog-to-digital converters is proposed. To achieve low power, the first three bit cycles consume no power from the reference by introducing minus energy during the third bit cycle and proper switching algorithm. To further reduce the switching energy, only single-side capacitors are switched from the forth bit cycle. Besides, to add one bit, the dummy capacitor is realized by four unit capacitors and switched to generate the least significant bit. Compared to the Sanyal and Sun switching technique, the proposed capacitor switching method achieves 94.19% energy saving and 47.66% capacitor area reduction.

Keywords SAR ADC · Switching algorithm · Ultra-low power · Minus energy · Capacitor-splitting

1 Introduction

Recently, the SAR ADC has been frequently used for biomedical applications due to its digital feature. The capacitor digital-to-analog converter (DAC) dissipates a large portion of the total power. Thus, many capacitor switching schemes [1–7] have been demonstrated for better power efficiency. Compared to the conventional switching scheme, the monotonic switching technique [1] achieves 81.26% less switching energy. The charge-average switching scheme [2] obtains 93.5% saving. The Sanyal and Sun [3], the Tong [4] and the Xie [5] switching schemes achieve low power by introducing the minus energy from the forth bit cycle, but they still consume much power during the third bit cycle. The bidirectional single-side (BBS) switching technique [6] generates the minus energy during the LSB cycle, but it is not energy efficient. The hybrid switching technique [7] dissipates no switching power during the first three bit cycles, and the Zhang switching scheme [8] introduces the minus energy during the second bit cycle. However, both are less energy efficient from the forth bit cycle because the monotonic switching method is used and double-side capacitors are switched. In this letter, an ultra-low-power capacitor-splitting switching algorithm with minus energy is proposed which consumes zero switching energy from the reference during the first three bit cycles and only single-side capacitors are switched from the forth bit cycle. The dummy capacitor is also reused to add one more bit, which further reduces switching energy. Therefore, compared to the Sanyal and Sun switching scheme, the proposed switching scheme reduces the switching energy by 94.19%.

2 Proposed capacitor-splitting switching scheme with minus energy

To reduce switching energy, several methods are often used, such as top-plating sampling, three voltage references, and making full use of the dummy capacitor [9]. But these techniques still consume much power from the voltage reference. The Sanyal and Sun scheme introduces the minus energy, which means that the DAC gives energy back to the reference voltage sources [3]. Thus, an ultra-low-power capacitor-splitting switching algorithm with minus energy was proposed. The capacitor-splitting

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method is to reduce the switching energy, because only single-side capacitors are switched from the third bit cycle.

To illustrate the proposed switching method, a 4-bit DAC is shown in Fig. 1. The $C/2$ is two Cs in series. First, top-plating sampling is conducted with bottom plates of the most significant bit (MSB) capacitors and the LSB capacitors reset to ground and V_{REF}, respectively. Then, the sampling switches are off and the first comparison is performed. The MSB is achieved, but no power is dissipated. If MSB = 1, the LSB capacitors on the V_{DACP} side are switched from V_{REF} to ground with other capacitors unchanged. Otherwise, the LSB capacitors on the V_{DACN} side are switched from V_{REF} to ground. Another comparison is performed, and the MSB-1 is obtained. It does not consume switching energy, too. From the third bit cycle, only single-side capacitors are switched, which is based on the MSB. If MSB = 1, only capacitors on the V_{DACN} side are changed. Otherwise, the same case occurs on the V_{DACP} side.

The switching detail of the third bit cycle is shown in Table 1. When the MSB and MSB-1 are the same, the MSB capacitors are switched from the ground to V_{CM}; when the MSB and MSB-1 are different, the LSB capacitors are switched from V_{REF} to V_{CM}. In this bit cycle, the minus energy is introduced, which is not non-physical. It means the capacitors discharge and give energy back to the reference voltage sources [3]. For an N-bit ADC, the switching energy during the third bit cycle is

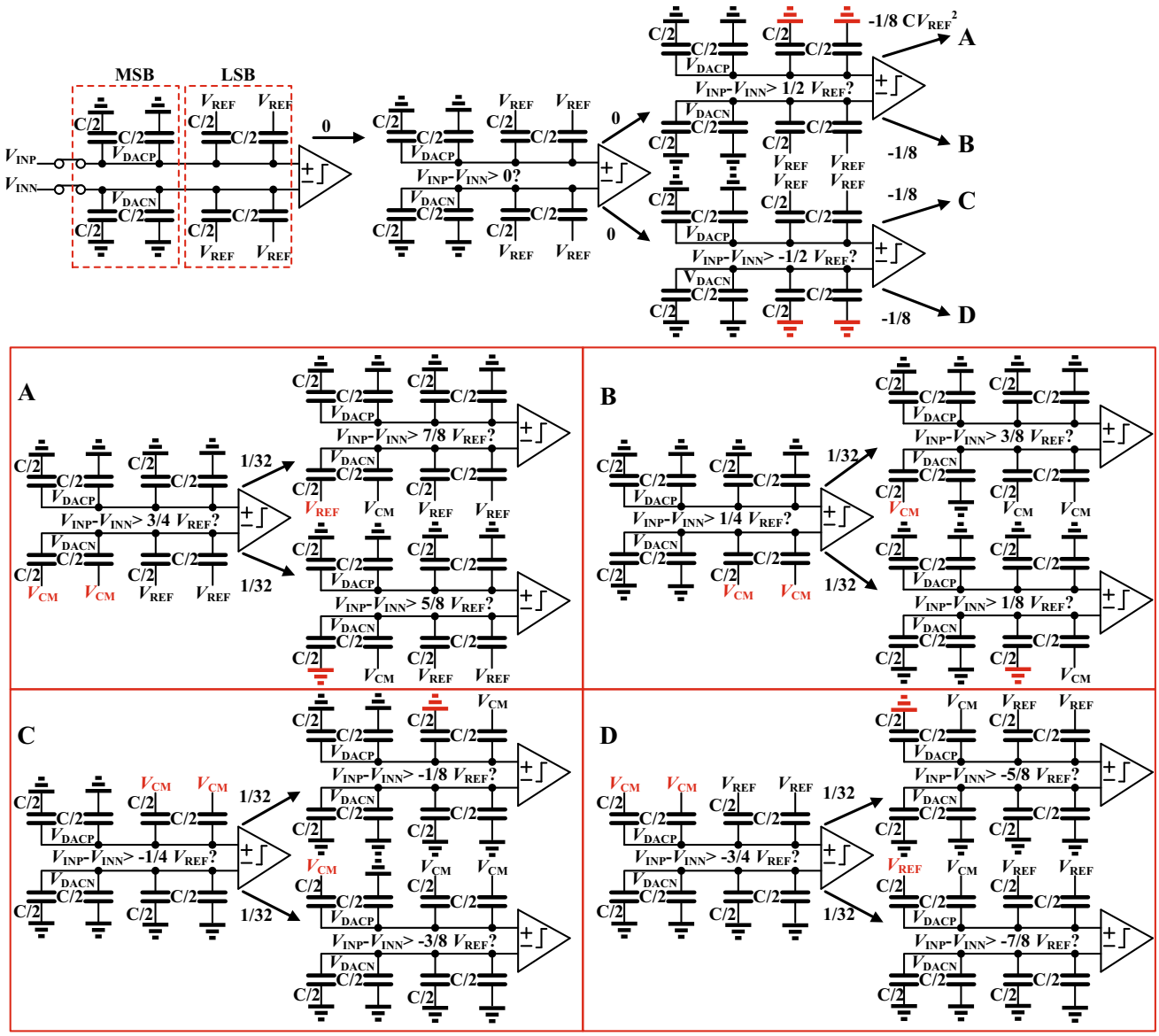

Fig. 1 Proposed switching scheme of 4-bit DAC

Table 1 Switching during the third bit cycle

	Switched capacitors during the third bit cycle
MSB = 1&&MSB-1 = 1	The MSB capacitors on the V_{DACN} side from ground to V_{CM}
MSB = 1&&MSB-1 = 0	The LSB capacitors on the V_{DACN} side from V_{REF} to V_{CM}
MSB = 0&&MSB-1 = 1	The LSB capacitors on the V_{DACP} side from V_{REF} to V_{CM}
MSB = 0&&MSB-1 = 0	The MSB capacitors on the V_{DACP} side from ground to V_{CM}

$$E_3 = -V_{CM}\cdot\left[\left(V_{DACP(N)}(2)+\frac{V_{REF}}{4}-V_{CM}\right)-\left(V_{DACP(N)}(2)-0\right)\right]\cdot 2^{N-4}C \quad -V_{REF}\cdot\left[\left(V_{DACP(N)}(2)+\frac{V_{REF}}{4}-V_{REF}\right)-\left(V_{DACP(N)}(2)-V_{REF}\right)\right]\cdot 2^{N-4}C = -2^{N-7}CV_{REF}^2 \tag{1}$$

or

$$E_3 = -V_{CM}\cdot\left[\left(V_{DACP(N)}(2)-\frac{V_{REF}}{4}-V_{CM}\right)-\left(V_{DACP(N)}(2)-V_{REF}\right)\right]\cdot 2^{N-4}C = -2^{N-7}CV_{REF}^2 \tag{2}$$

From the forth bit cycle, related capacitors are changed according to the first two bits, too. When the MSB and MSB-1 are the same, the related capacitor in the MSB part is switched from V_{CM} to ground or V_{REF} based on the third bit; when the MSB and MSB-1 are different, the related capacitor in the MSB part is switched from ground to V_{CM} or the related capacitor in the LSB part is switched from V_{CM} to ground, which is also based on the third bit. The former switching procedure is repeated until the LSB is achieved.

The output waveform of the proposed switching scheme is shown in Fig. 2(a). The related common-mode voltage is shown in Fig. 2(b) which affects the ADC linearity [10].

2.1 Switching energy

The behavioral simulations of different capacitor switching schemes and proposed capacitor-splitting switching scheme for 10-bit SAR ADC were performed in MATLAB. Figure 3 shows the average switching energy for these switching schemes against the output code. The proposed switching technique consumes only 9.24 CV_{REF}^2 average

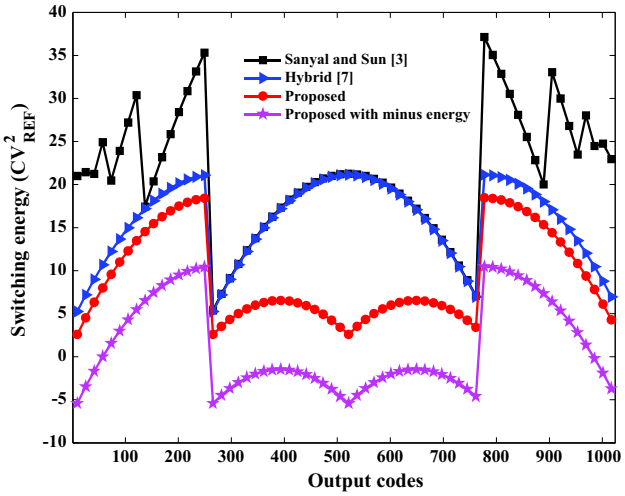

Fig. 3 Switching energy against output code

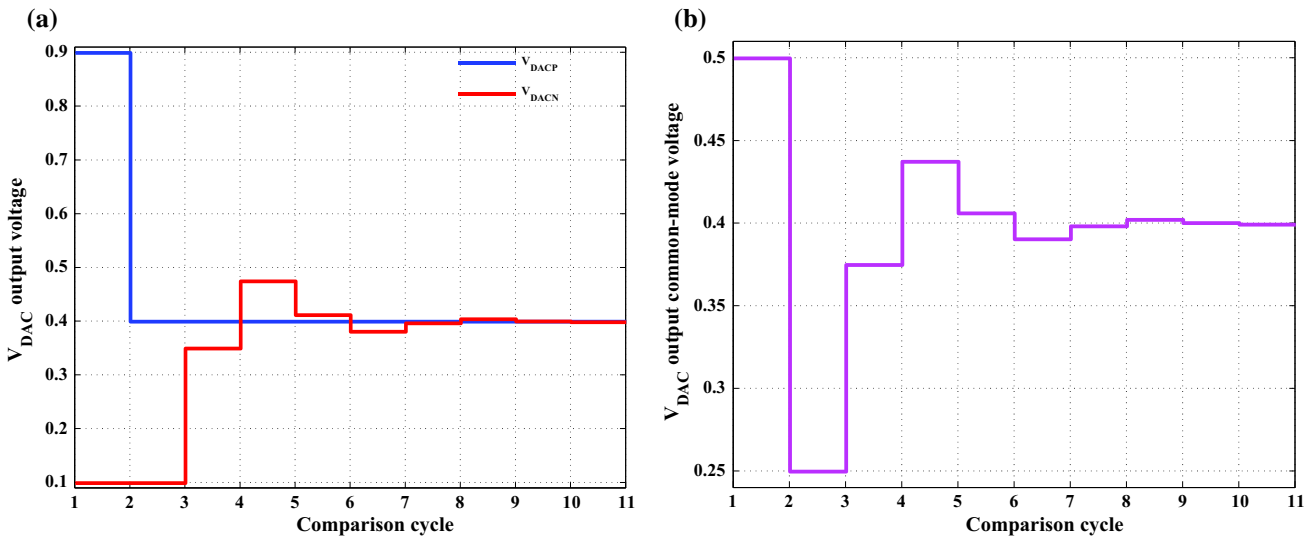

Fig. 2 Output waveform (**a**) and the related common-mode voltage (**b**) of the proposed switching scheme

Table 2 Comparison of different switching schemes for 10-bit SAR ADC

Switching schemes	Average switching energy (CV_{REF}^2)	Energy savings (%)	Number of required unit capacitors	Capacitor area reduction (%)
Sanyal and Sun [3]	21.33	Reference	512	Reference
Tong [4]	31.4	−47.21	256	50
BBS [6]	192	−800	512	0
Hybrid [7]	15.88	25.55	512	0
Zhang [8]	11.22	47.4	512	0
Proposed	9.24	56.68	268	47.66
Proposed with minus energy	1.24	94.19	268	47.66

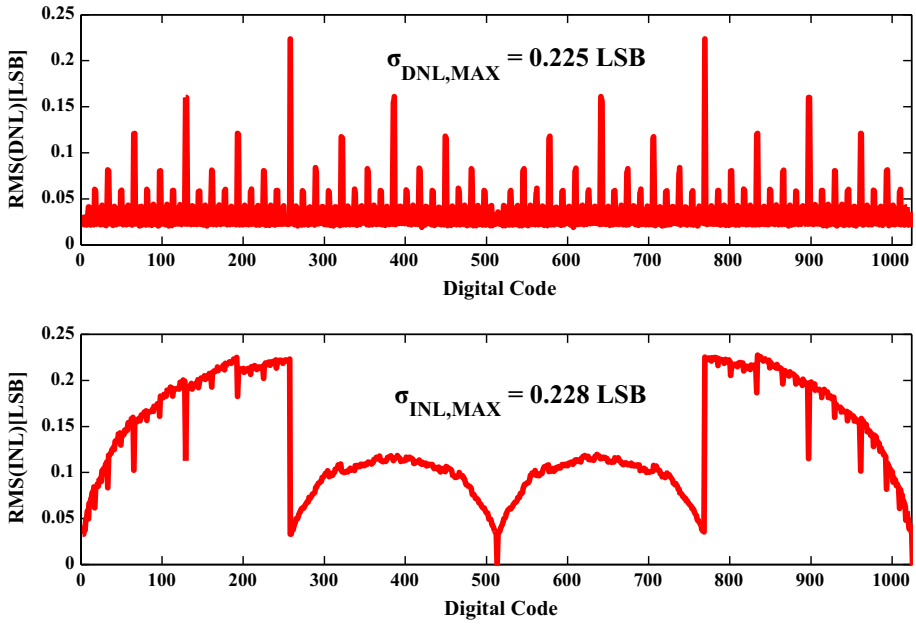

Fig. 4 Standard deviation of DNL and INL at each output code

switching energy from the reference and achieves 99.32% energy saving compared to the conventional switching. In Table 2, the comparisons for these switching methods are made and the Sanyal and Sun method [3] is chosen as a reference. The Tong [4], the hybrid [7], and the Zhang [8] switching techniques consume 31.4, 15.88, and 11.22 CV_{REF}^2 average switching energy, respectively. If the minus energy is considered, the switching energy is 1.24 CV_{REF}^2, 94.19% less. Besides, 268 unit capacitors are required, 47.66% less compared to the Sanyal and Sun technique. Therefore, the proposed approach is more area efficient and energy efficient.

2.2 Linearity

The switching energy is directly proportional to the value of the unit capacitor C. Thus, C should be as small as possible. However, the value of C is usually determined by the capacitor matching. Assume that the unit capacitor is Gaussian-distributed, modeled with a nominal value of C_u and a standard deviation of σ_u. For a binary-weighted capacitor array, each capacitor is unit capacitors in parallel. The parasitic effect of top-plate parasitic capacitance is ignored because it just leads to a gain error with no effect on the linearity performance. The bottom-plate parasitic capacitance of C in $C/2$ is also ignored for simplicity because it is little. Figure 4 shows behavioral simulation results of 512 Monte Carlo runs of 10-bit DAC with proposed switching scheme. The DNL and INL (integral nonlinearity) curves are the root-mean-square (rms) values, and C is Gaussian random variable with standard deviation of 1% ($\sigma_u/C_u = 0.01$). $\sigma_{DNL,MAX}$ and $\sigma_{INL,MAX}$ are 0.225 LSB and 0.228 LSB, respectively.

3 Conclusion

An ultra-low-power capacitor-splitting switching algorithm with minus energy and single-side capacitor switching for SAR ADCs is proposed. Compared to Sanyal and Sun

switching scheme, the proposed switching scheme achieves 94.19% energy saving and 47.66% capacitor area reduction. Thus, the proposed capacitor-splitting switching algorithm is often used for low-power and small-area SAR ADCs.

Acknowledgements This work was supported by the Scientific Research Foundation of Fujian University of Technology (GY-Z160057, GY-Z11002) and the Fujian Provincial Education Fund (JA06031).

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