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99.2% energy saving and high-linearity switching method for SAR ADCs

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Abstract A high energy saving and high linearity switching method of successive approximation register analogue-to-digital converters is presented. Based on the third reference voltage V_{cm} and split-MSB switching procedure, the proposed switching scheme achieves 99.2% less switching energy and 75% less number of capacitors over the conventional architecture. Moreover, the proposed scheme also achieves DNL and INL only 0.117LSB and 0.144LSB, respectively.

Keywords SAR ADC · Energy saving · High-linearity · Switching scheme · Split-MSB

1 Introduction

With the development of biological applications and wearable devices, low power analogue-to-digital converters become more popular while the successive approximation register (SAR) analogue-to-digital converter (ADC) is a good choice. In recent years, many studies have been carried on reducing the power of the SAR ADC [1–5]. Among them, the split-capacitor [1] achieves a 37% reduction over conventional SAR ADC. The monotonic switching technique [2] achieves an 81% energy reduction. And hybrid [3], mixed [4] achieve 98.4% and 99.4% energy saving, respectively. But we need to realize that many papers ignore the importance of linearity. The switching schemes [3, 4] do not present the linearity result. The technique of [5] presents switching energy and linearity at the same time while the energy saving is not enough. By using three voltage levels, the proposed scheme reduces energy consumption in the first three bit-cycles. Based on split-capacitor technique, the energy consumption and linearity are both further improved at the same time.

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2 Proposed low power and high linearity switching scheme

SAR ADC in the first few conversion cycles consumes bulk of the energy. Thus, the key to reducing switching energy in the capacitive DAC is to cut down the energy consumed in the first few conversion cycles. In order to reduce the switching energy further, the proposed scheme uses split-MSB capacitor, illustrating in the Fig. 1. Figure 1*a* and *b* illustrate the switching sequences on 3rd-MSB decision of the energy-back scheme and the proposed scheme. To explain the proposed scheme, a 4-bit differential SAR ADC is used, illustrating in the Fig. 2. Because of the switching scheme symmetrical, Fig. 2 just presents the switching scheme when MSB = 1. During the sampling phase, the differential input signal is sampled on the top-plates of both capacitor arrays, and the bottom-plates of capacitors are connected with [0.5…0.5 1.0.1], i.e. the bottom-plates of the most-significant bit (MSB) capacitor array are initially set to V_{cm}, and the bottom-plates of the other capacitors are set to V_{ref}. After that, the first comparison is performed and the sampling switches are turned off with no switching energy consumption. And the sequence of the higher voltage potential side of the capacitor array is set to [0…0 0.5…0.5] with no switching energy consuming. According to the second comparison result, the sequence is changed to

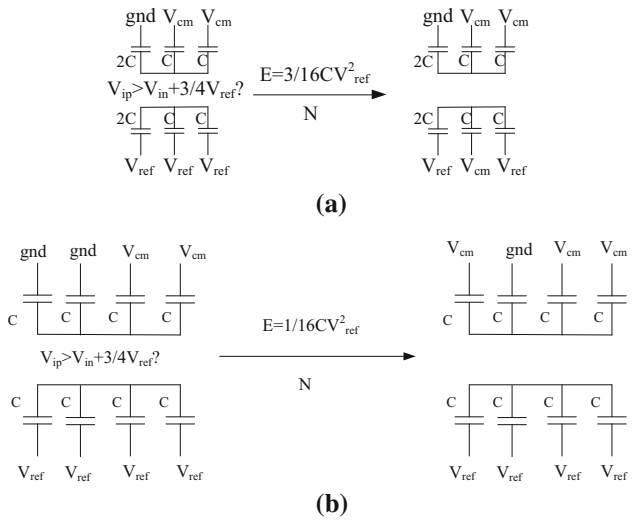


Fig. 1 Switch sequences on 3rd-MSB decision. **a** Energy-back switching scheme, **b** proposed switching scheme

[0.5…0.5 0.5…0.5] or [1…1 1…1]. This conversion consumes no energy as well. Thus, the proposed switching scheme achieves the first three comparison cycle no energy consumption.

The beginning of the 3rd-MSB to the least-significant bit (LSB) decision, the split-MSB capacitor array plays a very important role. In the rest of the comparison cycles, there is only one side of the DAC array change. The differential capacitor arrays will chose different reference voltages. For example, if 2nd-MSB = 1 and the i bit result is 1, the capacitor of main-DAC will change downward a V_{cm} voltage. If 2nd-MSB = 0 and the i bit result is 0, the capacitor of split-MSB will change upward a V_{cm} voltage.

As shown in Fig. 2, according to the comparator output, the main-DAC capacitor array or the split-MSB capacitor array is switched from V_{cm}/V_{ref} to gnd/V_{cm} or from gnd/V_{cm} to V_{cm}/V_{ref} while others remain unchanged. There is only one capacitor switch for each bit cycle, during the

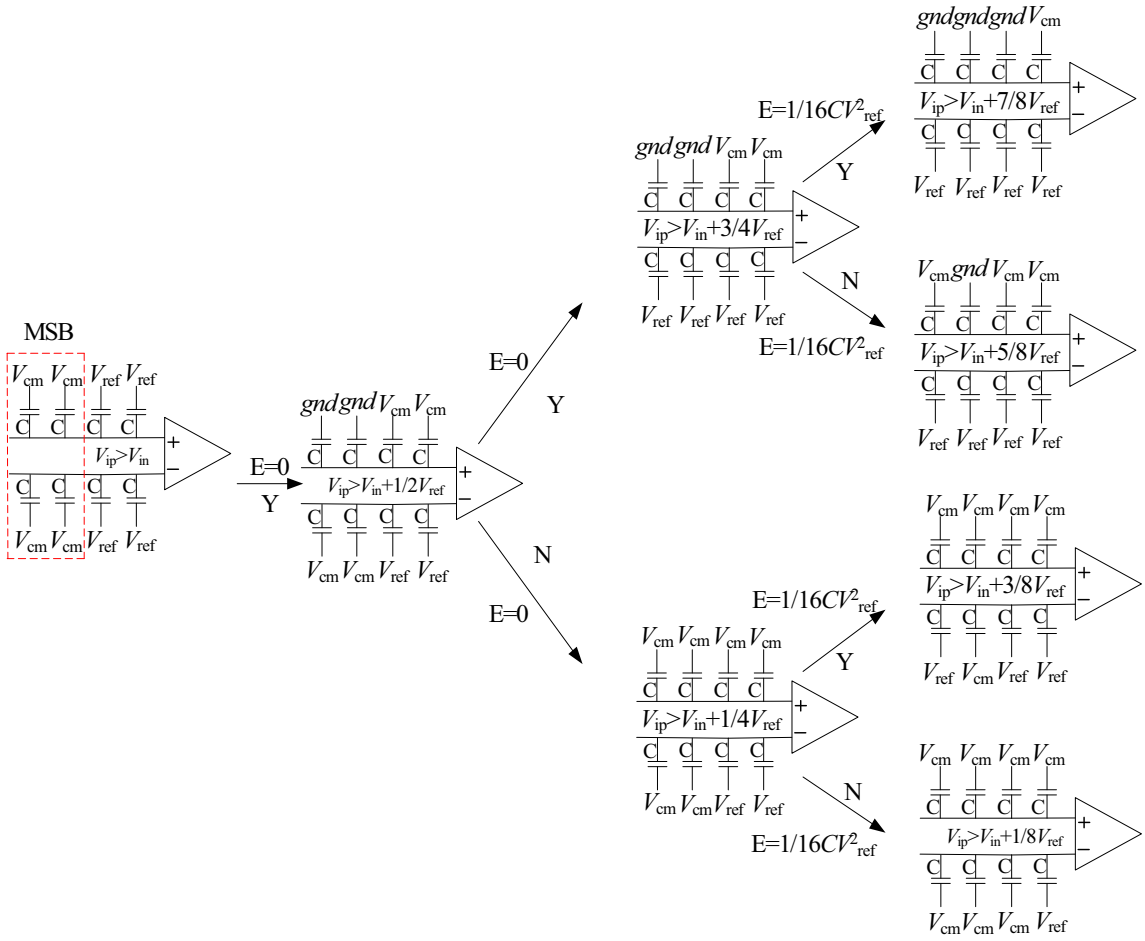


Fig. 2 The proposed switching scheme of 4 bit ADC

Table 1 Comparison of different switching schemes

Switching scheme	Average switching energy (CV^2_{ref})	Energy saving	Area reduction
Conventional	1363.33	0	0
Monotonic [2]	255.50	81.26%	50%
Hybrid [3]	15.88	98.83%	75%
Mixed [4]	7.94	99.4%	87.5%
This work	10.54	99.23%	75%

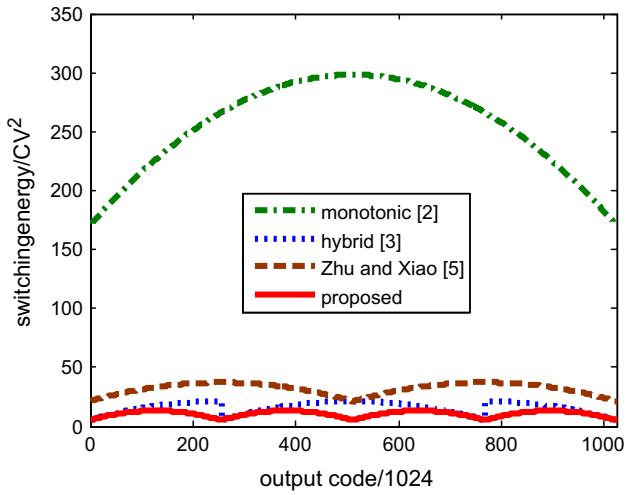


Fig. 3 Switching energy against output code

comparison cycles, so that less switching activity and lower energy.

3 Switching energy analysis

3.1 Switching energy

Behavioural simulation was performed in MATLAB for comparison of 10 bit SAR ADC. Table 1 summarises the features of previously reported switching schemes and the proposed switching scheme. The average switching energy for a 10 bit SAR ADC is $1363.3CV^2_{ref}$ whereas the switching energy for a 10 bit SAR using the proposed scheme is only 10.54 CV^2_{ref} which amounts to a reduction of 99.23% in the switching energy.

Figure 3 compares the switching energy of several different schemes and the proposed scheme. In the proposed switching scheme, the average switching energy for an N-bit SAR ADC is given below:

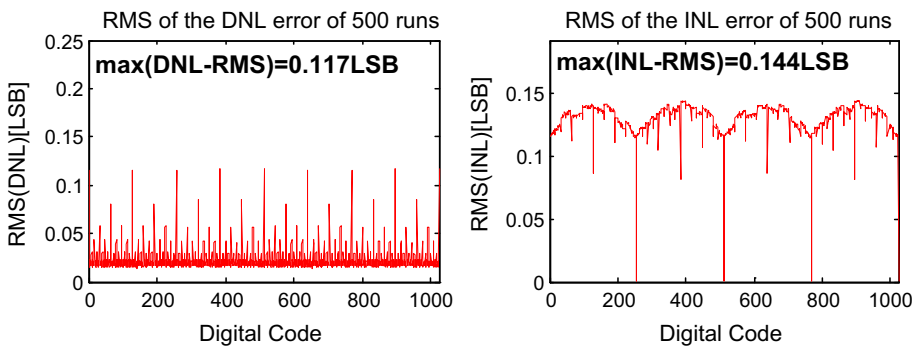
$$E_{avg} = \sum_{i=0}^{N-4} \frac{2^{N-3-i}-1}{2^{N-2i}} CV^2_{ref} \quad (1)$$

Parasitic capacitance affects the switching energy. The top-plate parasitic capacitance of the capacitor array increases the capacitor, thus increases the switching energy. When the capacitance is charging, the bottom-plate parasitic capacitance of the capacitor array needs charging thus it increases the switching energy. Otherwise the bottom-plate parasitic capacitance needs discharging but do not consume any additional energy from V_{ref}.

3.2 Linearity

The mixed switching scheme [4] achieves more than 99% energy saving over conventional switching scheme while ignores the linearity of the switching scheme. Figure 4 shows behavioural simulation results of 500 Monte Carlo runs of 10 bit SAR ADC with proposed switching scheme. Assuming the unit capacitor is modelled with a nominal value of C_u and a standard deviation of σ_u which is set to 1% ($\sigma(\Delta C/C = 0.01)$). The worst case DNL and INL occurs at $1/8V_{ref}$, $3/8V_{ref}$, $5/8V_{ref}$ and $7/8V_{ref}$. And the root-mean-square (RMS) of maximum DNL and the RMS of maximum INL are 0.117LSB and 0.144LSB, respectively.

Fig. 4 Simulation result with the proposed switching scheme



Based on the method provided in [5], the standard deviation of maximum DNL is given by:

$$\sigma_{DNL,MAX} = \frac{\sqrt{2 \times (2^{N-3} - 1)}}{C_u} \cdot \sigma_u \approx \frac{\sqrt{2^{N-2}}}{C_u} \cdot \sigma_u \qquad (2)$$

where $2 \times (2^{N-3} - 1)$ is the number of switched capacitors when the two code transitions occur. And the request of matching between unit capacitors can be smaller a factor of approximately 2 than that of the monotonic switching scheme.

4 Conclusion

A new energy-efficient switching scheme for SAR ADC is proposed. The proposed scheme achieves 99.23% energy saving over conventional switching scheme by using split-MSB technique and three reference voltages. In addition, the proposed switching scheme holds a high linearity that the DNL and INL are 0.117LSB and 0.144LSB, respectively. It is an ideal choice for low power SAR ADC.

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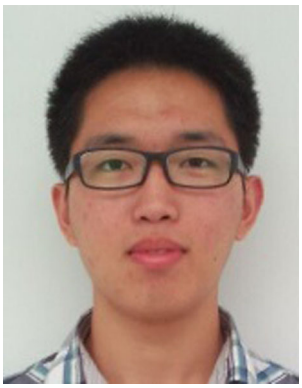

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