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MIXED SIGNAL LETTER

Energy-efficient switching scheme for ultra-low voltage SAR ADC

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Abstract An energy-efficient capacitor switching scheme for ultra-low voltage successive approximation register (SAR) analog-to-digital converter (ADC) is proposed. The novel switching scheme uses two reference levels, which eliminates the dependency on the accuracy of the extra reference voltage (V_{cm}). In addition, the proposed scheme combines merge-and-split (MS) switching method, floating switching method and LSB-down switching method. More switching energy is saved with switching energy optimization before the third comparison, and the number of capacitors in the capacitor array is also reduced by 75% due to LSB-down switching method. The proposed scheme achieves a 98.4% reduction in switching energy when compared with the conventional SAR architecture.

Keywords SAR ADC · Ultra-low voltage · Switching scheme · Floating capacitor · LSB-down

1 Introduction

Successive approximation register (SAR) analog-to-digital converters (ADCs) under ultra-low voltage supply are very popular in the design of wireless sensor network for portable, implantable, and wearable applications [1]. And the lowest reported supply voltage of ultra-low SAR ADC is 160 mV [2]. Capacitive digital-to-analog converters (CDACs) with charge redistribution technology [1–14] are widely used in SAR ADCs, which dominate the overall power consumption of SAR ADCs. In the past few years, many researchers have been devoted to reducing the power dissipation of CDACs [1–14]. Monotonic switching [4] and switching skip detection [5] methods using two reference levels have achieved considerable energy reductions. Moreover, switching methods using multiple reference levels can reduce more energy. So far, most of the researchers have focused on the switching methods with three reference levels. Compared with the conventional structure, V_{cm}-based switching [6], tri-level floating switching [9] and two-step switching [12] methods achieve 87.5, 99.6 and 99.75% reduction in switching energy, respectively. However, to realize the required extra reference voltage (V_{cm}) is arduous under ultra-low voltage supply. In addition, although the switching scheme using three reference levels can save much switching energy, the generation of V_{cm} may consume more static power. Hence, the switching methods using two reference levels are preferred and employed in ultra-low voltage SAR ADCs.

The main factor that limits the ultra-low voltage design of SAR ADC is the conventional analog design techniques suffer a lot of difficulties in terms of voltage headroom and dynamic range [2]. As a result, the researchers pay more attention to the ultra-low voltage design of the comparator, the sampling switch and the clock generator in SAR ADC [2], [13]. A novel subthreshold comparator and ultra-low-voltage analog switches are proposed in [2], where the supply voltage is from 160 to 300 mV. Moreover, an adaptive time optimized clock generator is proposed to reduce the total conversion time in [13], where the supply voltage is 400 mV. However, the capacitor switching scheme is almost independent on the supply voltage, provided that the analog circuits in SAR ADC is well-designed. Thus, the supply voltage of the proposed SAR architecture can also be from 160 to 400 mV. In addition, the proposed scheme simply needs two reference levels.

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In this Letter, an energy-efficient capacitor switching scheme is proposed for ultra-low voltage SAR ADC. Behavioral simulations show that the proposed scheme reduces the average switching energy by 98.4% over the conventional architecture and the dynamic common-mode voltage variation range of CDAC is only 0.5LSB.

2 Proposed SAR architecture

The architecture of the proposed 10-bit SAR ADC is illustrated in Fig. 1. In the fully differential architecture, except the unit capacitors and dummy capacitors, all capacitors are split into two equal capacitors. One is connected to V_{ref} and the other is connected to ground (GND) in the sampling phase. Additionally, the proposed 10-bit SAR ADC requires only 512 unit capacitors and two reference levels.

2.1 Proposed switching scheme

The proposed energy-efficient switching scheme is illustrated in Fig. 2, in which a 4-bit resolution is realized by a 2-bit capacitor array. And all capacitors in the two capacitor arrays are equal to the unit capacitor. During the sampling phase, V_{ip} and V_{in} are sampled to the top plates of the capacitor arrays. At the same time, the bottom plates of the positive-part capacitor array are set to '1 0 1 0' and the bottom plates of the negative-part capacitor array are set to '0 1 0 1', where '1' and '0' represent V_{ref} and GND, respectively. In the first bit cycle, the sampling switches turn off. The first comparison is performed directly and the first bit is obtained with no switching energy consumption. In the second bit cycle, if the first bit is 1, the capacitors that are connected to '1' in the positive side are merged with the ones that are connected to '0' in the negative side. And the voltage of the connected bottom plates is $0.5V_{ref}$, since the common-mode voltage of the DAC (V_{DAC_CM}) is $0.5V_{ref}$. As a result, V_P–V_N drops by half of V_{ref}. If the first bit is 0, $C_{1P,2}$, $C_{1N,2}$ C_{DP} and C_{DN} are merged instead and V_N–V_P drops by half of V_{ref}. Then the comparator gives the second bit result. In the third bit cycle, if the first bit is 1 and the second bit is 1, the bottom plate of $C_{1P,1}$ is switched to '0' and the bottom plate of $C_{1N,1}$ is switched to '1'. And V_P–V_N drops by $0.25V_{ref}$. Moreover, the similar operations are performed in other cases in this cycle, which are shown in Fig. 2(b). In the last bit cycle, LSB-down switching method [11] is performed. For example, if the third bit is 1 and the merged capacitors are C_{0P} and C_{0N}, the bottom plate of C_{0P} is connected to '0' and C_{0N} is floating [10]. As a result, V_P drops by 0.125Vref and V_N remains unchanged. V_{DAC_CM} is shifted by 0.0625Vref in this cycle.

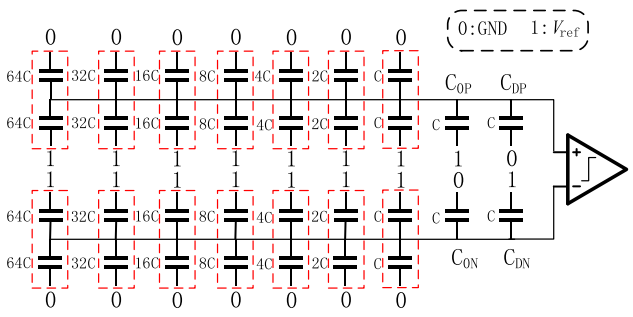


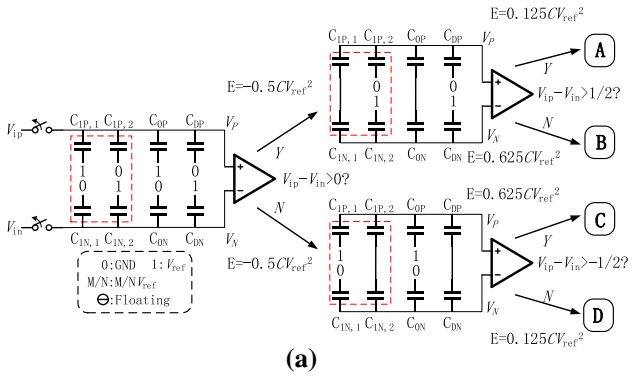
Fig. 1 The architecture of the proposed 10-bit SAR ADC

Since $0.5V_{ref}$ is generated without extra reference in the second cycle and utilized in the next bit cycles, the number of capacitors and the switching energy are significantly reduced for the proposed SAR ADC. It should be pointed out that negative energy is generated in the second bit cycle, which is not non-physical. It can be regarded as the energy that the DAC gives back to the reference voltage sources. And the proposed switching scheme directly accumulates it for comparison.

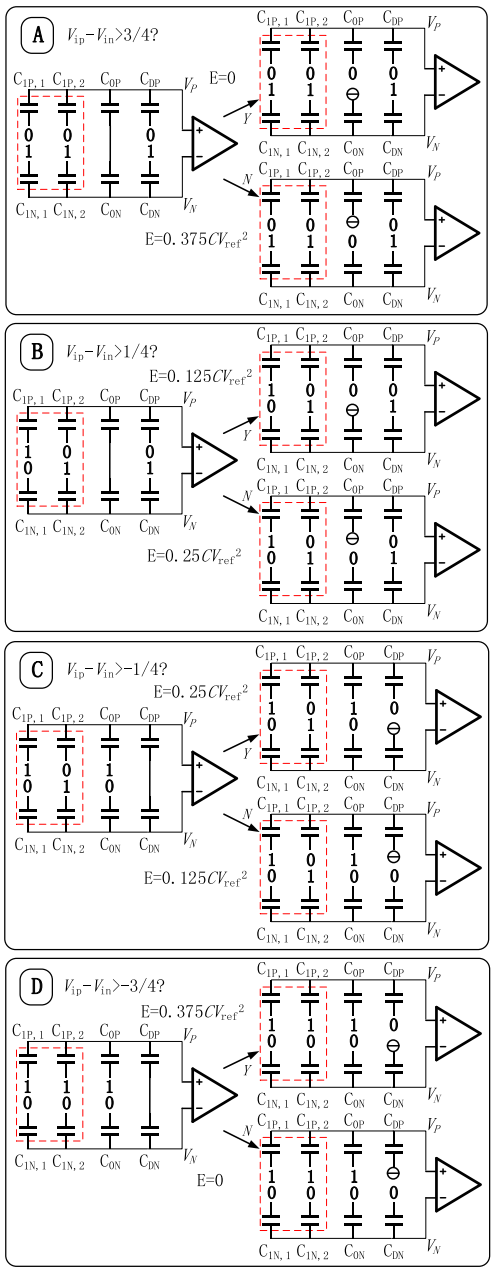
2.2 Common-mode voltage of DAC

In SAR ADC, the common-mode voltage of the DAC serves as the input common-mode voltage of the comparator, which determines the comparator's input-dependent dynamic offset. To achieve high performance of SAR ADC, the input common-mode variation is reduced as much as possible. The switching scheme proposed in [14] reduces the range of the common-mode voltage variation. The largest common-mode voltage variation is $0.25V_{ref}$, which is generated in the second bit cycle. Moreover, in the following comparison cycles, the common-mode voltage variation converges to a small value, which is within 0.5LSB. Hence, the scheme can relax the design requirements for the comparator. However, the scheme proposed in this letter is superior to the scheme in [14], since its largest common-mode voltage variation is only 0.5LSB, which is generated in the last bit cycle.

The comparator input waveform of a 5-bit SAR ADC in the proposed scheme is shown in Fig. 3. The comparator inputs have a constant common-mode voltage till the generation of the LSB, and the common-mode voltage variation is introduced at the inputs because of LSB-down operation. However, the magnitude of this variation is only 0.5LSB, which practically is negligible.



(a)



(b)

Fig. 2 **a** First two bit-cycles of the proposed switching scheme. **b** Last two bit-cycles of the proposed switching scheme

2.3 Switching energy

The behavioral simulations of the different switching schemes for a differential 10-bit SAR ADC were performed in MATLAB. And the results of switching energy against the output codes are illustrated in Fig. 4.

Table 1 compares the main features of different switching schemes. The proposed scheme consumes only 21.3C V_{ref}^2 average switching energy and achieves a 98.4% energy saving compared with the conventional scheme. Although the proposed scheme uses only two reference levels, it is more energy-efficient than the tri-level switching method used in [6–8].

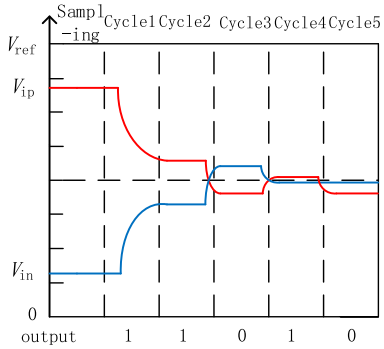


Fig. 3 Waveform of the proposed scheme when V_{in} is smaller than V_{ip}

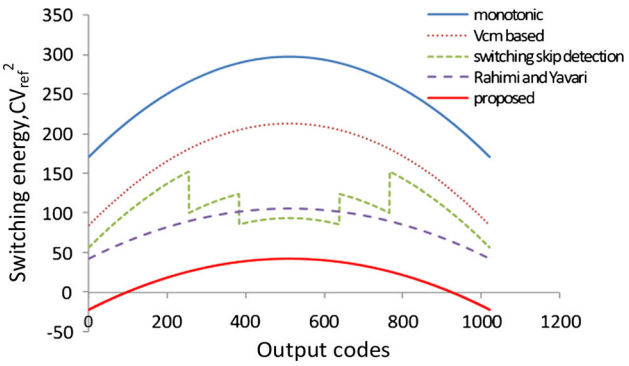


Fig. 4 Switching energy for 10 bit SAR ADC

Table 1 Comparison of switching techniques for 10-bit SAR ADC

Switching scheme	Area (C)	Average energy (CV_{ref}^2)	Extra reference voltage	V_{cm} of DAC variation
Conventional [3]	2048	1363.4	No	0
Monotonic [4]	1024	255.5	No	$0.5V_{ref}$
Switching Skip Detection [5]	1024	211.97	No	$0.25V_{ref}$
V_{cm}-based [6]	1024	170.2	Yes	0
Rahimi and Yavari [8]	512	84.9	Yes	0.5LSB
Zhu et al. [7]	512	31.9	Yes	$0.25V_{ref}$
Proposed	512	21.3	No	0.5LSB

3 Conclusion

A novel energy-efficiency capacitor switching scheme using two reference levels is proposed for ultra-low voltage SAR ADC. The behavioral simulations show that the proposed scheme achieves an energy saving of 98.4% compared with the conventional one. Fewer bit capacitors are needed at the same resolution because of LSB-down switching method. In addition, the proposed scheme introduces a small common-mode voltage variation at the comparator inputs, which relaxes the design requirements for the comparator.

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