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A computer-aided approach for voltage reference circuit design

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Abstract This work presents a computer-aided design (CAD) approach for voltage reference circuits by controlling main characteristics, such as temperature coefficient, power consumption, mismatch caused by the manufacturing process, transistor area and output noise. The CAD tool and the proposed methodology allow the designer to obtain accurate and optimum initial circuit sizing, thereby reducing the large number of computer runs usually required in voltage reference circuit designs. An illustrative example was carried out in a 180 nm CMOS process and verified by post layout simulations, whose results were in close agreement with the tool predictions, as shown in this paper. The reference circuit achieves an output voltage of 500 mV, a temperature coefficient of 15.19 ppm/°C over the temperature range of −40 °C to 100 °C, a maximum quiescent current of 5 μA, a power supply rejection ratio of −57 dB, and a line regulation of 0.250 % from 1.2 to 1.8 V supply voltage. The chip occupies an area of 0.072 mm^2.

Keywords CAD · Multi-threshold · Mutual-compensation · Voltage-reference

1 Introduction

A major challenge faced by integrated circuit (IC) designers is the choice of adequate design approach to achieve a specified circuit performance, while improving time-to-market. Usually, the limited time available for the design stage leads to a trial-and-error procedure, which requires a large number of simulations to ensure correct operation under manufacturing process variations. Therefore, area, power consumption, and other features are not always optimized. The development of CAD tools based on device models to help in the IC analog design [11, 8] allows efficient solutions by decreasing both number of simulations and design time.

This work presents a CAD tool for voltage reference circuit design by determining characteristics such as temperature coefficient (TC), power consumption, mismatch caused the manufacturing process, area, and output noise. One of the challenges in CAD tool development of voltage reference circuits is the device modeling along the temperature range of interest, to cover both industrial and commercial ranges. An additional difficulty is the compensation of manufacturing process effects, such as mismatch and process variations.

By using proper device models, it is possible to carry out symbolic simulations, and through a cost function determine initial sizing with optimized features. The design methodology advanced in this paper allows the designer to obtain initial sizing devices at a low computational cost and high accuracy. The primary contributions of this work are a CAD tool development and a novel design methodology, which, according to what has been found on the literature, reduces a gap in design techniques of voltage references.

This paper is organized as follows. Section 2 presents device models, circuit equations and proposed architecture for the voltage reference circuit. Section 3 describes the design methodology aided by the CAD tool. Section 4 assesses the circuit design and the CAD tool performances through electrical simulations and comparisons with other

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works reported in the recent literature. Concluding remarks are made in Sect. 5. Finally, in the appendix a temperature compensation technique is shown.

2 Voltage reference circuit

In most system-on-chip applications a voltage reference circuit that is insensitive to temperature, supply and process variations, among other effects, is needed. A voltage reference circuit can be implemented by taking advantages of the temperature behavior of bipolar transistors, MOS transistors, and diodes [8]. Two topologies are commonly employed to achieve a voltage-independent-of-absolute-temperature (V_{IOAT}) performance: one obtained through a pro-por-tio-nal-to-ab-so-lute–tem-pe-ra-ture (PTAT) behavior plus com-ple-men-ta-ry-to-ab-so-lute-tem-pe-ra-ture (CTAT) behavior [9], and other obtained by subtracting a CTAT curve from a CTAT one [16].

A low cost technique capable of producing a near to zero TC without using curvature compensation circuitry can be derived by using topologies based on the subtraction between two voltages that have similar temperature behaviors, such as the so-called CTAT-CTAT in Fig. 1. Usually these topologies are implemented in non-standard CMOS processes, such as channel implant [16] and different gate components [14] to obtain two threshold voltages that have similar temperature dependencies and close offset voltages. In [17] a CTAT-CTAT mutual compensation was implemented, on a standard CMOS process, by subtracting the difference between p-type and n-type threshold voltages.

The design steps of a CTAT-CTAT voltage reference circuit in standard 180 nm CMOS process is presented next, and can be straightforwardly adapted to other technology nodes.

2.1 Devices models

In CAD tool design, as well as in theoretical analysis, proper models must be chosen for the devices. The proposed voltage reference exploits the multi-threshold MOS transistor characteristics to achieve the mutual compensation, and hence the UICM model [13] is one alternative for transistor modeling, since it allows analysis of MOS transistors at all inversion levels. The UICM equation that is adequate to all inversion levels, when transistor operates in saturation, is given by

$$V_P - V_{SB} = U_T \cdot F(i_f) \tag{1}$$

where

$$F(i_f) = \sqrt{1 + i_f} + \log\left(\sqrt{1 + i_f} - 1\right) - 2 \tag{2}$$

$$V_P = \frac{V_{GB} - V_{To}}{n} \tag{3}$$

$$i_f = \frac{I_D}{I_S} \tag{4}$$

$$I_S = \frac{1}{2} n K' \frac{W}{L} U_T^2 \tag{5}$$

where V_{SB} and V_{GB} are the source-to-bulk and gate-to-bulk voltages, respectively, I_D is the drain current, U_T is the thermal voltage, whereas i_f, n, V_{To}, K' and W / L are, respectively, the inversion level (or forward current), slope factor, threshold voltage, gain factor and aspect ratio of the transistor. The technology dependence parameters n, V_{To} and K' should be extracted from simulations, at fixed temperatures, as proposed in [4]. In order to model their temperature behavior we propose the use of second-order polynomials, which are the result of fitting the parameters at adequate points within the temperature range of interest. Table 1 shows the results of the polynomial fitting, and Fig. 2 presents their behavior along the temperature range.

2.2 Proposed architecture

To produce a CTAT current, it is usual to convert a voltage into a CTAT current by using a CTAT generator [5]. The structure proposed in this paper is depicted in Fig. 3, and its main idea is to copy the voltage V_{G4} to V_R, such that the current through M_4 is N-fold lower than that through R. Therefore, the CTAT generator equation is given by

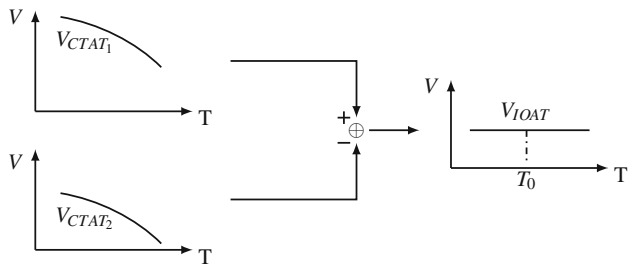

Fig. 1 Illustrative diagram of the CTAT-CTAT technique

Table 1 Second-order polynomial fitting ($p_2T^2 + p_1T + p_0$) for the UICM parameters (T in Kelvin)

MOS	Parameter	p_2	p_1	p_0
	n_n	3.37e−7	−2.51e−5	1.215
n-type	V_{Ton}	−1.02e−6	5.11e−5	408.5e−3
	K'_n	4.39e−9	−4.14e−6	113.5e−5
	n_p	4.40e−7	−6.11e−5	1.276
p-type	V_{Top}	−1.12e−6	−1.35e−5	479.8e−3
	K'_p	3.72e−10	−3.93e−7	141.8e−6

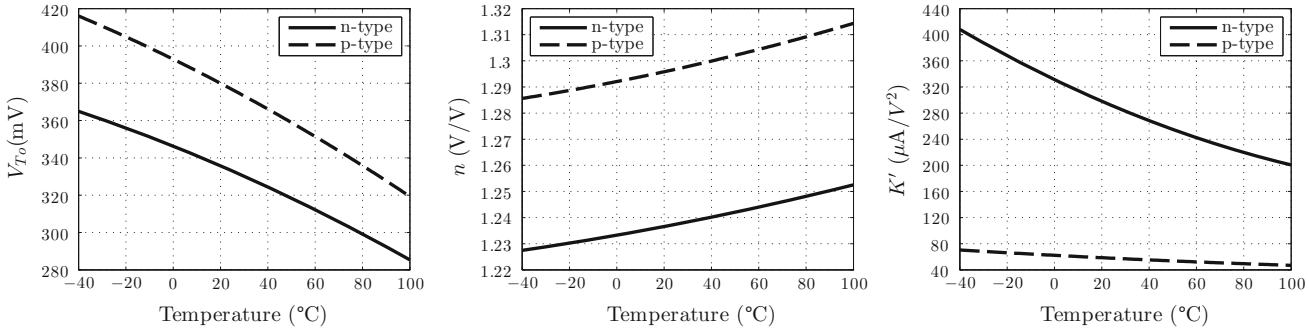

Fig. 2 Temperature behavior of the extracted second-order polynomials for the UICM parameters: **a** threshold voltage; **b** slope factor; **c** gain factor

$$V_R = R \cdot NI_{CTAT} \approx V_{G4} = V_{Ton} + n_n U_T \cdot F(i_{f4}) \tag{6}$$

where $F(i_{f4})$ is a function of the inversion level of M_4 (i_{f4}), as shown in Eq. (2). The required ratio of the transistor M_4, given a fixed inversion level at room temperature, is derived as

$$\frac{W_4}{L_4} = \frac{I_{CTAT}}{\frac{1}{2} n_n U_T^2 K_n' i_{f4}} = \frac{2}{NR} \frac{V_{Ton} + n_n U_T \cdot F(i_{f4})}{n_n U_T^2 K_n' i_{f4}} \tag{7}$$

Hence, the inversion level of M_4 can be used to adjust the temperature influence on the CTAT generator. Similar approach was presented in [12]. This behavior along the temperature for a 180 nm CMOS process is displayed in Fig. 4. The condition

$$N \cdot R > \frac{1}{g_{m4}} \tag{8}$$

must be ensured to provide a stable negative feedback, where g_{m4} is the transconductance of transistor M_4. The capacitance C_L is chosen such that an adequate loop phase margin is obtained.

Using two CTAT generator circuits, as indicated in Fig. 5, where each circuit operates at different inversion levels, the mutual compensation can be achieved. As a result, the voltage output V_{IOAT} is given by

$$V_{IOAT}(T) = K_2 \cdot V_{G4,2}(T, i_{f4,2}) - K_1 \cdot V_{G4,1}(T, i_{f4,1}) \tag{9}$$

where

$$K_1 = \alpha_1 \cdot \frac{R_3}{N_1.R_1} = \frac{\alpha_{11}\alpha_{13}}{\alpha_{12}} \cdot \frac{R_3}{N_1.R_1} \tag{10}$$

$$K_2 = \alpha_2 \cdot \frac{R_3}{N_2.R_2} \tag{11}$$

and α_{11}, α_{12}, α_{13}, α_2, N_1, N_2 are current mirror factors of the circuit shown in Fig. 5. The condition for mutual compensation can be found by assuming that V_{IOAT} does not change with temperature, and differentiating both sides of Eq. (9), which yields

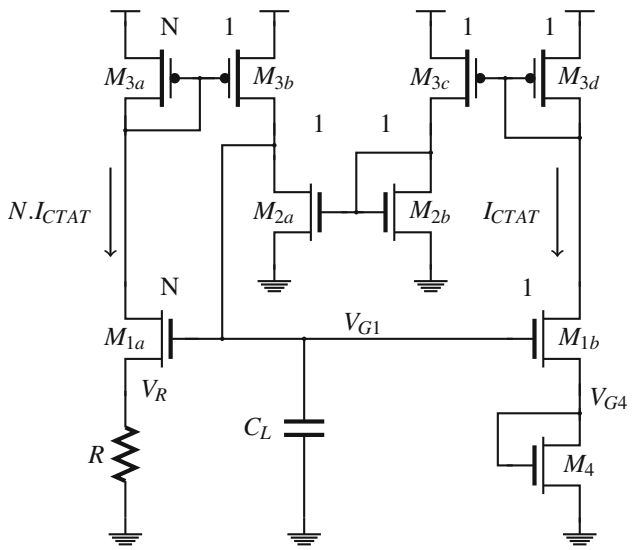

Fig. 3 Schematic diagram of the CTAT generator circuit

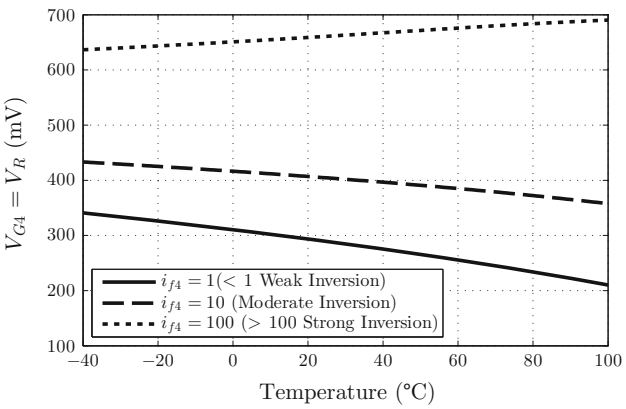

Fig. 4 Temperature influence on the CTAT generator at each inversion level of M_4 (i_{f4} defined at T = 40 °C)

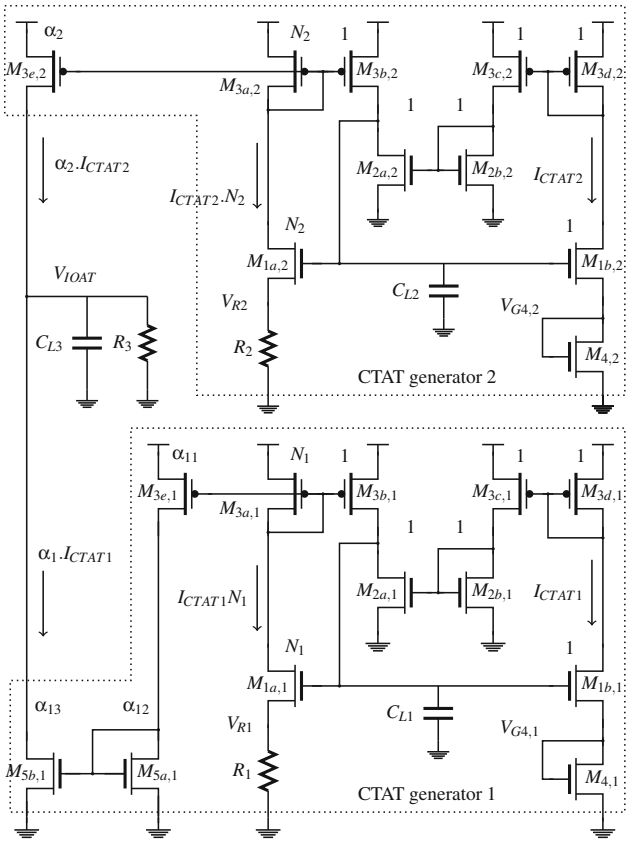

Fig. 5 Schematic diagram of the voltage reference circuit

$$\frac{\partial V_{G4,2}(T, i_{f4,2})}{\partial T} \cdot K_2 - \frac{\partial V_{G4,1}(T, i_{f4,1})}{\partial T} \cdot K_1 = 0, \tag{12}$$

which can be written as

$$\frac{\partial V_{G4,1}(T_o, i_{f4,1})}{\partial T} \Big/ \frac{\partial V_{G4,2}(T_o, i_{f4,2})}{\partial T} = \frac{K_2}{K_1} \tag{13}$$

The detailed derivations of the parameters K_1, K_2 and the inversion levels $i_{f4,1}$ and $i_{f4,2}$ needed to achieve the mutual compensation are presented in the Appendix.

2.3 Mismatch analysis

In [6, 7] expressions for MOS transistor mismatch variations at all inversion levels was proposed. A similar development can be used to obtain the variance of the normalized voltage V_R of the CTAT generator, that is,

$$\sigma^2\left(\frac{\Delta V_R}{V_R}\right) = \frac{1}{W_1 L_1}\frac{N+1}{N}\left[A^2_{V_{To}} + \frac{A^2_{K'}}{(g_{m1}/I_{D1})^2}\right] + \frac{1}{W_4 L_4}\left[A^2_{V_{To}} + \frac{A^2_{K'}}{(g_{m4}/I_{D4})^2}\right] \tag{14}$$

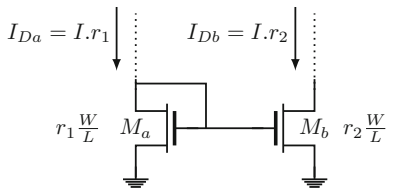

Fig. 6 Schematic diagram of a simple current mirror (see Eq. (17))

where $A_{K'}$ and $A_{V_{To}}$ are technology dependent parameters that model a normal distribution having zero mean and variances given by, respectively,

$$\sigma^2(\Delta V_{To}) = \frac{A^2_{V_{To}}}{WL} \tag{15}$$

$$\left(\frac{\sigma(\Delta K')}{K'}\right)^2 = \frac{A^2_{K'}}{WL} \tag{16}$$

Thus, the variance of the normalized output current of the current mirror circuit depicted in Fig. 6, assumes the form

$$\sigma^2\left(\frac{\Delta I_{Db}}{I_{Db}}\right) = \frac{r_1 + r_2}{r_1 r_2}\frac{1}{WL}\left[A^2_{K'} + (g_{mb}/I_{Db})^2 A^2_{V_{To}}\right] \tag{17}$$

where r_1 and r_2 are the numbers of transistors connected in parallel to implement M_a and M_b, respectively.

Moreover, the Eqs. (14) and (17) can be expressed as a function of the inversion levels by using

$$g_{m\ell}/I_{D\ell} = \frac{2}{nU_T\left(\sqrt{i_{f\ell}+1}+1\right)} \tag{18}$$

where $g_{m\ell}$, $i_{f\ell}$ and $I_{D\ell}$ denote the transconductance, inversion level and drain current of transistor M_ℓ, respectively.

2.4 Noise analysis

The impact of thermal and flicker noises on the voltage reference performance was addressed in this work. The power spectral density (PSD) of the thermal noise current at the output can be approximated by the contributions of the transistors that are not in closed loop, yielding

$$S_{I_{TN}} \approx Si_{3e,2} + (Si_{3e,1} + Si_{5a,1})\frac{\alpha^2_{13}}{\alpha^2_{12}} + Si_{5b,1} + Sv_{R_3}\frac{1}{R_3^2} \tag{19}$$

where

$$Si_\ell = \frac{8}{3}nk_BT \cdot g_{m\ell} \tag{20}$$

$$Si_{R_3} = 4k_BT \cdot R_3 \tag{21}$$

are the PSDs of the currents through M_ℓ and R_3, respectively. The PSD of the flicker noise current at the output for both CTAT generator 1 and CTAT generator 2 are derived as

$$S_{I_{FN1}} = \frac{\alpha_{11}^2\alpha_{13}^2}{\alpha_{12}^2}\left[Sv_{4,1}\cdot g_{m4,1}^2 + 2\cdot Sv_{3c,1}\cdot g_{m3c,1}^2 + (Sv_{1a,1}+Sv_{1b,1})\cdot g_{m1b,1}^2 + 2\cdot Sv_{2a,1}\cdot g_{m2a,1}^2\right] + (Sv_{3a,1}+Sv_{3b,1}+Sv_{3e,1})\cdot g_{m3e,1}^2\frac{\alpha_{13}^2}{\alpha_{12}^2} + (Sv_{5a,1}+Sv_{5b,1})\cdot g_{m5b,1}^2 \quad (22)$$

$$S_{I_{FN2}} = \alpha_2^2\left[Sv_{4,2}\cdot g_{m4,2}^2 + 2\cdot Sv_{3c,2}\cdot g_{m3c,2}^2 + (Sv_{1a,2}+Sv_{1b,2})\cdot g_{m1b,2}^2 + 2\cdot Sv_{2a,2}\cdot g_{m2a,2}^2\right] + (Sv_{3a,2}+Sv_{3b,2}+Sv_{3e,2})\cdot g_{m3e,2}^2 \quad (23)$$

where Sv_ℓ is the PSD of the flicker noise voltage for each transistor M_ℓ and according to [1], it can be derived as

$$Sv_\ell = \frac{2\pi}{w}\frac{N_o}{W_\ell L_\ell}\left(\frac{1+\sqrt{1+i_{f\ell}}}{2}\right)^2\cdot\frac{\log(1+i_{f\ell})}{i_{f\ell}} \quad (24)$$

where N_o is the flicker noise constant, w is the frequency (in radians), $i_{f\ell}$, W_ℓ and L_ℓ are the inversion level, width and length of the transistor M_ℓ, respectively. Therefore, the total PSD of the noise voltage at the output can be derived as

$$Sv_{OUT} = R_3^2\cdot(S_{I_{FN1}} + S_{I_{FN2}} + S_{I_{TN}}) \quad (25)$$

and the dominant pole which the power noise must be integrated can be approximated by $1/(R_3C_{L3})$.

3 CAD tool for voltage reference circuit design

The proposed equation-based CAD tool was implemented in a graphic user interface with the purpose of producing a simple methodology for optimized initial device sizing. The design of the voltage reference circuit aided by the CAD tool is described in the flow diagram of Fig. 7, which can be summarized into two main steps:

Step 1. Enter parameters R_1, R_2, $i_{f4,1}$, $i_{f4,2}$, α_1 and α_2 to adjust the mutual compensation and $V_{IOAT}(T_o)$ to establish the reference voltage at room temperature, and hence determine power consumption, TC, and R_3.

Step 2. Enter desired mismatch value for V_{IOAT} and minimum transistor dimensions. These parameters are then used by the optimization algorithm to minimize the circuit area. The cost function comprises a weighted combination of Eqs. (14) and (17) to exploit tradeoffs between area and mismatch. Capacitor C_{L3} influences the output dominant pole, and therefore its value is needed for noise power computation. Desired area, noise power and device dimensions are saved in an output file.

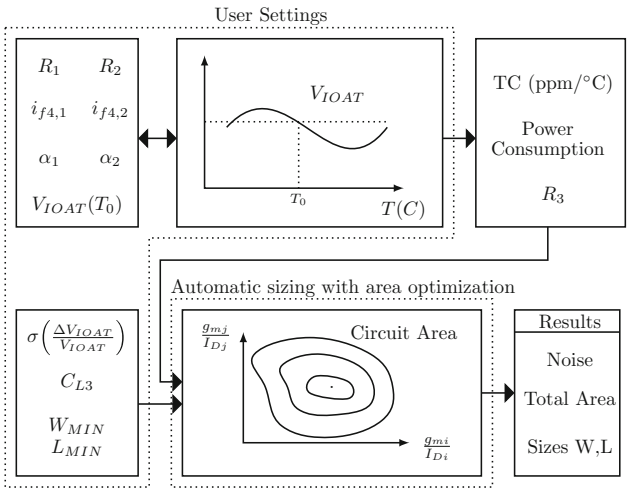

Fig. 7 Diagram of the proposed design methodology

A snapshot of the user interface is presented in Fig. 8. As can be seen at the top left corner, the user selects the following mutual compensation parameters: mirror factors α_1 e α_2, resistances R_1 and R_2, inversion levels $i_{f4,1}$ and $i_{f4,2}$, the desired temperature range, and the nominal output reference voltage. The predicted circuit behavior is shown in three graphics at the selected temperature range. These curves show the resulting voltages $V_{G4,1}$ and $V_{G4,2}$, currents $\alpha_1 I_{CTAT1}$ e $\alpha_2 I_{CTAT2}$, and reference voltage V_{IOAT}.

At the bottom left of the window are the input parameters, namely, the minimum transistor dimensions W_{MIN} and L_{MIN}, the desired mismatch on V_{IOAT}, and the output capacitance C_L. The obtained results are displayed at the bottom left corner, including the estimated area occupied by the transistors, the estimated mismatch on V_{IOAT}, and the estimated RMS noise voltage. The device sizes are saved in the file *result.txt*, as shown at the bottom right corner.

4 A design example

A design example was developed in a 180 nm standard CMOS process and validated through post-layout simulations using Spectre. The temperature behavior simulations of the voltage reference circuit and the CAD tool predictions can be seen in Fig. 9. Note that the temperature coefficient obtained by simulations is 15.20 ppm/°C, whereas the one predicted by the CAD tool is 15.71 ppm/°C. These TC values follow the definition given by

$$TC = \frac{V_{IOATmax} - V_{IOATmin}}{\Delta T\cdot V_{IOATnom}}\times 10^6(\text{ppm}/^\circ\text{C}) \quad (26)$$

where $V_{IOATmax}$, $V_{IOATmin}$ and $V_{IOATnom}$ are, respectively, the maximum, minimum and nominal values of the reference voltage within the temperature range ΔT. The small

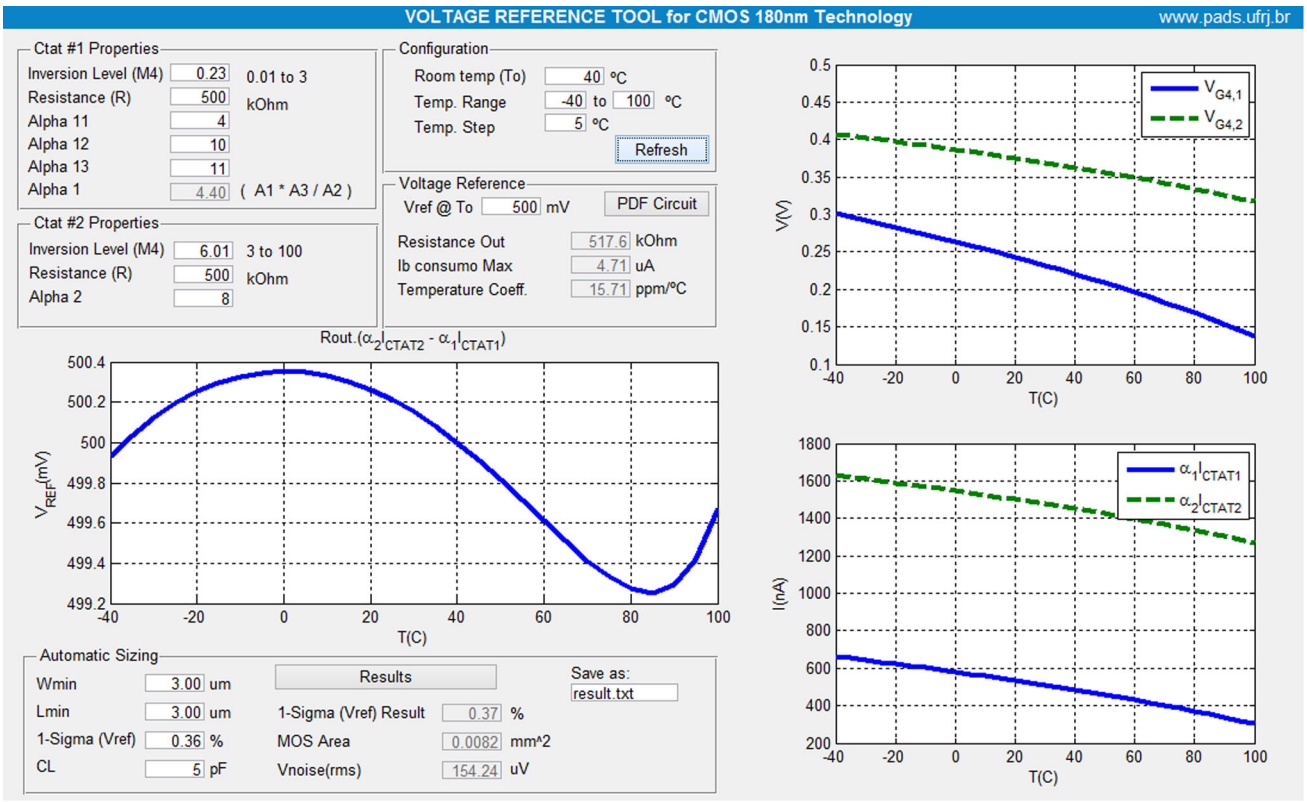

Fig. 8 Graphical user interface of the development CAD tool

prediction errors for the temperature coefficient and the offset voltage are due to the fact that transistor parameters extraction was made for the particular case in which the drain voltage is equal to the gate voltage, hence ignoring mobility reduction effects.

The mismatch variations estimated by the CAD tool were evaluated through Monte Carlo simulations as shown in Fig. 10. The histogram indicates a mean value of the output voltage of 500.7 mV and a standard deviation of 1.71 mV. Both results correspond to a relative standard deviation of 0.34 %, slighty lower than 0.37 %, which was estimated by the CAD tool. The importance of controlling mismatch variations of the voltage reference is that it can be reduced simultaneously with the temperature coefficient variations, since the ratio K_2/K_1 given by Eq. (13) is determined by current and resistance ratios. The influence of such variations on the performance of the voltage reference is presented in Fig. 11 through process and mismatch simulations after calibration of the output voltage at 40 °C (without TC calibration), which was carried out by varying the value of R_3.

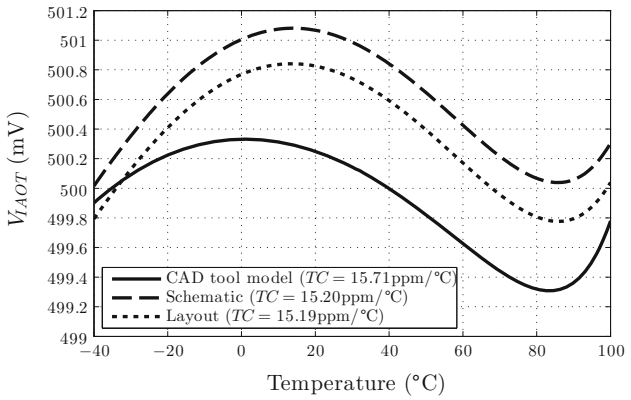

Fig. 9 Temperature behavior results of the CAD tool versus simulations

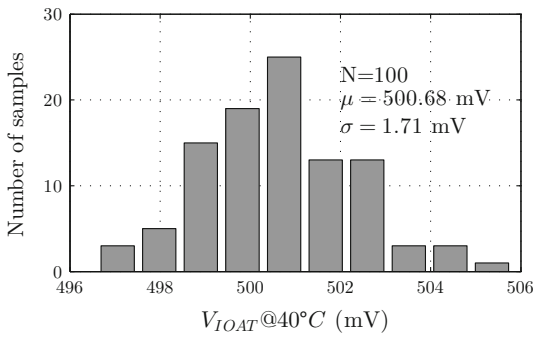

Fig. 10 Histogram simulation results of Monte Carlo mismatch variations (N = 100) on V_{IOAT} at 40 °C

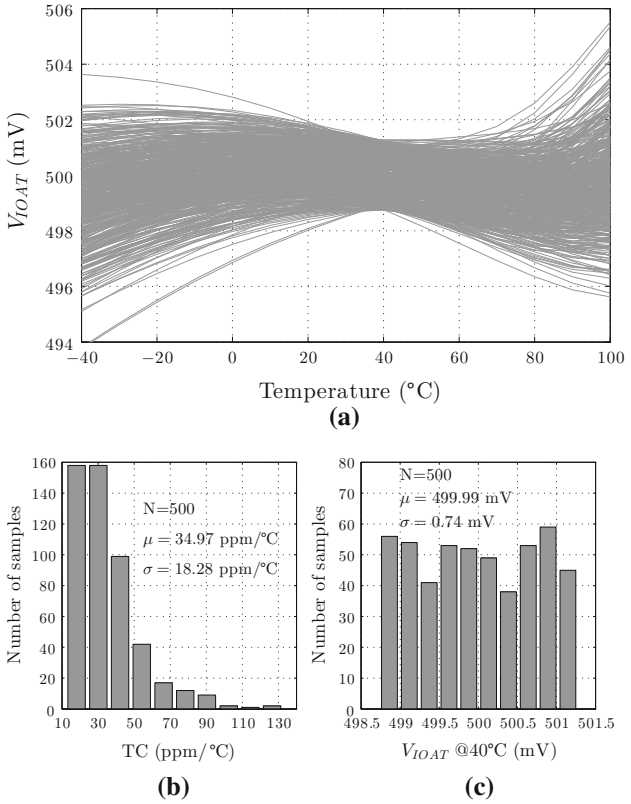

Fig. 11 Histogram simulation results of Monte Carlo process and mismatch variations (over 500 samples) of the circuit after calibration at 40 °C : **a** V_{IOAT} temperature behavior; **b** temperature coefficient histogram; (c) V_{IOAT} histogram at 40 °C

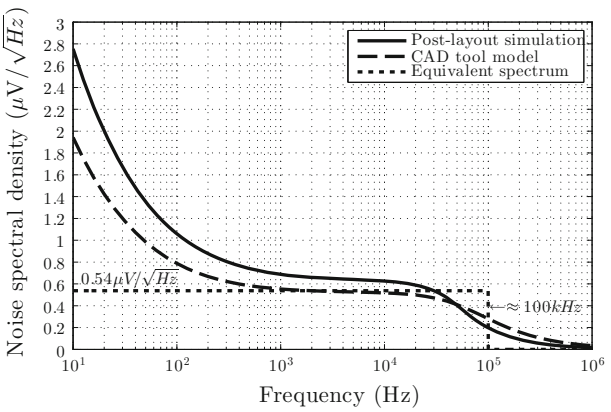

Fig. 12 Noise spectral density produced by the CAD tool *versus* simulated results

As shown in Fig. 12, the noise PSD behavior produced by post-layout simulations of the voltage reference circuit is closeagreement with the one given by Eq. (25) derived in this work and incorporated to the CAD tool. The total noise at the output obtained by simulations is 170 μV_{rms}, whereas the CAD tool predicted 154 μV_{rms}.

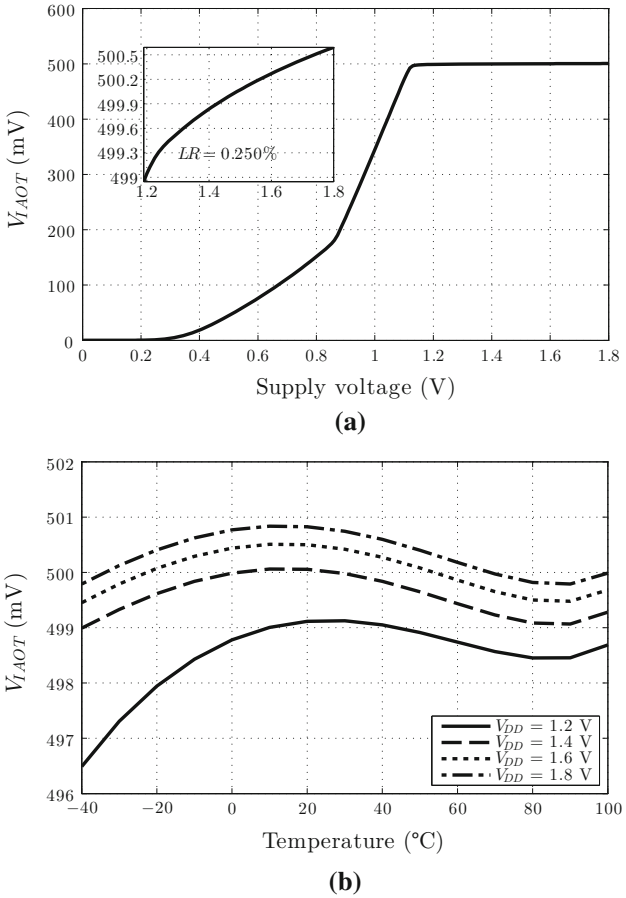

Fig. 13 Simulated results of the voltage reference as a function of the supply voltage: **a** output voltage at 40 °C; **b** temperature behavior

Table 2 Results obtained with the CAD tool and by post layout simulations of the voltage reference circuit

Parameter	CAD tool	Simulation
TC	15.71 ppm/°C	15.19 ppm/°C
Max. Current @-40 °C	4.7 µA	5.0 µA
V_{IOAT} @40 °C	500.0 mV	500.6 mV
$V_{DD(min)}$	N/A	1.2 V
V_{noise}	154 μV_{rms}	170 μV_{rms}
$\sigma(\Delta V_{IOAT})$	0.37 %	0.34 %

Fig. 13 shows simulation result of the voltage reference as a function of supply voltage. The circuit produces the voltage reference value for supply voltage ranging from 1.2 to 1.8 V, and a line regulation

$$LR = \frac{\Delta V_{IOAT}}{\Delta V_{DD}} \cdot 100\,(\%) \tag{27}$$

of 0.250 %.

Table 3 Transistor dimensions obtained with the CAD tool

CTAT Generator 1			CTAT Generator 2		
M	W/L	i_f	M	W/L	i_f
$M_{1a,1}$	100/3	0.1	$M_{1a,2}$	107/9	0.5
$M_{1b,1}$	25/3	0.1	$M_{1b,2}$	27/9	0.5
$M_{2a,1}$	3/44	13.3	$M_{2a,2}$	3/65	32.6
$M_{2b,1}$	3/44	13.3	$M_{2b,2}$	3/65	32.6
$M_{3a,1}$	12/30	41	$M_{3a,2}$	12/39	90.4
$M_{3b,1}$	3/30	41	$M_{3b,2}$	3/39	90.4
$M_{3c,1}$	3/30	41	$M_{3c,2}$	3/39	90.4
$M_{3d,1}$	3/30	41	$M_{3d,2}$	3/39	90.4
$M_{3e,1}$	12/30	41	$M_{3e,2}$	24/39	90.4
$M_{4,1}$	16/3.2	0.23	$M_{4,2}$	7/28	6.0
$M_{5a,1}$	30/10	13.3			
$M_{5b,1}$	33/10	13.3			

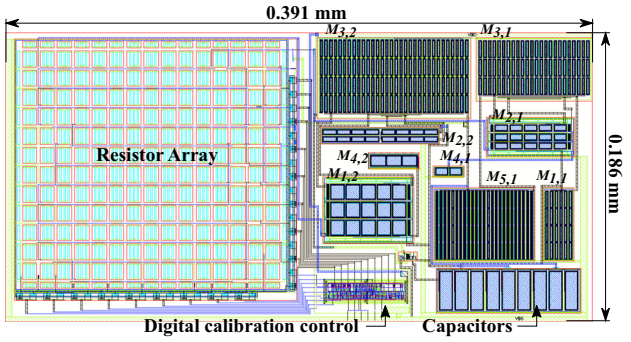

Fig. 14 Layout of the proposed voltage reference

Table 4 Resistance parameters

Material	R_{sq} ($k\Omega$/sq)	TC (ppm/°C)
P^+ Poly	0.260	160
N^+ Poly	0.370	−812
P^+ Diff	0.105	1340
N^+ Diff	0.072	1900
HR Poly	1.600	−1360

A performance summary of the CAD tool voltage reference is presented in Table 2. The transistor dimensions are listed in Table 3. The resistances of R_1, R_2 and R_3 are equal to 500 kΩ and occupy approximately 44 % of the total chip area (Fig. 14), which is 0.072 mm^2. Placed inside the resistor array, resistance R_3 can be adjusted in the range from 422.5 kΩ to 580 kΩ in steps of 2.5 kΩ, thereby enabling calibration of the voltage reference after fabrication. The P^+ poly-silicon resistance is particularly adequate since its temperature coefficient is smaller than those of the other process resistances (Table 4).

Table 5 shows a comparison of the proposed voltage reference circuit with state-of-the-art ones reported in the literature. It can be concluded that the maximum current consumption of 5 μA (at minimum temperature) of the proposed circuit is lower than those of similar CTAT-CTAT topologies, such that its power dissipation is substantially lower. This is due mainly to the fact that transistors that define the circuit currents ($M_{4,1}$ and $M_{4,2}$) operate near weak and moderate inversion levels. The silicon area of the proposed circuit is larger than that of the other designs in Table 5, but this is the trade-off result for controlling the mismatch variations below 0.37 %, which can avoided a temperature coefficient calibration with a mean about 35 ppm/°C.

5 Conclusions

In this work an efficient CAD tool was advanced for voltage reference circuit design. The tool enables the designer to determine the main features at a low computational cost. The fact that mutual compensation transistors operate in sub-threshold region, accurately designed by the CAD tool, makes the proposed approach suitable for low power applications. The current consumption of the circuit

Table 5 Summary of the performance of the proposed voltage reference circuit

	This work	[2]	[3]	[10]	[17]
Supply voltage (V)	1.2*	0.8	1.2	1.2	1.8
Current consumption (μA)	5 (max)*	6.8	120	36	8 (max)
Ref. voltage (mV)	500*	330.5	735	767	847
Temp. range (°C)	−40 to 100	−40 to 85	−40 to 120	−40 to 120	0 to 130
TC (ppm/°C)	15.19*	163*	1.0*	3.4 to 6.9	13.6
PSRR (dB)	−57 @1 kHz*	−47 @3.6 kHz*	−30 @100 kHz	−80 @400 Hz	−72 @DC
Chip area (mm^2)	0.072	0.013	0.063	0.036	0.011
Line regulation (%/V)	0.250*	0.600	–	0.054	0.0185
Noise (RMS)	0.54 μV/$\sqrt{Hz}$*	232 μV*	388 μV	2 μV/$\sqrt{Hz}$	–
CMOS process (μm)	0.18	0.13	0.13	0.18	0.35

* Simulations

designed as an illustrative example is 5 μA, which is lower than what has been achieved in similar topologies reported in the literature. In addition, the proposed architecture produces an adjustable reference voltage, in the sense that its value can be defined by setting the output resistance. The small prediction error for the temperature coefficient shows that the second-order polynomials, that were used to model the transistors along the temperature range, are adequate to voltage reference circuit designs.

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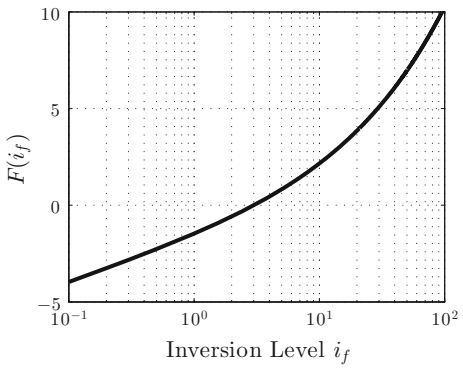

Fig. 15 Behavior of $F(i_f)$ according to the UICM model

Appendix – mutual compensation approach

Using two CTAT generator circuits as shown in Fig. 3, we obtain CTAT voltages given by

$$V_{CTAT\ell}(T) = K_\ell \cdot V_{G4,\ell}(T) \quad \ell = 1, 2 \tag{28}$$

where

$$V_{G4,\ell}(T) = V_{Ton}(T) + \frac{k_B T}{q} \cdot n_n(T) \cdot F(i_{f4,\ell}) \quad \ell = 1, 2 \tag{29}$$

The mutual compensation can be derived assuming that $V_{CTAT2}(T)$ minus $V_{CTAT1}(T)$ does not change with temperature, which can be established by the conditions

$$V_{CTAT2}(T_o) - V_{CTAT1}(T_o) = V_{IOAT} \tag{30}$$

$$\frac{\partial V_{CTAT2}(T_o)}{\partial T} - \frac{\partial V_{CTAT1}(T_o)}{\partial T} = 0, \tag{31}$$

where V_{IOAT} is the desired output voltage and T_o is the room temperature. Combining Eqs. (30) and (31), we obtain,

$$K_2 - K_1 = \frac{V_{IOAT}}{V_{Ton} - V'_{Ton} \cdot T_o} \tag{32}$$

$$K_2 F_2 - K_1 F_1 = \frac{q}{n_n k_B} \cdot \frac{V'_{Ton} \cdot V_{IOAT}}{V'_{Ton} \cdot T_o - V_{Ton}} \tag{33}$$

Now, fixing the gain K_1 and the function F_1 through the inversion level i_{f1}, as in Eq. (2), yields

$$K_2 = \frac{K_1(V'_{Ton}T_o - V_{Ton}) - V_{IOAT}}{V'_{Ton}T_o - V_{Ton}} \tag{34}$$

$$F_2 = \frac{K_1 F_1 (V'_{Ton}T_o - V_{Ton}) + \frac{q}{n_n k_B} V_{IOAT} V'_{Ton}}{K_1(V'_{Ton}T_o - V_{Ton}) - V_{IOAT}}. \tag{35}$$

Therefore, by using the calculated values for K_1, K_2, F_1 and F_2, a mutual compensation (Eq. (13)) that generates the voltage V_{IOAT} at the output of the reference is achieved.

The proposed technique based on the above equations takes advantage of the second term of Eq. (29), as follows.

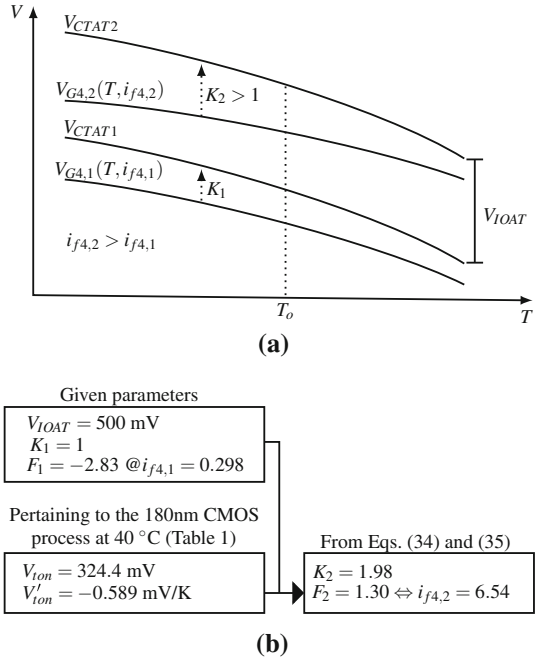

Fig. 16 Diagram of the proposed technique to achieve the mutual compensation that takes advantage of the NMOS multi-threshold characteristics: **a** graphical representation; **b** numerical example

Since the thermal voltage ($k_B T/q$) has PTAT behavior and $F(i_f)$ increases monotonically with i_f (see Fig. 15), the inversion level can be used to adjust the temperature influence according to Fig. 4. As illustrated in Fig. 16(a), an increase of the inversion level $i_{f4,2}$ makes it possible to reduce the temperature influence and increase the value of the voltage $V_{G4,2}$. Consequently, by multiplying $V_{G4,2}$ by the factor $K_2 > 1$, we can increase the temperature influence again, and create a voltage V_{CTAT2}, which decreases with the temperature at practically the same rate as that of the voltage V_{CTAT1} (produced by $K_1 V_{G4,1}$). Finally, the difference between V_{CTAT2} and V_{CTAT1} yields V_{IOAT} (Eq. (30)). V_{IOAT}. In Fig. 16(b) we present an illustrative numerical example in which fixing V_{IOAT}, K_1 and F_1, the

required values of K_2 and F_2 are obtained. To reduce power consumption, F_1 should be as low as possible, which is limited by the value of $V_{G4,1}$ at maximum temperature, thereby ensuring the correct operation of $M_{4,1}$.

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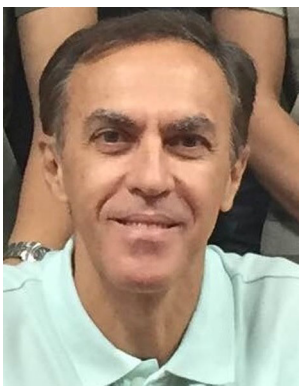

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