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Electronically tunable memristor emulator circuit

Hasan Sözen[1] · Uğur Çam[2]

Abstract In this paper, memristor emulator circuit which is built with off the shelf electronic devices is presented. It consists of three operational transconductance amplifiers (OTA) and four second generation current conveyors (CCII). Using OTA offers an extra control parameter, operational transconductance parameter (g_m), in addition to frequency (f) and amplitude value of voltage across emulator (v_m). Since g_m is proportional to current flowing through the bias terminal of OTA, it is possible to change the memristance variation via a simple change of amplitude value. Since g_m parameter is adjustable via an external dc voltage/current source, the memristance of presented emulator circuit is electronically tuneable. Mathematical model is derived to characterize the behaviour of the emulator circuit. Frequency analysis is performed to determine how to maintain the pinched hysteresis loop at high frequencies. The presented emulator circuit is simulated with SPICE simulation program. The breadboard experiment of emulator circuit is built using CA3080 and AD844 ICs for OTA and CCII devices respectively. Frequency dependent pinched hysteresis loop in the current versus voltage plane holds up to 10 kHz. Mathematical model and theoretical analyses show a good agreement with SPICE simulation and experimental test results.

Keywords Memristor emulator · Electronically tunable memristance · Memristor · g_m Controlled memristor

1 Introduction

There are four circuit variables in circuit theory; namely charge, voltage, current and flux. Five of possible six combinations between circuit variables are well known. Three of them defines resistor, capacitor and inductor. Current and voltage are defined by two of remaining possible three combinations. Prof. Leon Chua, postulated the mathematical relations of the fourth fundamental two terminal circuit element, memristor, which defines the missing relation between flux and charge [1]. Memristor is a nonlinear resistor with memory. In 1976, Chua and Kang generalized memristor concept to much broader class called memristive systems [2]. Both memristor and memristive devices have the pinched hysteresis loop in the current versus voltage plane. Thus, the resistance of the device depends on the time history of the current flowing through it. Under sinusoidal excitation, the area of the pinched hysteresis loop is inversely proportional to frequency of voltage signal across the memristor [2]. On May 1, 2008 Stanley Williams and his group fabricated two terminal memristor using titanium dioxide (TiO_2) nanoscale device [3]. Recently, Di Ventra et al. [4] extended the notion of memristive systems to memcapacitive and meminductive systems and defined the special cases of the newly extended systems as memcapacitors and meminductors. Scientists have used memristor in wide application areas such as; programmable logic, signal processing,

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neural networks, oscillators, image processing, etc. [5–10] since the first physical realization of memristor.

It is important to have a simulation model for memristive devices to investigate their effects in circuits and verify the theoretical analyses. In the literature, several SPICE models for memristor [12–23] memcapacitor [24] and meminductor [25] elements have been proposed.

Memristor is still unavailable commercially. It is difficult to fabricate it due to technical drawbacks and high cost. In the literature several emulator circuits for memristor have been presented in order to experimentally explore dynamics of memristor in electronic circuits [26–40]. Indeed, Prof. Leon Chua proposed the first emulator circuit with relatively complex and bulky structure [1]. Many of the emulator circuits in the literature were realized using analog multiplier to obtain flux controlled memristance [26, 30, 31, 34–37, 39]. Analog multiplier circuit is used to multiply the flux of the emulator with the voltage across emulator circuit. Some emulator circuits have grounded restriction [26, 28, 29, 32, 33, 38, 39]. In [26], a flux controlled emulator circuit with smooth piecewise-quadratic nonlinearity was proposed and used in a chaotic circuit. The emulator circuit was complex and bulky. Pershin and Ventra proposed a memristor emulator using digital potentiometer, microcontroller and analog to digital converter and used in programmable analog circuits. The presented memristor emulator was based on threshold-type behaviour. The emulator had some drawbacks since the resolution of digital signal and digital potentiometer is finite [27]. Biolek et al. [28] presented a mutator which transform a nonlinear resistor into memristor. In [29], memristor emulator that consists of an integrator and a controllable resistor. JFET was used as a controllable resistor by the output voltage of integrator block in presented emulator circuit. In [30], an incremental/decremental memristor emulator was proposed. It requires several integrated circuits and it is bulky with limited operation frequency. Abuelma'atti and Khalifa [32, 33] presented memristor emulator using current feedback operational amplifiers and used in digital circuits. In [34], floating flux controlled memristor emulator is presented using two op amps and single analog multiplier. Presented memristor emulator circuit in the same study was transformed to memcapacitor circuit by using current conveyors. In [35, 36], floating flux controlled memristor emulator using current conveyors was presented. Elwakil et al. [38] proposed a mathematical model capable of generating double loop hysteresis behaviour and an emulator circuit using current conveyors and analog multiplier which satisfies the model. In [39], a grounded charge controlled memristor emulator was presented using CMOS DDCC and analog multiplier.

In this paper, memristor emulator circuit using OTA and CCII elements is proposed. Using OTA offers an extra control parameter, transconductance parameter (g_m), in addition to frequency (f) and amplitude values of applied voltage across emulator (v_m), in order to adjust memristance variation. Furthermore, the proposed emulator circuit has continuous state levels to achieve several memristance levels different from emulators with binary state levels. It is shown by frequency analysis that the pinched hysteresis loop holds up to 10 kHz. In Sect. 2, we introduce our emulator circuit with its mathematical model. In Sect. 3, frequency analysis is performed. Simulation results are given in Sect. 4. Conclusion of the paper is given in Sect. 5.

2 Memristor emulator circuit

Memristor defines a nonlinear relationship between charge q and flux φ. It is the fourth fundamental circuit element since its characteristics cannot be duplicated by any combination of other fundamental circuit elements. For a charge controlled memristor, its relation is $\varphi(t) = \varphi(q)$, where its relation becomes $q(t) = q(\varphi)$ for flux controlled memristor. For a flux controlled memristor, nonlinear constitutive relationship between the memristor terminal voltage v and the internal current i can be written as following equation.

$$v(t) = M(\varphi)i(t) \tag{1}$$

In this paper, flux controlled memristor emulator which works only for floating state is proposed. In case of grounding one of the terminal, the mathematical relations for memristance become obsolete. It uses three operational transconductance amplifiers, four second generation current conveyors, six resistors and one capacitor elements as given in Fig. 1. The g_m parameters of U5 and U6 are used for multiplication process. Therefore only g_m parameter of U1 (g_{m1}) can be used to change memristance characteristic besides f and v_m.

In ideal case, current flowing through input terminals of operational transconductance amplifier and terminal Y of CCII is zero. Hence, for the presented circuit, all current passes through the resistor R_1. Input current can be written as following where $v_A(t)$ defines voltage at node A.

$$i_{in}(t) = \frac{v_A(t)}{R_1} \tag{2}$$

U1 with capacitor C (omitting R_2) perform integral function. R_2 is used to eliminate the output offset of the integrator. When DC level is ignored the mathematical relation of the integrator block can be given as the following;
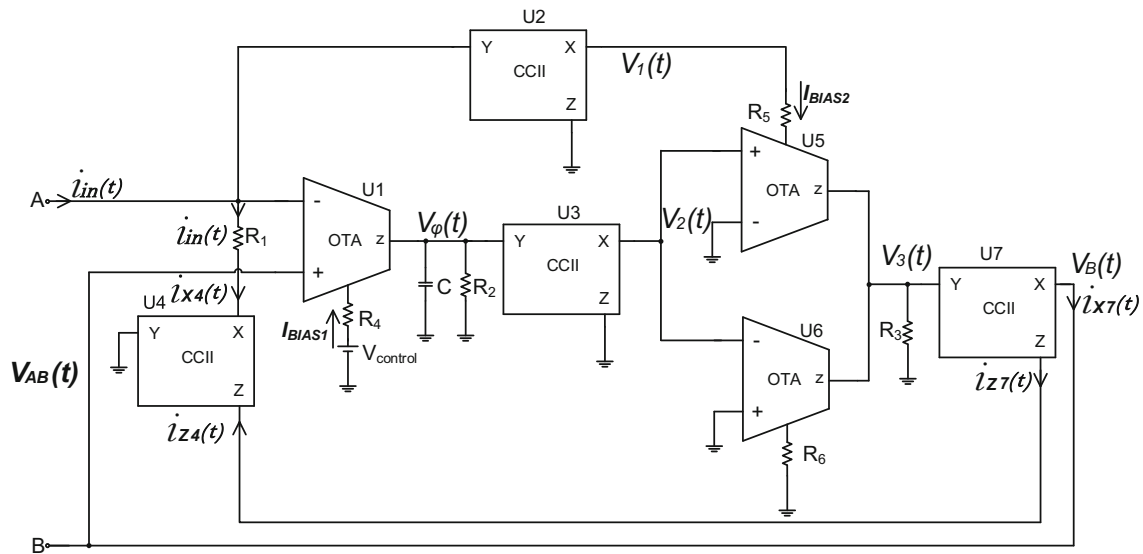
Fig. 1 Emulator circuit for floating memristor

$$v_\varphi(t) = -\frac{g_{m1}}{C} \int (v_A(\tau) - v_B(\tau))d\tau \tag{3}$$

where g_{m1} denotes the transconductance parameter of U1. Since the flux is defined as $\varphi_{AB}(t) = \int (v_A(\tau) - v_B(\tau))d\tau$, relation given in (3) can be written as;

$$v_\varphi(t) = -\frac{g_{m1}}{C} \varphi_{AB}(t) \tag{4}$$

U2 and U3 are used to copy voltages $v_A(t)$ and $v_\varphi(t)$ without any current copying to their terminal X, since the current flowing through terminal Y of CCII is zero [11]. U4 is used to perform the input–output current equality with U7 since the current flowing through terminal X of CCII is equal to current flowing through terminal Z. Thus the following relations are obtained.

$$i_{in}(t) = i_{X4}(t) = i_{Z4}(t) = i_{Z7}(t) = i_{X7}(t) = i_B(t) \tag{5}$$

OTA pairs U5 and U6 are used to multiply the voltages $v_1(t)$ and $v_2(t)$ denoted in Fig. 1 [41]. The mathematical description of the multiplying process using U5 and U6 devices can be obtained as;

$$v_3(t) = -\frac{g_{m1}\varphi_{AB}(t)v_A(t)R_3}{2V_TR_5C} \tag{6}$$

where V_T is the thermal voltage given by KT/q. Thermal voltage (T) is 26 mV at room temperature, K is Boltzmann's constant and q is charge. When there is not an important change in room temperature, the effect of V_T on circuit operation becomes negligible.

U7 is used to copy the voltage $v_3(t)$ to node B and provides all current at outputs of U5 and U6 to flow through resistor R_3. Hence, the voltage across the emulator circuit can be written as;

$$v_A(t) - v_B(t) = i_{in}(t)R_1 + \frac{g_{m1}\varphi_{AB}(t)i_{in}(t)R_1R_3}{2V_TR_5C} \tag{7}$$

By making use of (2) the following equation can be obtained;

$$v_{AB}(t) = i_{in}(t)\left[R_1 + \frac{g_{m1}R_1R_3\varphi_{AB}(t)}{2V_TR_5C}\right] \tag{8}$$

It is obvious from (8) that the memristance expression for flux controlled memristor emulator circuit can be obtained as;

$$M_{AB}(\varphi) = \left[R_1 + \frac{g_{m1}R_1R_3\varphi_{AB}(t)}{2V_TR_5C}\right] \tag{9}$$

3 Frequency behaviour analysis

The emulator circuit has a memristance expression which consists of connected series of a linear time invariant resistor with a flux and g_{m1} controlled linear time varying resistor. Assuming that the power supply for used ICs is $\pm V_{dd}$ and a sinusoidal voltage $v_{AB}(t) = v_m \sin(2\pi ft)$ is imposed on terminals A and B, the memristance can be calculated as;

$$M_{AB}(\varphi) = \left[R_1 - \frac{g_{m1}R_1R_3v_m\cos(2\pi ft)}{4\pi fV_TR_5C}\right] \tag{10}$$

The relationship between time variant and time invariant parts of memristance denotes the frequency and g_{m1} dependence of pinched hysteresis loop. The relationship between two parts can be described by the ratio of amplitudes of time variant and time invariant parts as following.

$$k = \frac{g_{m1}R_3 v_m}{4\pi f V_T R_5 C} = \frac{1}{\tau f} \qquad (11)$$

where $\tau = \frac{4\pi V_T R_5 C}{g_{m1}R_3 v_m}$ is the time constant of the emulator circuit. It is obvious from (11) that k is inversely proportional to f. On the other hand increasing g_{m1} will increase k on the contrary f. Therefore, g_{m1} and f can be used for holding pinched hysteresis loop at high frequencies. There are three conditions between k and pinched hysteresis loop of memristance.

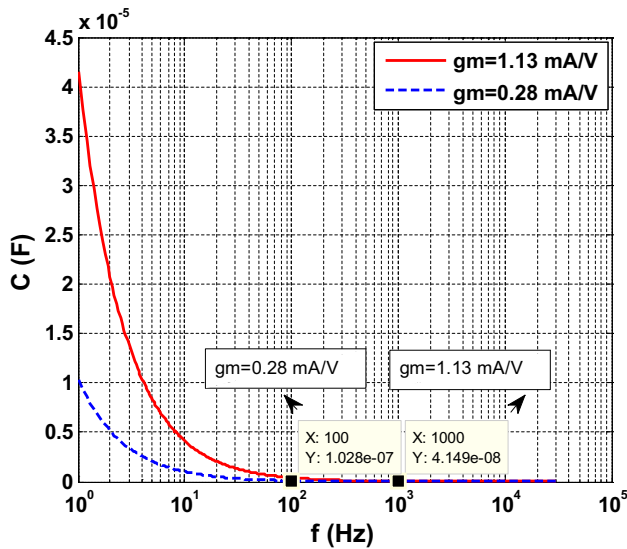1. $k \rightarrow 0$, the memristance approximates to linear resistor.

2. $k \rightarrow 1$ the memristance has the maximum pinched hysteresis loop.
3. $k \geq 1$ the memristance value will have negative or zero value due to "$cos(2\pi ft)$" expression in Eq. (10).

Consequently the numerical value of k must be on the interval, i.e., $0 < k < 1$ for achieving pinched hysteresis loop. Since "$cos(2\pi ft)$" can take values in the interval ± 1, in order to obtain positive memristance value, f must satisfy the following denoted in (11). Since voltages on circuit

Fig. 2 Variation of capacitor C with frequency for k = 0.5

Table 2 Component List used in emulator circuit

Element	Value	Frequency range
V_{dd}	± 15 V	
V_m	100 mV	
R_1	10 KΩ	
R_2	40 KΩ	
R_3	15 KΩ	
R_4	500 KΩ	
R_5	200 KΩ	
R_6	200 KΩ	
C	10 uF	1–10 Hz
	1 uF	10–50 Hz
	220 nF	50–100 Hz
	100 nF	100–500 Hz
	47 nF	500–1 kHz
	22 nF	1–5 kHz
	10 nF	5–8 kHz
	4.7 nF	8–10 kHz

Table 1 Comparison of presented emulator circuit with other published studies

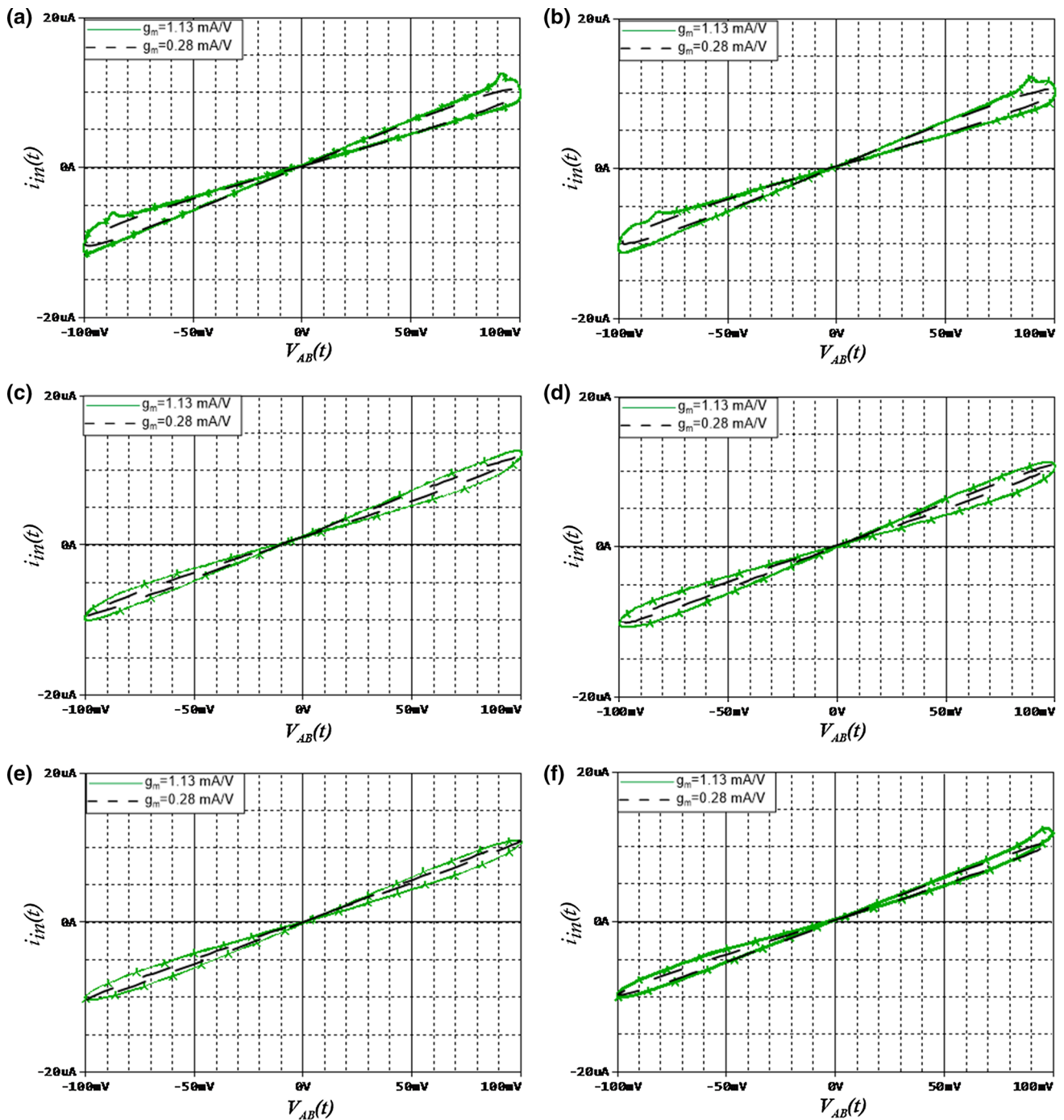| Emulator	Maximum frequency for memristor regime	Control parameter of emulator
[26]	1 kHz	V_m, f_m
[27]	50 Hz	V_m, f_m
[28]	100 Hz	V_m, f_m
[29]	2 Hz	V_m, f_m
[30]	800 Hz	V_m, f_m
[31]	17 Hz	V_m, f_m
[32]	500 Hz	V_m, f_m
[33]	600 Hz	V_m, f_m
[34]	50 Hz	V_m, f_m
[35]	20.2 kHz	V_m, f_m
[36]	120 Hz	V_m, f_m
[37]	16 Hz	V_m, f_m
[38]	100 Hz	V_m, f_m
[39]	1 MHz	V_m, f_m
[40]	5 kHz	$V_m, f_m\ g_m$
Presented	10 kHz	$V_m, f_m\ g_m$

Fig. 3 Frequency dependent pinched hysteresis loop of memristor emulator circuit for different frequencies: **a** 10 Hz, **b** 100 Hz, **c** 1 kHz, **d** 5 kHz, **e** 8 kHz, **f** 10 kHz

branches must be bounded by power supply voltage V_{dd}, it is more logical to use f and g_{m1} as control parameters of pinched hysteresis loop rather than v_m. Capacitor C, with other parameters; f, v_m, g_{m1}, can be used to for holding pinched hysteresis loop at high frequencies. The approximated values for C in function f are given in Fig. 2 for $k = 0.5$. Values of the other elements are given in Table 1.

$$f > \frac{g_{m1}R_3 v_m}{4\pi V_T R_5 C} \quad (12)$$

Therefore, based on (10) and (11), and the configuration of $v_A(t) - v_B(t)$, all the possible values of memristance satisfy the following;
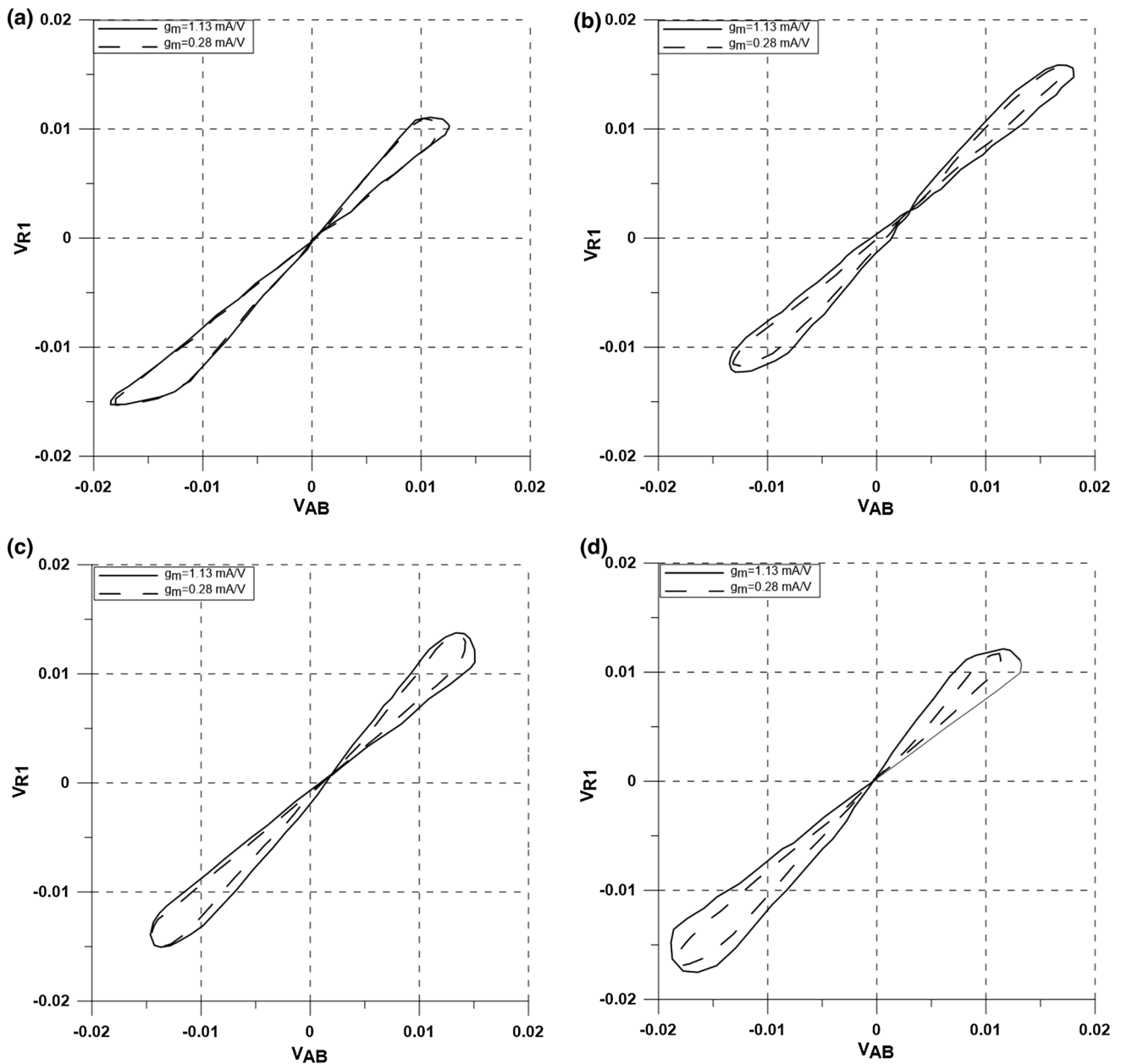
$$0 < M_{AB} < 2R_1 \quad (13)$$

Fig. 4 Grapher program outputs of the frequency dependent pinched hysteresis loop of memristor emulator circuit for different frequencies: **a** 100 Hz, **b** 1 kHz, **c** 5 kHz, **d** 10 kHz

The additional control parameter, g_{m1}, is adjusted via an external DC voltage source, $V_{control}$, as shown in Fig. 1. The value of g_{m1} is determined by the relation which is given in (14). It is derived by taking the schematic diagram of OTA type CA3080 into account [42].

$$g_m = 19.2 \left(\frac{V_{control} + V_{EE} - V_{BE}}{R_4} \right) \qquad (14)$$

4 Simulation and experimental test results

Theoretical analyses are verified using PSPICE simulation program. SPICE models of CA3080 and AD844 ICs are used for OTA and CCII devices, respectively. The circuit parameters used in simulations are given in Table 2. In order to hold loop up at 10 kHz, values of R_2 and C are altered. The new values are given in Table 2. Comparison
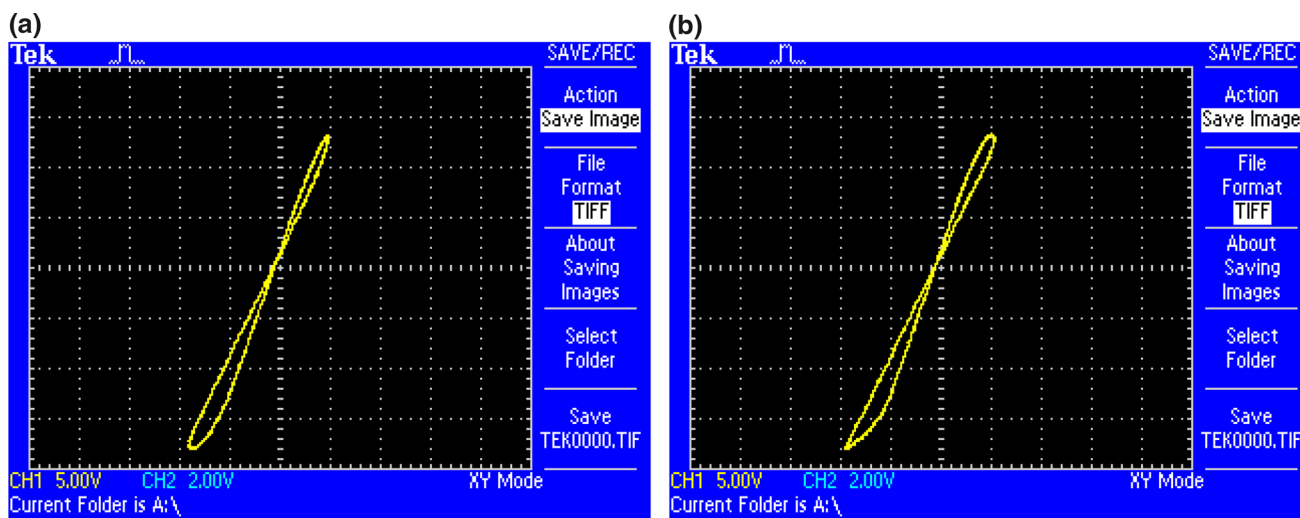
Fig. 5 Oscilloscope trace of the frequency dependent pinched hysteresis loop of memristor emulator circuit for f = 1 kHz for each g_{m1} parameters. For **a** $g_{m1} = 0.28$ mA/V, **b** $g_{m1} = 1.13$ mA/V

of presented memristor emulator circuit with other published studies is given in Table 1.

Simulation results given in Fig. 3 are obtained for two distinct g_{m1} parameters; i.e., 1.13 and 0.28 mA/V. The emulator circuit is simulated for different frequencies for each g_{m1} parameter. These g_{m1} values are determined randomly. It is obvious from (10) and (11) that for bigger g_{m1} parameter, the area of pinched hysteresis loop increases and vice versa. In order to maintain the pinched hysteresis loop, value of capacitor C is changed together with R_2 as given in Table 2. Therefore, it is possible to maintain memristance characteristic at high frequencies. SPICE simulation results given in Fig. 3(a–f) are obtained for 10 Hz, 100 Hz, 1 kHz, 5 kHz, 8 kHz and 10 kHz respectively. It is seen from the figures that the area of pinched hysteresis loop increases for higher g_{m1} parameters for each frequency value as it is expected from (10) and (11). It is obtained from simulation results that the reaction of pinched hysteresis loop is different for each frequency value due to the value of capacitor C in the integrator block. This situation confirms (10) and (12). When the value of C is choose high, the variation of memristance becomes smaller and vice versa. As it is seen in Fig. 3(a–f), frequency dependence of hysteresis loop can be controlled by g_{m1} parameter and mainly with C and R_2 elements. Therefore, it becomes possible to hold up memristance characteristic at high frequencies. The power consumption of the presented emulator circuit is calculated as 1.2 μW.

The breadboard experiment of proposed emulator circuit is built using commercially available ICs; CA3080 and AD844 for OTA and CCII elements, respectively. Numerical values of passive elements are given in Table 2. Measurements are obtained for each g_{m1} parameter as

performed in SPICE simulations. Circuit parameters given in Table 2 are used. Since $v_A(t)$ is R_1 times of input current, the numerical values of voltages $v_A(t)$ and $v_{AB}(t)$ are taken by a flash memory and plotted using Grapher plot program. Figure 4(a–d) show the Grapher program outputs for 100 Hz, 1 kHz, 5 kHz, and 10 kHz respectively. Frequency dependence of the pinched hysteresis loop shows high accuracy with simulation results and mathematical model of memristor emulator circuit. Also, the picture of $i-v$ hysteresis for each g_{m1} parameter is included for f = 1 kHz in Fig. 5.

5 Conclusion

In this paper, an emulator circuit of a flux-controlled memristor which is composed of OTAs and CCIIs has been presented. The most significant feature of the proposed emulator circuit is the possibility of controlling memristance value by changing transconductance parameter of one of the used operational transconductance amplifier by a bias voltage. By this way, in addition to frequency and amplitude values of input voltage across memristor, transconductance parameter is added as a control parameter for memristance variation. The mathematical expressions are given to describe the behavior of presented circuit. CA3080 and AD844 ICs are used to build the emulator circuit for practical application of memristor. It has continuous state levels to achieve several memductance levels which are different from emulators with binary state levels. Frequency analysis has been performed to present a design guideline to hold pinched hysteresis loop of current–voltage curve at high frequencies. Moreover, our emulator

works for different frequency ranges with a simple change in capacitor C. The oscilloscope measurements from the breadboard experiment circuit and SPICE simulation results verifies the theoretical analyses.

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