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Design methodology for low power RF LNA based on the figure of merit and the inversion coefficient

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Abstract The complexity of radiofrequency circuit design comes from the large number of parameters to be adjusted. Constant node shrink in CMOS process and variation of technology skills significantly contribute to this complexity. The paper reports on a reliable and portable design methodology based on a low-power figure of merit (FOM) and inversion coefficient applied to the design of a low noise amplifier (LNA). The design procedure considers the circuit specifications and the optimization of the FOM. As a case of study it is applied to 2.4 GHz LNA designed in a 28 nm technology then exploited to compare different CMOS technology nodes: 28, 65, 130 nm.

Keywords LNA · RF · Design methodology · FOM · Inversion coefficient · Low-power · CMOS

1 Introduction

The market of connected mobile devices is booming with the development of Smartphone, tablets, watches, and the emergence of new needs such as wireless sensor networks (WSN) and bio-data networks (BAN). The tight time to market, and cost of development, impose companies to improve design procedures for new product generations. Among the most famous optimization algorithms exploited in the design of analog/RF circuits are: genetic algorithms [1] or neural networks [2]. However the complex description of the circuit parameters to set up the optimization procedure, the simulation time and the final circuit performances do not significantly improves the design procedure of wireless circuits and systems. New design methodologies are mandated to address the development of future RF circuits.

The small form factor of modern electronic devices imposes power saving and advanced energy management. For the RF functions the use of a figure of merit (FOM) which represents the trade-off between the performances and the power consumption, is a relevant approach to perform both power saving and/or the optimization of the circuit characteristics.

Finally, in advanced Silicon technologies, the increase of the cut-off frequency (f_T) in CMOS contributes to the reduction of the power consumption of RF blocks, however the variation of technology characteristics from one node to another makes difficult the portability of circuits and design methodologies. In order to address this issue, a design approach is proposed based on the inversion coefficient (IC) [3]. The IC is a normalization of MOS drain current which allows a description of the transistor behavior independently of technological parameters.

The paper is organized as follows: Sect. 2 discusses a low-power FOM for biasing optimization based on an IC description. This approach is validated with measurement results. Section 3 proposes a design methodology which is exploited to compare different technological nodes. Section 4 describes the normalization of MOS transistor characteristics with the IC. Section 5 presents a complete

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design methodology applied to the implementation of a 2.4 GHz LNA based on a current reuse topology in a 28 nm CMOS process of STMicroelectronics.

2 FOM Polarization

2.1 Inversion Coefficient, IC

The IC description of MOS drain current is derived from the charge-based model [3]. Unlike surface-potential-based models, it provides a simple and continuous model of transistor in all operating regions. Furthermore, IC parameter allows a comprehensive analysis and optimization of circuits, according the biasing conditions.

The IC (1) [3, 4] is the measure of the channel inversion level when the transistor is in saturation. The transistor work in saturation when the voltage V_{DS} is higher than the pinch-of voltage (or V_{DSsat}) [3]. IC is a drain-current normalization over the technological parameter $I_{spec\diamond}$, defined in (2), and the ratio between transistor width (W) and length (L):

$$IC = \frac{I_D}{\frac{W}{L}.I_{spec\diamond}} \tag{1}$$

$$I_{spec\diamond} = 2n\mu_0 C_{ox} U_T^2 \tag{2}$$

In (2), C_{ox} is the oxide capacitance per unit area, U_T (=kT/q) is the thermal voltage, μ_0 is the low-field surface mobility; n is a slope factor (which moves from 1.4 for Weak Inversion to 1.6 for Strong Inversion, but it is fixed at 1.5). The different operating regions in saturation are: Weak Inversion (or subthreshold voltage; WI: IC <0.1), Moderate Inversion (close to the threshold voltage; MI: 0.1 < IC < 10) and Strong Inversion (higher than threshold voltage; SI: IC >10).

2.2 FOM optimization

Since the 1970s, low power analog designs have been optimized by maximizing the metric «gm/I_D» [5], namely current efficiency, which is maximum in weak inversion region—i.e. IC <0.1—in Fig. 1. For RF applications, the transistors are usually biased in SI region—i.e. IC >10—where the f_T is high (Fig. 1). Unfortunately the current efficiency is low in the SI region which is not relevant for power saving. Since the 2000s, new metrics such as «gm^2/I_D» [6] and «gm f_T/I_D» [7] have been introduced for the design of low power RF. The (gm f_T/I_D), Fig. 1, is maximum in MI region which represents a good trade-off between current efficiency and speed. Interestingly the technology scaling improves the f_T which becomes now considerably higher than the operating frequency of RF applications: f_T >350 GHz in 28 nm CMOS. The design of

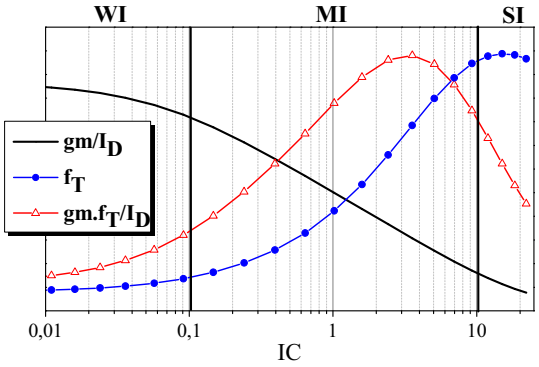


Fig. 1 Design metric: « gm/I_D » , f_T and « gm f_T/I_D » versus IC

RF circuits in MI region becomes more and more attractive as the circuits performances benefit from technology scaling, and the FOM are optimized.

In LNA design, the two most important characteristics are the voltage gain (A_v) and the noise factor (F) which define the receiver sensitivity. The linearity (IIP3) is also considered but the optimization of the IIP3 is critical in base-band signal. Indeed the level of non-linearity and inter-modulation is magnified by the gain of the receiver chain, and base-band circuits have to process signals with large distortions. Hence the linearity of a LNA has to meet the standard specification, and does not need to be optimized. For this reason we will further use the FOM defined in (3) [6] which considers: the minimum noise factor (F_{min}), the unmatched voltage gain (Av_{abs}) and the power consumption (I_D V_{dd}) at the operating frequency ($freq_{GHZ}$).

$$FOM = \frac{Av_{abs}.freq_{GHz}}{(F_{\min}-1)_{abs}.(I_D.Vdd)_{mW}} \tag{3}$$

A basic NMOS common source configuration with capacitive load, Fig. 2, is simulated in a 28 nm CMOS technology for a fixed V_{DD}. The simulation results are reported in Fig. 3 versus the IC. We can observe Av and F_{min} are respectively maximum and minimum in MI region [6]. The degradation of these performances in strong inversion is due to the carriers' velocity saturation.

For the circuit of Fig. 2, the FOM defined in (3) and the (g_m f_T/I_D) of the transistor are reported in Fig. 4. The two

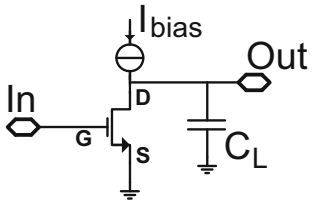


Fig. 2 Capacitive load common in CMOS 28 nm technology source with W_N = 11 µm, L_N = 30 nm, C_L = 100 fF

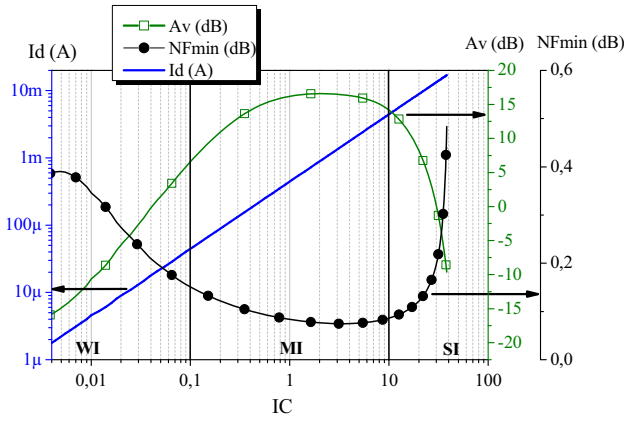


Fig. 3 Voltage gain (*Av*), minimum noise figure (NF_{min}) at 2.4 GHz and current (I_D) versus IC: capacitive load common source simulation in CMOS 28 nm

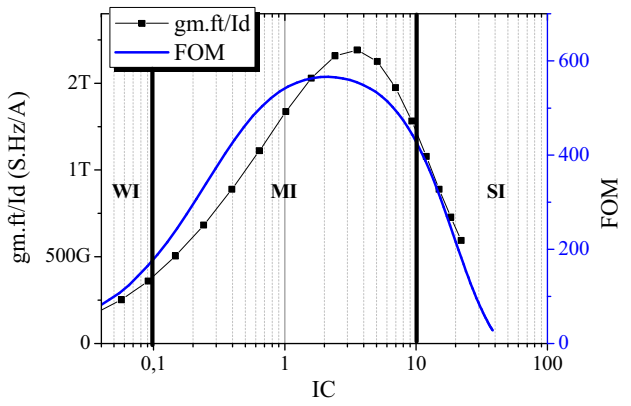


Fig. 4 FOM at 2.4 GHz and « gm f_T/I_D » versus IC: capacitive load common source simulation in CMOS 28 nm

metrics exhibit a close-form evolution, and reach a maximum in the MI region. The IC value for FOM_{max}, 2, is close to the value for $(g_m\ f_T/I_D)_{max}$, 3.5. Unlike the $(g_m\ f_T/I_D)$ the FOM actually represents the performances of the circuit which makes it a relevant metric for the design of low power LNA.

2.3 FOM measurement

Two low power RF LNA, implemented in a 130 nm CMOS technology and dedicated to the 2.4 GHz ISM band are measured. These circuits were designed and optimized with the $(g_m\ f_T/I_D)$ approach.

The first LNA, Fig. 5, is a cascode topology with an inductive degeneration and a body bias tuning. The control of the substrate voltage (V_{BS}) is intended for performance optimizations in various regions of inversion. The circuit takes place in a 2 mm^2 silicon area.

The second circuit is based on a current-reuse configuration, Fig. 6. A capacitive divider combined with the series inductor L_G performs the input matching. The circuit

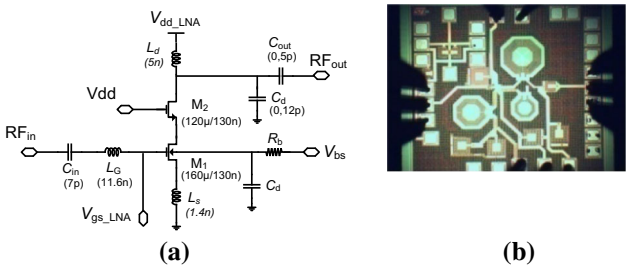


Fig. 5 Inductively degenerated cascode : schematic (**a**) and picture (**b**)

only needs one inductor (L_G), L_{pk} belongs to the buffer, which reduces the silicon footprint to 0.63 mm^2.

The two circuits are measured at 2.4 GHz with a fixed V_{DD}. The transistor inversion region is adjusted by changing the gate biasing (V_{GS}). For the two circuits, the measured S_{21} and the noise figure NF are reported in Fig. 7. For the two circuit configurations, the gain and NF characteristics exhibit the same evolution, in good agreement with the simulation presented in Fig. 3. Furthermore the FOM figures out a maximum in the moderate inversion for an IC close to 1.5. These measurement results confirms the existence of an optimum polarization in the moderate inversion region for RF low power LNA. At this operating point, the measured performances for each LNA are reported in the Table 1. The inductively degenerated cascode have a gain of 8.8 dB and a noise figure of 3.3 dB for a power consumption of 400 µW. The current reused have a gain of 14.3 dB and a noise figure of 5 dB for a power consumption of 80 µW.

This section demonstrates an optimum biasing in the design of LNA according the FOM defined in (3). This optimum biasing occurs when the amplifying transistors operate in Moderate Inversion (MI) region. The values of the IC_{opt} as well as the magnitude of the FOM depend on the technology node and the circuit topology. Unlike the metrics reported so far, such as the $(g_m\ f_T/I_D)$, the FOM embeds the performances of the LNA, which can be further exploited to adjust and optimize the circuit characteristics. We propose in the next sections a comprehensive description of a design methodology based on this FOM, and dedicated to the sizing of low power LNA.

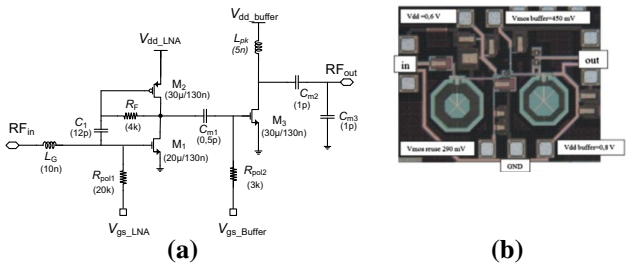


Fig. 6 Current-reused circuit: schematic (**a**) and picture (**b**)

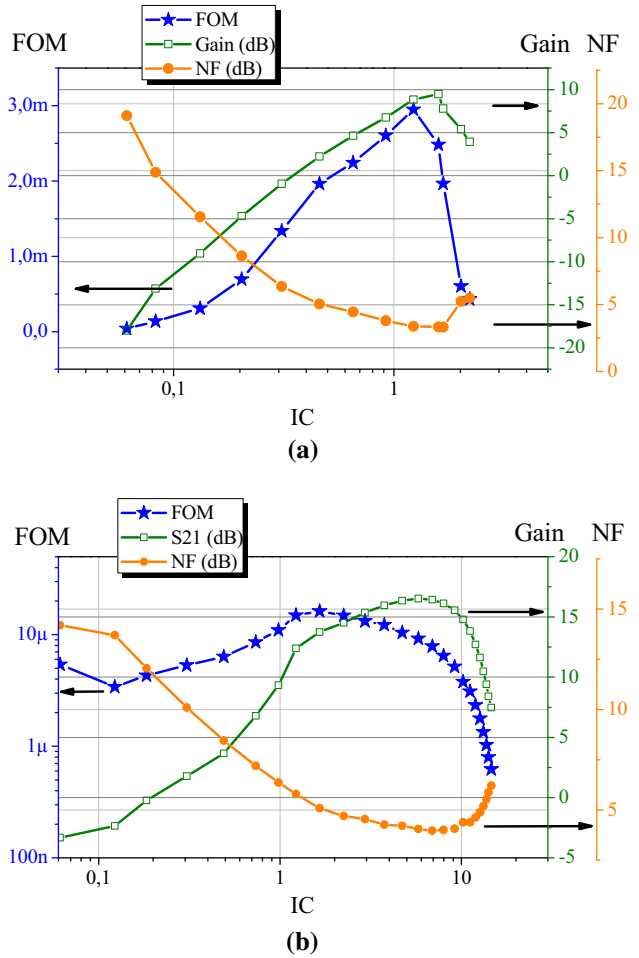


Fig. 7 Performances for Gain, Noise figure and FOM at 2.4 GHz for: Inductively degenerated cascode (**a**) and current-reused (**b**)

Table 1 Circuits performances at 2.4 GHz for the maximal FOM operating point

	Cascode	Current-reused
V_{DD}	0.5	0.6
P (µW)	400	80
S21 (dB)	8.8	14.3
S11 (dB)	−12	−11
S22 (dB)	−15	−13
NF (dB)	3.3	5

3 Design methodology based on the FOM

3.1 "Active part" design flow

The MOS transistor model allows to use only to three design parameters: the biasing with the IC and the size with the width (W) and the length (L). With this parameters, it is possible to define the circuit performances (4): the voltage gain (A_v), the noise figure (F_{min}) and the current (I_D).

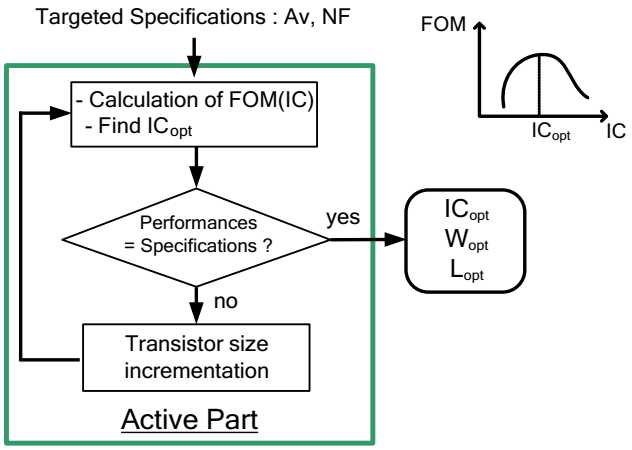


Fig. 8 "Active part" design flow with the FOM_{opt} method

$$\begin{cases} A_v = f_{Av}(W, L, IC) \\ F_{\min} = f_{\mathrm{Fmin}}(W, L, IC) \\ I_D = f_{Id}(W, L, IC) \end{cases} \quad (4)$$

The FOM calculation at (3) allows us to find the optimal biasing and the circuit performances (Sect. 2.2). This approach allows to realize a design methodology for the "Active Part" to finds the size and optimal biasing for transistor(s), represented in the Fig. 8. Two steps are required to find the "Active Part"; based on A_v and F_{min} specifications, the first step we find the optimum IC (IC_{opt}) calculating FOM. In the second step, we estimate the performances at fixed gate width (W) and length (L). The loop runs over these two steps, incrementing W and L, until the LNA characteristics meet the specifications. For a complete design flow, the input matching is added in the Sect. 4.

3.2 Method relevance

The method relevance is demonstrated by simulation for a capacitive common source in CMOS 28 nm (Fig. 2). The required performances are: a capacitive load of 100 fF, a frequency of 2.4 GHz, the noise figure must be below 1 dB and the voltage gain is constant at 10 dB. For a fixed length (L) of 40 nm, in Fig. 9 current and FOM are shown for different widths (W). In the same figure, the operating point of the method FOM_{opt} at IC_{opt} is obtained, according with the required performances. The method allows to work nearest the minimum current with a difference below 1 %. However, FOM_{opt} does not match with maximum FOM and the difference is 0.15 %: it is necessary to include weights in the FOM equation but we decide to keep a generic FOM formula. Our principal objective is not to

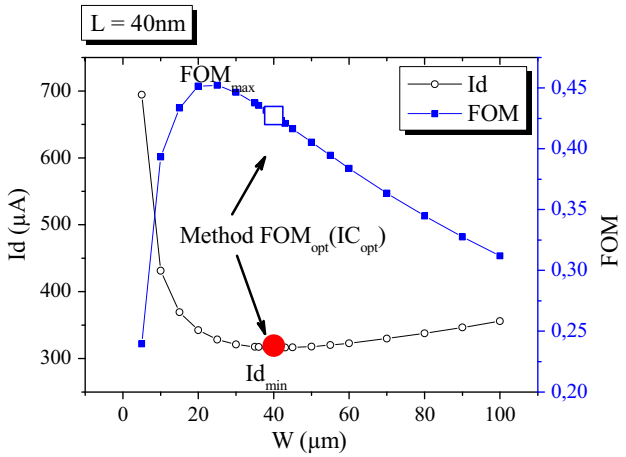


Fig. 9 Current and FOM variation function the width (W) and comparison with the FOM_{opt} method for a constant voltage gain (10 dB) and fixed length (L = 40 nm)

find the circuit with the best FOM but to respect the performances and have the lowest power consumption. FOM_{opt} method allows to find quickly the minimum current respecting the required performances.

For different gate lengths (Table 2) and constant gain, the method allows to obtain size and transistor biasing close to the minimum current configuration. Moreover, the inversion coefficient $IC_{opt}(FOM_{opt})$ obtained by the method is close to $IC(FOM_{max})$. However the method is not efficient in some cases: for the 30 nm gate length it has been observed a difference of 5 % between Id_{min} and $Id(FOM_{opt})$ and 22 % between FOM_{max} and FOM_{opt}. Anyway, the method can quickly size a circuit configuration close to the minimum current.

3.3 FOM evolution versus gate length

The minimum channel length is a parameter often used to increase the operating frequency and reduce the circuit consumption. However, reducing the gate length consequently decreases the maximum intrinsic gain. For advanced technologies and low power RF applications using the minimum length is not necessarily the best solution. For a capacitive load common source in CMOS 28 nm, the design method shown in Fig. 8 is applied to obtain: a voltage gain of 10 dB, a noise lower than 1 dB for the operating frequency of 2.4 GHz. The circuit is optimized for different gate lengths (L) and the simulation results are reported in Fig. 10. We observe that, for a constant gain, the minimum noise figure increases with the channel length. The FOM should decrease with the noise figure. However, it is observed that current decreases from gate length of 30–60 nm and then increases. This current variation induced a maximum FOM for a length of 40 nm.

We explain the current variation with the effect of velocity saturation and parasitic capacitances. The effect of the velocity saturation carrier generates a transconductance saturation in the strong inversion for advanced technologies. This phenomenon is represented by the coefficient λ_c [8], detailed in Sect. 4. We assume that there is a correlation between the a minimum current and the coefficient λ_c [8]. Evolution of λ_c compared to the $Id_{opt}(IC_{opt})$ method is shown in Fig. 11. Value of λ_c does not change linearly with the gate length (L), and its slope increases with gate length (L) decreasing. The relationship between λ_c and $Id_{opt}(IC_{opt})$ is not direct, but minimum current matches to the slope variation of λ_c. The increase of λ_c causes transconductance saturation, and consequently gain saturation. To keep a constant gain, it is necessary to increase the transconductance, so the current. From a gate length of 30–60 nm, current decreases according with the λ_c. For length higher than 60 nm, current increases because there are more parasitic capacitances: it is necessary to increase the current to keep a constant gain. It is necessary a trade-off between velocity saturation and parasitic capacitances to size gate length and minimize the current.

We compare different technologies to check if the minimum channel length is the best choice for advanced technologies in low power RF applications.

3.4 Technologies comparison

For circuits with same gain and similar noise figure, FOM maximization allows to decrease current consumption. The

Table 2 Numeric comparison: FOM_{opt} method versus best circuit performances

L (nm)	Id_{min} and $Id(FOM_{opt})$		FOM_{max} and FOM_{opt}		
	Difference (µA)	Relative difference (%)	FOM relative difference (%)	IC (FOM_{max}")	IC_{opt}
30	20	5	22	0.42	0.12
35	0.7	0.2	9.4	0.45	0.19
40	3	0.97	0.14	0.37	0.23
65	1.7	0.6	0.22	0.46	0.23
70	2	0.7	0.27	0.49	0.22

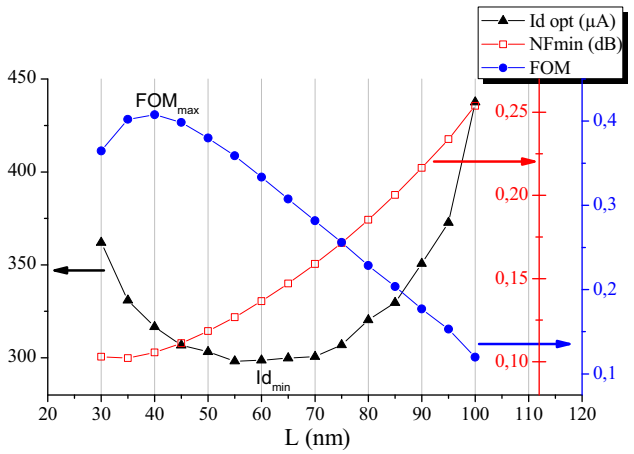


Fig. 10 FOM, NF_{min} and Id_{opt} at ICopt versus gate length (L) for a constant gain (10 dB)

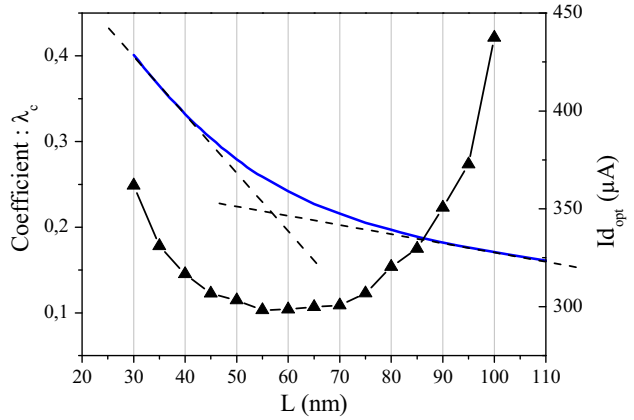


Fig. 11 Velocity saturation parameter λ_c and current evolution versus gate length

method is applied on different technologies and N-MOS transistors of STMicroelectronics: 28 nm-nfet, 28 nm-N Low Voltage Threshold (nlvt), 28 nm-N Super Low Voltage Threshold (nslvt), 65 nm-nlvt and 130 nm-nrfhsmos4.

The capacitive load common source topology is designed to obtain: a voltage gain of 10 dB with a noise figure lower than 1 dB at 2.4 GHz, for a load capacity of 100 fF. The method is applied for different gate lengths and the simulations results are shown in Figs. 12, 13 and 14.

In previous sections, we found that it exists an optimal gate length (L) to maximize the FOM. The same behavior is shown in Fig. 12 for the 28 and 65 nm technologies, but not for the 130 nm technology. For 28 and 65 nm technologies, the minimum length is not the best choice to design a low power RF LNA. For 28 nm CMOS, the optimal length is 40 nm and for the 65 nm CMOS is 75 nm. For 130 nm technology, the optimal length is the minimum length. The transistor transition frequency (f_T) has a strong impact on this phenomenon: 90 GHz for

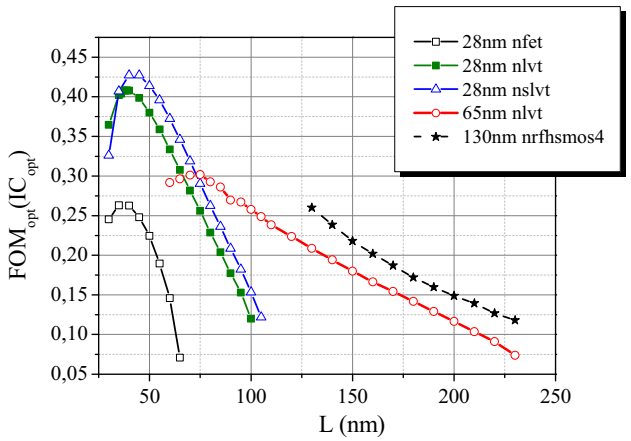


Fig. 12 FOM comparison versus length for different technologies at 2.4 GHz and a voltage gain of 10 dB

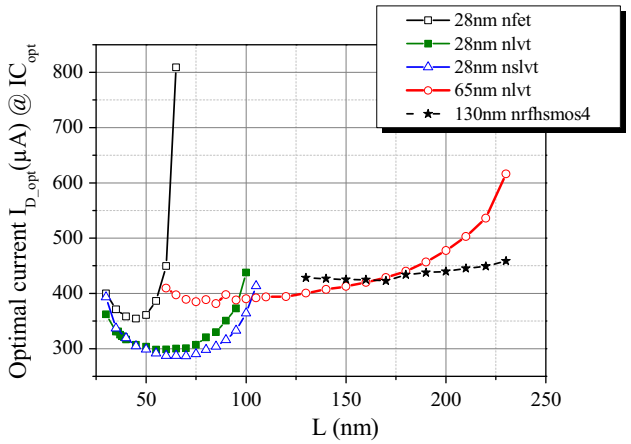


Fig. 13 Optimal current versus length for different technologies at 2.4 GHz and a voltage gain of 10 dB

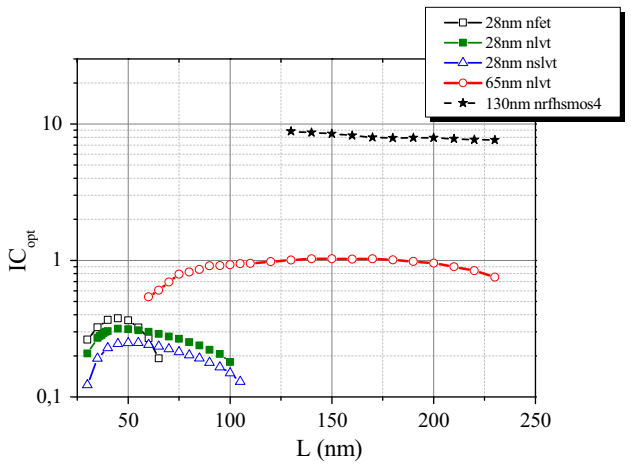


Fig. 14 Optimal Inversion coefficient versus gate length for different technologies at 2.4 GHz and voltage gain of 10 dB

130 nm, 180 GHz for the 65 nm and 350 GHz for the 28 nm.

Figure 12 highlights several behaviors:

- Technological progress allows to increase FOM, using the minimum gate length.
- FOM slopes depends on technologies: in 65 and 130 nm technologies slopes decrease similarly while in 28 nm slope decreases faster.
- In 28 nm CMOS, "lvt" and "slvt" have a FOM twice higher than the "fet". Threshold voltage reduction is clearly favorable to the FOM.

The I_{Dopt} evolution for different gate lengths is shown in Fig. 13. Some behaviors can be observed:

- A minimum current is highlighted according to gate length particularly on 28 nm CMOS.
- Transistor length for the minimum current does not match to the maximum FOM. For the 28 nm-nlvt, the maximum FOM is for L = 40 nm while the minimum current is for L = 55 nm.
- In Fig. 12, the FOM of 65 nm-nlvt is higher than 28 nm-nlvt for L = 75 nm. Figure 13 shows that the current of 65 nm-nlvt becomes lower than 28 nm-nlvt for L ≥ 100 nm.

Figure 14 shows IC for different gate lengths at the FOM_{opt}. The three technologies are biased in moderate inversion (0.1 < IC < 10). Technological progress allows to reduce the optimal IC. The circuit in 130 nm CMOS works at the limit of strong inversion and circuits in 28 nm CMOS are closed to weak inversion.

In order to develop the method analytically, we normalize transistor as described in the next section.

4 Transistor normalization

The literature proposes different models of MOS transistor [9–11] whose complexity usually increases with the operating frequency. For applications below 10 GHz, a RC model provides enough accuracy. A small-signal model, including noise sources, is proposed in Fig. 15. The model is composed by transconductance (g_m) and conductance (g_{ds}) for the active part, and by capacitances and a resistance for the passive part.

4.1 Transconductance & conductance

The transistor transconductance g_m is defined in (5) [8] and it depends on the IC with G_m(IC, λ_c), transistor size (W, L) and the technologic parameter $I_{spec\diamond}$. In deep-submicron technology (L < 200 nm), velocity-saturation increases the transconductance saturation and is represented by the coefficient λ_c, which depends on the technology and gate length (L). For a long channel, the coefficient λ_c is null.

$$g_m = \frac{Gm(IC,\lambda_c).I_{spec\diamond}}{U_T}.\frac{W}{L} = f_{g_m}(\boldsymbol{W},\boldsymbol{L},\boldsymbol{IC})$$
$$\text{with } Gm(IC,\lambda_c) = \frac{1}{n}\frac{\sqrt{(IC.\lambda_c+1)^2+4.IC}-1}{\lambda_c(IC.\lambda_c+1)+2} \quad (5)$$

The transistor's output conductance g_{ds} (6) depends on the drain current and the early voltage V_M [3]. It is simplified and represented by the IC, the size (W, L), $I_{spec\diamond}$ and an empirical technological parameter α_{Gds}.

$$g_{ds} = \frac{I_D}{V_M} \cong \frac{I_D}{\alpha_{Gds}.L} = \frac{IC.I_{spec\diamond}}{\alpha_{Gds}.L}.{}^{W}\!/_{L} = f_{g_{ds}}(\boldsymbol{W},\boldsymbol{L},\boldsymbol{IC}) \quad (6)$$

The analytic expressions of g_m (5) and g_{ds} (6) are compared with electrical simulations for 28 nm CMOS technology of STMicroelectronics in Fig. 16 for a capacitive common source (W = 6 µm and L = 30 nm). The model of g_m (5), accounting for velocity saturation λ_c, is validated in all operating regions. The conductance model (6), not including λ_c, fits the simulation results in weak and moderate inversion regions. The analytic g_{ds} overestimates the simulated g_{ds} in the SI region (IC >10). However, the effect of this is minor on the design methodology and circuit optimization, as shown in Sect. 2.

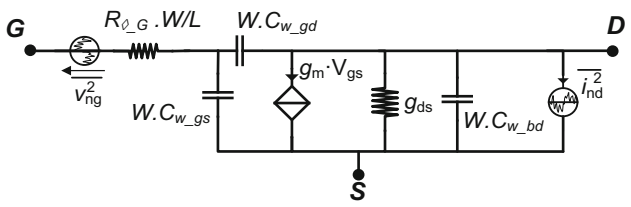


Fig. 15 Small signal model including noise sources

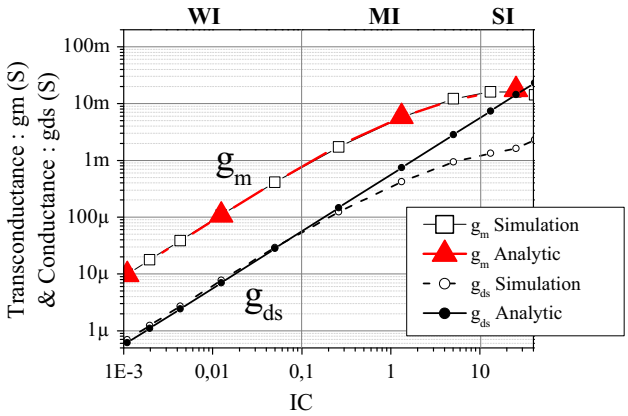
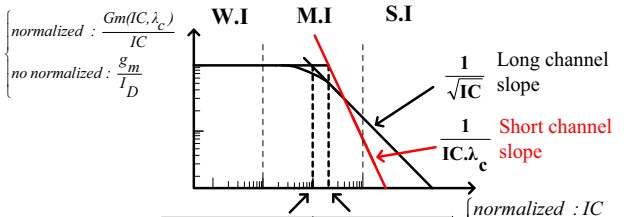


Fig. 16 Transconductance and Conductance versus IC



	Long channel	Short channel
Normalized	$IC = 1$	$IC = 1/\lambda_c$
No normalized	$I_{spec} = I_D$	$\lambda_c = \frac{I_{spec\diamond}.W}{I_D.L}$

Fig. 17 Extraction of $I_{spec\diamond}$ and λ_c

According (5) and (6), only 3 parameters are required to described g_m and g_{ds}: $I_{spec\diamond}$, λ_c and α_{Gds}. Our design methodology is persistently based on these characteristics. These parameters can be extracted throughout two DC simulations of each transistor type.

The first simulation provides a plot of ($I_D - V_{GS}$) to find g_m for $I_{spec\diamond}$ and λ_c extraction. According Fig. 17, the representation of the g_m to drain current ratio, namely current efficiency, over the drain current, I_D, exhibits two trends: a constant in WI region and a negative slope in SI region. The intersection of the representative asymptotes of WI and SI regions occurs when I_D equals I_{spec} for long channel and depends of λ_c for short channel. $I_{spec\diamond}$ will be further deduced with (2) and λ_c with Fig. 17. The parameters λ_c depends to gate length (L).

The second simulation is the characteristics ($I_D - V_{DS}$) to find g_{ds}; α_{Gds} is deduced from (6) for a fixed size and current.

The g_m and g_{ds} parameters are solely dependent on the size (W, L) and the IC for a given technology ($I_{spec\diamond}$,λ_c, α_{Gds}).

4.2 Parasitic transistor capacitances and resistances

The parasitic capacitances and resistances depend on technological parameters C_w and $R_\diamond$, respectively, and are normalized to the transistor size W and L according to (7) and (8).

$$C = W.C_w = \boldsymbol{f_C}(\boldsymbol{W}) \tag{7}$$

$$R = \frac{R_\diamond.W}{L} = \boldsymbol{f_R}(\boldsymbol{W},\boldsymbol{L}) \tag{8}$$

To extract the capacitances and resistances, a S-parameter simulation is used on a single transistor at fixed size (W, L) in order to work out the admittances Y_{ij} [1] (Eq. 9).

if $2.\pi.f.R_G.(C_{GS} + C_{GD} + C_{GB}) << 1$:

$$\begin{cases} C_{GDw} \cong -\dfrac{imag(Y_{12})}{2.\pi.f}.\dfrac{1}{W} \\ C_{BDw} \cong \dfrac{imag(Y_{22})}{2.\pi.f}.\dfrac{1}{W} - C_{GDw} \\ C_{GSw} + C_{GBw} \cong \dfrac{imag(Y_{11})}{2.\pi.f}.\dfrac{1}{W} - C_{GDw} \\ R_{G.\diamondsuit} \cong \dfrac{real(Y_{11})}{[imag(Y_{11})]^2}.\dfrac{L}{W} \end{cases} \tag{9}$$

For noise analysis, the gate resistance noise $\overline{v_{ng}^2}$ and the channel noise $\overline{i_{nd}^2}$ (10) are considered accordingly [3].

$$\begin{cases} \overline{i_{nd}^2} = 4.k.T.g_{ds} \\ \overline{v_{ng}^2} = 4.k.T.R_G = 4.k.T\dfrac{R_{G.\diamondsuit}.W}{L} \end{cases} \tag{10}$$

In next section we combine the transistor normalization and the bias with the FOM method to define an analytical design methodology.

5 LNA design methodology base on the FOM_{OPT} and transistor normalization

5.1 Complete design flow

In previous section, we have shown that only three design parameters, IC, W and L, are needed to represent MOS transistor. Consequently with the same parameters, it is possible to define the LNA performance (11): voltage gain (A_v), noise figure (F_{min}), current (I_D) and input impedance (Z_{IN}).

$$\begin{cases} A_v = f_{Av}(W,L,IC) \\ F_{\min} = f_{\mathrm{Fmin}}(W,L,IC) \\ I_D = f_{Id}(W,L,IC) \\ Z_{IN} = f_{Z_{IN}}(W_{opt},L_{opt},IC_{opt},\text{Input Passives}) \end{cases} \tag{11}$$

The FOM calculation at (3) allows to find the optimal biasing and the LNA performances (Sect. 2). With this approach we can realize a complete design methodology including the input matching represented in Fig. 18. This methodology has two parts; the "Active Part" finds the size and optimal biasing for transistor(s) and the "Passive Part" finds the input matching.

The "Active Part", explained in Sect. 3.1, is based on A_v and F_{min} specifications. In the first step FOM calculation provides the optimum IC (IC_{opt}). In the second step, we

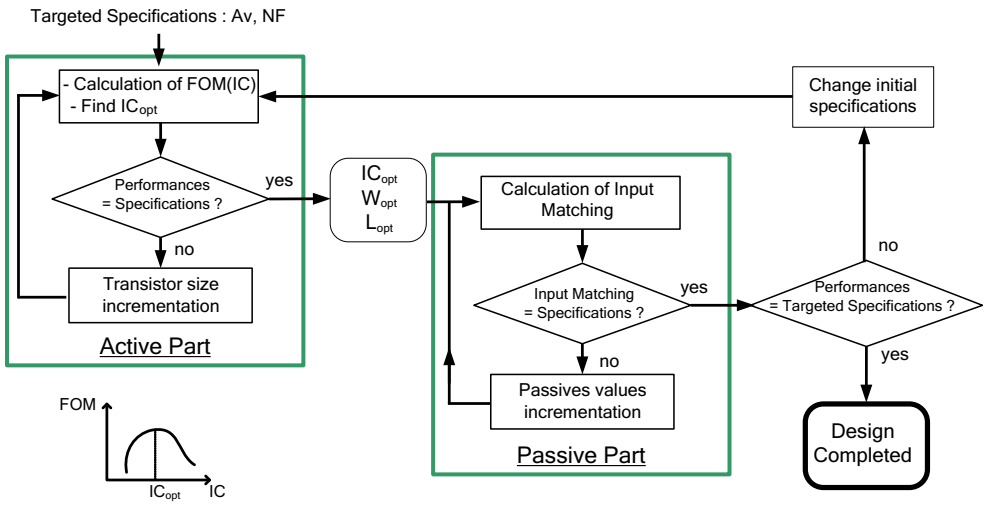


Fig. 18 Complete design flow

check the performances (A_v, F_{min}) for IC_{opt} and fixed gate width (W) and length (L). The loop runs over these two steps, incrementing W and L, until the LNA characteristics respect the specifications. In the most of the case, use a smaller length (L) allows to reduce the current consumption. Consequently, the width (W) is increment the first than a minimum size to a maximum size define by the layout size. Then, the length (L) is incremented for a small size, the width (W) redo a loop in the range of the minimum to the maximum size.

For a complete design flow, the input matching is also designed with the "input passives". In the "Passive Part", the input matching is designed with the parameters previously obtained in the "Active part": IC_{opt}, W_{opt}, L_{opt},. If the LNA performances do not respect the targeted specifications, the initial specifications are adjusted.

In next paragraph the circuit performances (A_v, F_{min}, I_D, Z_{IN}) are described in terms of circuit components: g_m, g_{ds}, C_{gs}, C_{gd}, C_{bd}, R_G, "input passives" in order to make an analytical methodology.

5.2 Application on a current reused circuit

The current reused circuit that we implemented in 28 nm CMOS is shown in Fig. 19. The LNA core is composed of two transistors, one NMOS (M_1) and PMOS (M_2) using the same bias current. The transistor M_1 is biased with the voltage V_{gs_LNA}. The transistor M_2 is self-biased by the feedback resistance R_F and the current of M_1. The input matching is achieved with a capacitive divider setting the real part at 50 ohms. It is composed by: the parasitic capacitances and the transconductances of the LNA transistors (M_1 and M_2), the load capacitance (input capacitance of transistor M_3) and a tunable capacitance C_{in}. The imaginary part is set to zero by the series inductance L_G.

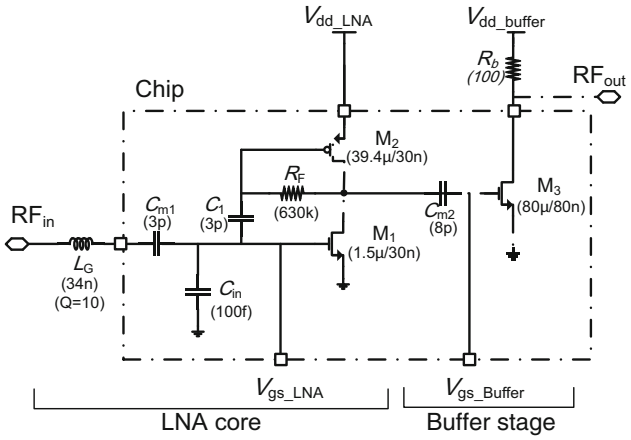


Fig. 19 Current reused circuit in CMOS 28 nm

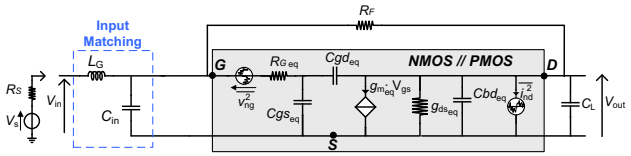


Fig. 20 Small signal schema of the current reused LNA

The output matching is achieved with a resistive common source (M_3). Polarizations are separated to control each stage independently.

In Fig. 20, the analytical description of the circuit is made from the small signal schema. Current reused topology model can be represented as two capacitive common sources in parallel: NMOS and PMOS. The transistors M_1 and M_2 are grouped (12) through equivalent components, denoted *eq*.

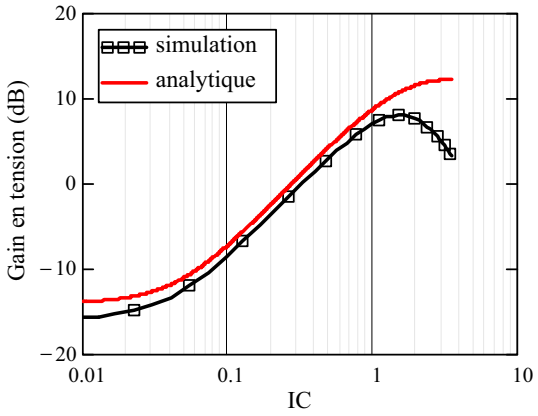


Fig. 21 Voltage gain versus IC at 2.4 GHz: analytic and simulation

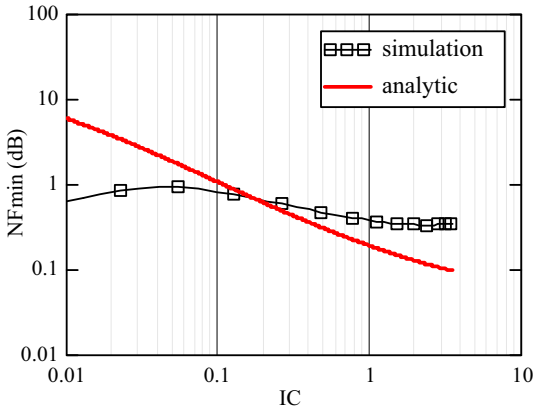


Fig. 22 Minimum noise figure versus IC at 2.4 GHz: analytic and simulation

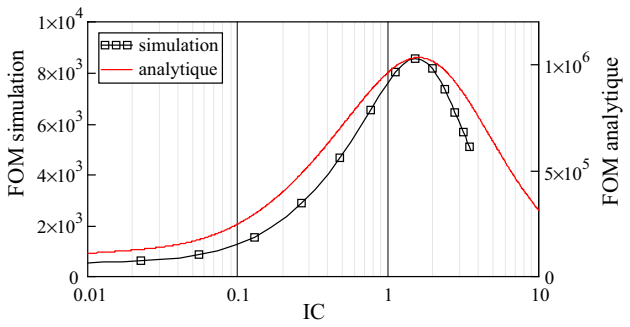


Fig. 23 FOM versus IC at 2.4 GHz: analytic and simulation

$$
\begin{aligned}
g_{m\_eq} &= g_{m\_1}(IC_1, W_1, L_1) + g_{m\_2}(IC_2, W_2, L_2)\\
g_{ds\_eq} &= g_{ds\_1}(IC_1, W_1, L_1) + g_{ds\_2}(IC_2, W_2, L_2)\\
C_{GS\_eq} &= C_{GSw\_NMOS}.W_1 + C_{GSw\_PMOS}.W_2\\
C_{GD\_eq} &= C_{GDw\_NMOS}.W_1 + C_{GDw\_PMOS}.W_2\\
C_{BD\_eq} &= C_{BDw\_NMOS}.W_1 + C_{BDw\_PMOS}.W_2\\
C_L &\approx C_{GS\_3}\\
R_{G\_eq} &= R_{G\diamondsuit\_NMOS}.{}^{W_1}\!/_{L_1} + R_{G\diamondsuit\_PMOS}.{}^{W_2}\!/_{L_2} \qquad (12)
\end{aligned}
$$

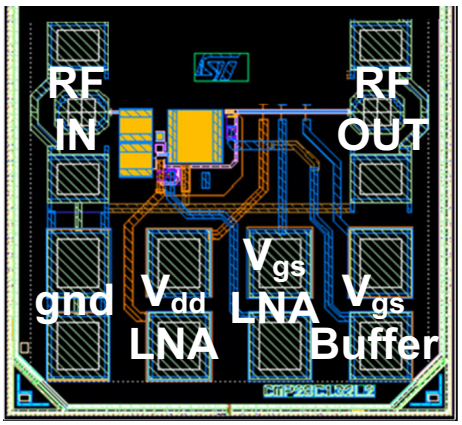
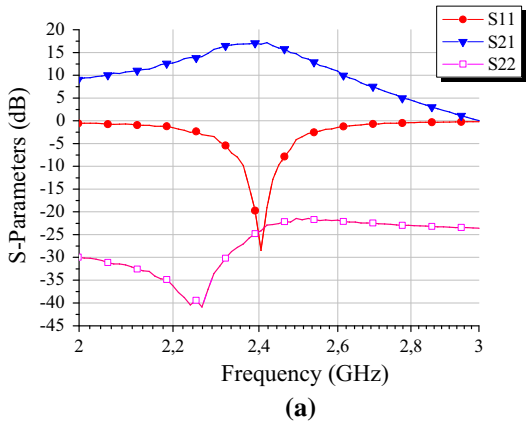
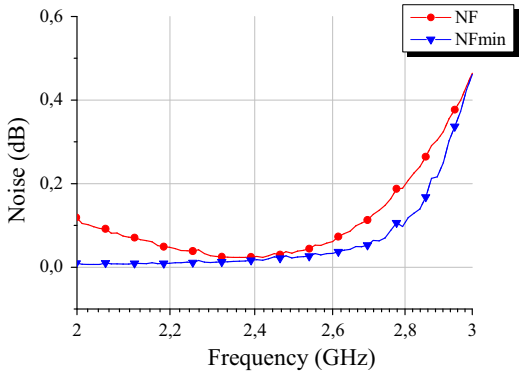


Fig. 24 Snapshot of current reuse



(a)



(b)

Fig. 25 S-parameters (**a**) and noise figure (**b**) simulations results at 15 μW

The LNA core voltage gain (A_v), without input matching, is described in Eq. (13). To simplify A_v equation we distinguish the output impedance Z_{out} and the feedback impedance Z_{eq_fb} in Eqs. (14) and (15). The gate resistance (R_G) impact is negligible.

$$|A_v| \cong \left|\frac{(Y_{eq\_fb} - g_{m\_eq}).Z_{out}}{1 + Z_{out}.Y_{eq\_fb}}\right| \qquad (13)$$

Table 3 Current-reused simulation at 2.4 GHz in 28 nm CMOS

P µW	S_{21} dB	Av dB	S_{11} dB	S_{22} dB	NF dB	ICP1 dBm	IIP3 dBm
15	17	17	−19	−24	0.25	−23	−18

$$Z_{out} = \frac{1}{g_{ds\_eq} + j\omega(C_{BD\_eq} + C_L)} \tag{14}$$

$$Y_{eq\_fb} = \frac{1}{Z_{eq\_fb}} = \frac{1}{R_F} + j\omega.C_{GD\_eq} \tag{15}$$

The extraction of the 28 nm CMOS technologic parameters allows to compare in Fig. 21, the analytical gain Eq. (14) and gain simulation. The analytical gain behavior fits perfectly to the simulation up to IC = 1. Then, simulated gain decreases rapidly. We have observed in Fig. 15, that conductance (g_{ds}) analytical model diverges for IC>1.

The circuit noise, generated by gate resistors, the inductance (L_G) and the channel conduction require noise matching. The minimum noise figure (F_{min}) of the circuit is shown in Eq. (16). The influence of the feedback resistor (R_F) can be skipped if its value is important. The input matching network introduces a Q-factor (Q_π) or passive gain. The minimum noise factor is often calculated with only the transconductance. However the use of voltage gain allows to take into account the complete transfer function. Analytical minimum noise figure is compared to the simulation in Fig. 22. We observe that analytical noise equation and simulation are the same behavior differing by 0.4 dB for 0.01 > IC > 1. The noise factor diverges due to g_{ds}.

$$F_{\min} = \frac{\left(g_{ds\_eq} + 1/R_F\right). + g_{m\_eq}^2\left(R_{//} + R_S.Q_\pi^2\right)}{g_{m\_eq}^2.R_S.Q_\pi^2} \tag{16}$$

We compare the analytical and simulation of FOM in Fig. 23. The shapes of the curves are close. The maximum analytical and simulated FOM appears in moderate inversion, for an IC = 1.2 and an IC = 1.5 respectively. These curves show that the circuit design by analytical method is relevant and reliable.

The circuit input matching (Z_{in}) is represented in Eq. (17).

$$Z_{in} = \mathrm{Re}(Z_{in}) + j.\mathrm{Im}(Z_{in})$$

$$\text{with} \begin{cases} \mathrm{Re}(Z_{in}) = \dfrac{\frac{1+gm_{eq}.Z_{eq\_out}}{Z_{eq\_fb}+Z_{eq\_out}}}{\left(\frac{1+gm_{eq}.Z_{eq\_out}}{Z_{eq\_fb}+Z_{eq\_out}}\right)^2 + \left(\omega.(C_{in}+C_{GS\_eq})\right)^2} \\ \mathrm{Im}(Z_{in}) = \dfrac{\omega.L_G - \omega.(C_{in}+C_{GS\_eq})}{\left(\frac{1+gm_{eq}.Z_{eq\_out}}{Z_{eq\_fb}+Z_{eq\_out}}\right)^2 + \left(\omega.(C_{in}+C_{GS\_eq})\right)^2} \end{cases} \tag{17}$$

The LNA is designed to operate at 2.4 GHz for 0.5 V supply; it is expected to achieve more than 15 dB gain and a NF lower than 1 dB. The design flow allows to get a current of 30 µA and to size the components as shown in Fig. 19. The inversion coefficients (IC_{opt}) at FOM_{opt} are 0.5 (MI) for the NMOS (M_1) and 0.02 (WI) for the PMOS (M_2). The biasing in MI for the two transistors should be applied; however a trade-off between the parasitic capacitance and carrier mobility put the PMOS transistor in WI which decreases the global current consumption.

LNA is implemented in 28 nm STMicroelectronics CMOS technology and cover a surface of 0.39 mm^2, including the PADs without inductance (Fig. 24). Simulations are realized with a supply voltage of 0.5 V and a current of 30 µA (15 µW), excluding the 50 Ω buffer (Fig. 25; Table 3). The gain represented by S_{21} reaches a maximum of 17 dB at 2.4 GHz; therefore the current-reused topology provides a large voltage gain with a low voltage supply. The fine tuning of input matching gives an S_{11} of −19 dB at 2.4 GHz. The output matching has no resonance which allows a broadband use with a S_{22} under −20 dB. The noise reaches a value of 0.25 dB at 2.4 GHz. The very low current degrades the linearity: ICP1 is −23 dBm and IIP3 is −18 dBm.

6 Conclusion

A new approach of design methodology for RF low power LNA is presented in this paper. The method efficiency comes from the association of circuit's performances (A_v, F_{min}, I_D) in low power FOM calculation and the optimum polarization. The local optimum bias in moderate inversion is confirmed with the measurements of two RF LNAs in CMOS 130 nm. This approach allows to size the core of the LNA and secondly to set the matching. This method is used to compare different technologies: we observe that for advanced technologies, such as 65 nm CMOS or 28 nm CMOS, the use of the minimum gate length is not the best choice to reduce current consumption. Using analytical representations of the circuits from the transistor normalization and the IC, it is possible to size the components automatically. This automation is a major asset to quickly design a circuit, modifying the performances or the CMOS technology. Finally, this design methodology is used to design a 2.4 GHz LNA in 28 nm CMOS technology of STMicroelectronics.

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