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MIXED SIGNAL LETTER

Two advanced energy-back SAR ADC architectures with 99.21 and 99.37 % reduction in switching energy

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Abstract This letter presents novel energy-efficient switching schemes for a successive approximation register analog-to-digital converter. The new switch method consumes no switching energy in the first three comparison cycles. The average switching energy is reduced by 99.21 and 99.37 % for the signal-independent and signal-dependent common mode voltage at the comparator, respectively. A 75 % reduction in the total capacitance over the conventional scheme is also achieved. The variation of the common mode voltage at the comparator input in the proposed architecture is 50 % less than in other low power switching schemes.

Keywords Analog-to-digital conversion (ADC) · Successive approximation register (SAR) ADC · Switching scheme · Switching energy

1 Introduction

Due to low power consumption, successive approximation register (SAR) analog-to-digital converters (ADCs) are preferred for low- and medium-speed applications, such as sensors readout [1], biomedical implants [2], or physical measurements [3]. In the conventional SAR ADC with a capacitive DAC, the energy drawn from the reference source during the capacitor switching plays an important role in the overall power consumption. Recently, several novel switching schemes have been developed to reduce that energy [4–8].

Taking the conventional SAR switching procedure as the reference with the zero power reduction, the monotonic switching technique [4] claims to achieve an 81.26 % reduction. In that procedure capacitors of bottom and upper arrays are only switched in one direction and the common mode voltage at the comparator input monotonically decreases from $V_{ref}/2$ to the least significant bit (LSB) voltage. The varying of the common-mode voltage at the comparator input can degrade the performance of the ADC because of the common mode dependent offset voltage. Thus, the additional techniques like [4, 9] should be applied to the comparator design.

The V_{cm}-based monotonic capacitor switching scheme [10] achieves an 87.1 % reduction in the switching energy by the use of the second reference voltage V_{cm} equal to $V_{ref}/2$, also used in all following schemes.

The tri-level scheme [7] reduces the switching energy by 96.89 %. Because of the use of single sided switching (only bottom or upper capacitor arrays are switched during conversion), the common-mode voltage at the comparator varies from the $V_{ref}/2$ to the $V_{ip} \pm V_{LSB}$ or $V_{in} \pm V_{LSB}$ (initially sampled voltage values of upper or bottom capacitor arrays). Thus, the common-mode voltage at the comparator input is input signal-dependent, which can cause an even more complicated comparator design as for monotonic switching to eliminate the harmonic distortion of the output signal. The same common-mode voltage consideration can be applied to the the hybrid capacitor [6] switching scheme, which reduces the switching energy by 98.83 %

The energy-back scheme [5] reduces the switching energy by 98.4 %. The common mode voltage in that scheme is independent of the input signal value.

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There are also some interesting non-symmetrical switching architectures [11, 12], which require additional comparison cycles, or switching schemes which utilize the splitting of DAC capacitors [8, 13], or multi-reference switching scheme [14, 15].

In this letter, a new switching scheme based on the energy-back scheme [5] is presented. When used for the first three decisions it saves 99.22 % of the switching energy, while providing a signal-independent common voltage level at the comparator input. Using the scheme to decide the first four bits saves 99.37 % of the switching energy, but the common voltage level at the comparator input becomes slightly dependent on the input signal. The proposed switching architecture also has a lower variation of the common voltage level.

2 The switching scheme

2.1 Energy-back switching scheme

The energy back switching scheme proposed by [5] is based on two ideas. First, during the sampling phase the bottom plate of the MSB capacitor is connected to the ground, while all other capacitors bottom plates are connected to V_{ref}(Cp $= [0, 1, 1 \ldots 1]$, Cn $= [0, 1, 1 \ldots 1]$, where Cp and Cn are upper and bottom capacitor arrays of the differential DAC, respectively). That gives the possibility to save energy during the first capacitor switch in the SAR algorithm. That is illustrated in Fig. 1.

Secondly, the energy back switching scheme takes advantage of the fact, that switching of the (MSB-1) from V_{ref} to the ground is equivalent regarding the output voltage to the switching of the MSB capacitor from V_{ref} to $V_{ref}/2$. This idea is illustrated in Fig. 2. The switching energy can be divided into two parts:

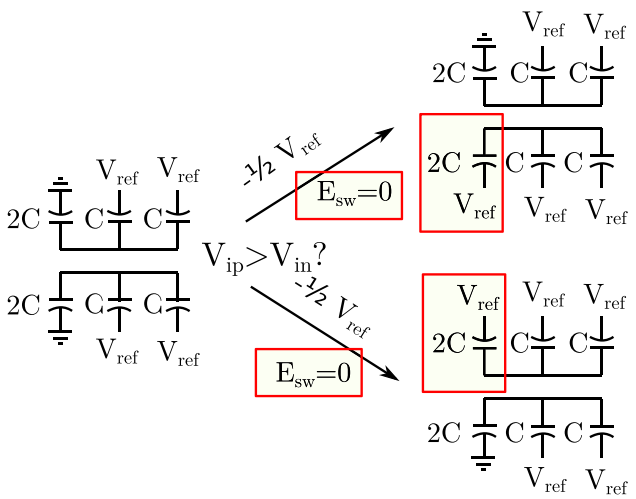

Fig. 1 Energy savings by first switch in enery back scheme

$$E_{sw} = E_{sw}^{V_{ref}/2} + E_{sw}^{V_{ref}},$$

where $E_{sw}^{V_{ref}/2}$ is the energy drawn from $V_{ref}/2$ and $E_{sw}^{V_{ref}}$ is the energy drawn from V_{ref}:

$$\begin{aligned} E_{sw}^{V_{ref}/2} &= -2(V_{ref}/2)(Q_1 - Q_0) \\ &= -2C(V_{ref}/2)(V_x - V_{ref}/4 - V_{ref}/2 - (V_x - V_{ref})) \\ &= -CV_{ref}^2/4, \\ E_{sw}^{V_{ref}} &= -2(V_{ref})(Q_1 - Q_0) \\ &= -2C(V_{ref})(V_x - V_{ref}/4 - V_{ref} - (V_x - V_{ref})) \\ &= CV_{ref}^2/2, \end{aligned}$$

The complete switching energy is given by:

$$\begin{aligned} E_{sw} &= E_{sw}^{V_{ref}/2} + E_{sw}^{V_{ref}} \\ &= CV_{ref}^2/2 - CV_{ref}^2/4 \\ &= CV_{ref}^2/4 \end{aligned}$$

Based on these two ideas the energy back switching scheme algorithm flowchart can be depicted as shown in Fig. 3. After the first switching, the i-th capacitor is connected to the ground if (i-1)th capacitor is already connected to ground, otherwise the (i-1) capacitor should be connected to $V_{ref}/2$.

2.2 Advanced energy back switching schemes

In order to overcome the charging from the reference source of the largest most-significant bit (MSB) capacitor after the first comparison cycle, the energy-back scheme [5] uses the approach shown on Fig. 1. Unfortunately, this approach does not eliminate the energy consuming charge of the next (MSB-1) capacitor. Unlike [5], in the proposed scheme, two capacitors are switched after the first comparison (Fig. 4). If the voltage at the upper plates of the upper capacitor array (V_P) is larger than at the

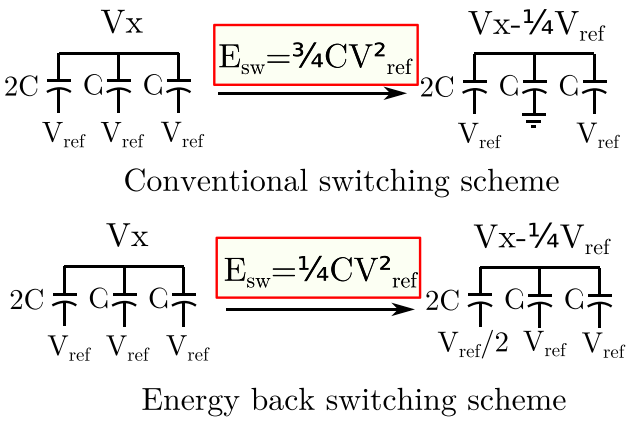

Fig. 2 Energy savings in enery back scheme

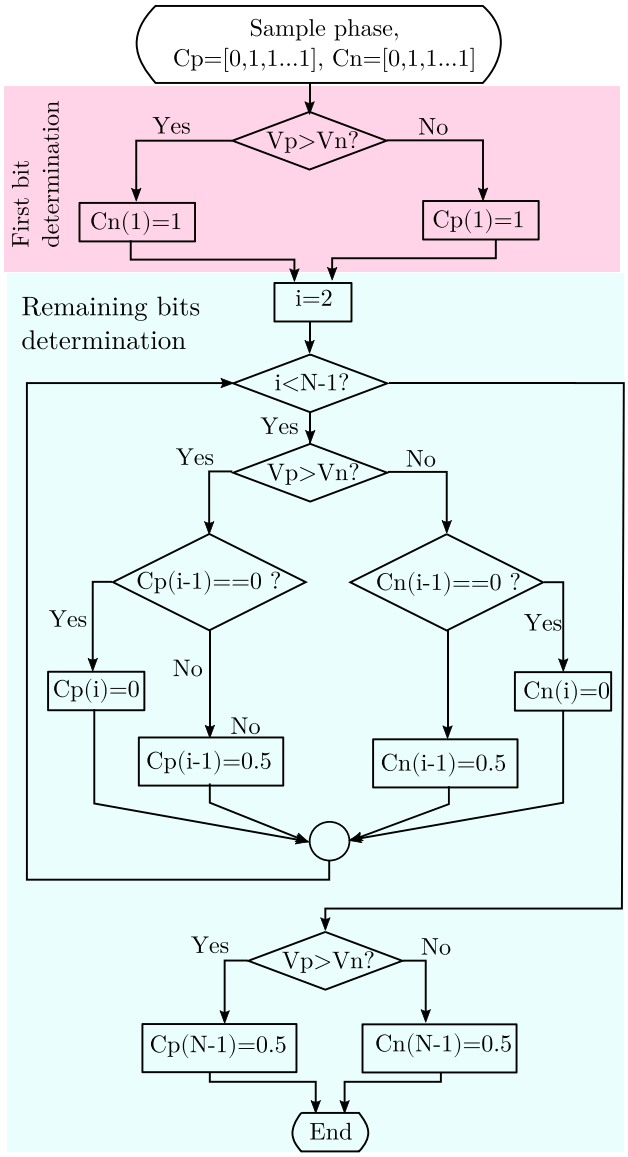

Fig. 3 Energy back switching scheme flowchart. Vp and Vn are voltages at the *top* plate of the *upper* capacitor array and at the *top* plate of the *bottom* capacitor array, respectively. Cn(i) = 0.5 should be read as "the *bottom* plate of the ith capacator of the *bottom* array is connected to $V_{ref}/2$". i is the cycle variable, N is the number of bits in ADC

upper plates of the bottom capacitor array (V_N), the (MSB-1) capacitor of the upper part of the array is switched from V_{ref} to the ground, which results in $0.25CV_{ref}^2$ switching energy. At the same time the MSB capacitor of the bottom part of the array is switched from V_{ref} to $V_{ref}/2$, which results in $-0.25CV_{ref}^2$ switching energy. Thus, the overall switching energy of that operation is equal to zero, because the energy, which charges the upper array, is drawn from the bottom array and not from the reference. Furthermore, that switching does not change the common mode voltage at the comparator input $(V_N + V_P)/2$.

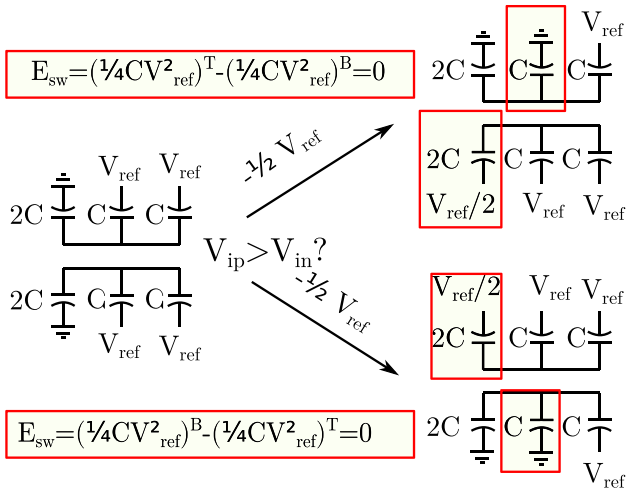

Fig. 4 First switching in proposed schemes

Now, the second switching can also be performed without any energy consumption. As it can be seen in Fig. 4, bottom plates of the upper and bottom capacitors arrays can be connected as $[0, 0, 1 \ldots 1]$ or $[0.5, 1, 1 \ldots 1]$. Depending of the comparison result of V_P and V_N voltages, one should add or subtract $0.25V_{ref}$ from the differential voltage $(V_P - V_N)$. As shown in Fig. 5 both operations can be carried out without any energy consumption. Compared to the hybrid capacitor switching scheme in [6], which also obtains the zero-energy second switching, only one capacitor is switched. The common mode signal $(V_N + V_P)/2$ goes up to $5V_{ref}/8$ at this point, independent of the initial input signal value. If the input signal independent common mode voltage at the comparator input is sufficient for the design, the conventional energy back switching scheme should be used for further switchings (proposed switching scheme I).

The switching energy can be lowered even more, but at the cost of a slight input signal-dependence on common voltage at the comparator input (proposed switching scheme II). The illustration of switchings for 5-bit ADC is shown in Fig. 6. In this figure both switching schemes are shown. For the proposed I conventional energy back

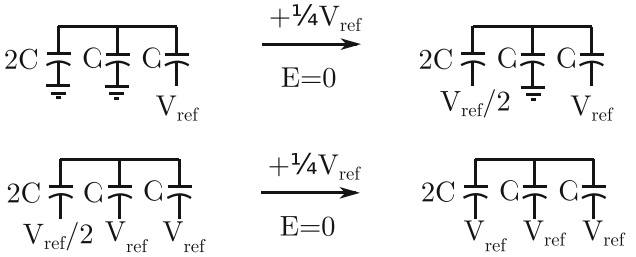

Fig. 5 Second switching options in proposed schemes

switching scheme should be used after switching to the states A,B,C,D (from 3rd switching). In proposed II conventional energy back switching scheme is also used for half of the switching options for 3rd switching. But for the other half more efficient power efficient switching from $[x, 0, 1, \ldots 1]$ to $[x, 0.5, 1 \ldots 1]$ is proposed, where $x = \{0,0.5\}$.

The flowchart of the proposed schemes is given in Fig. 7.

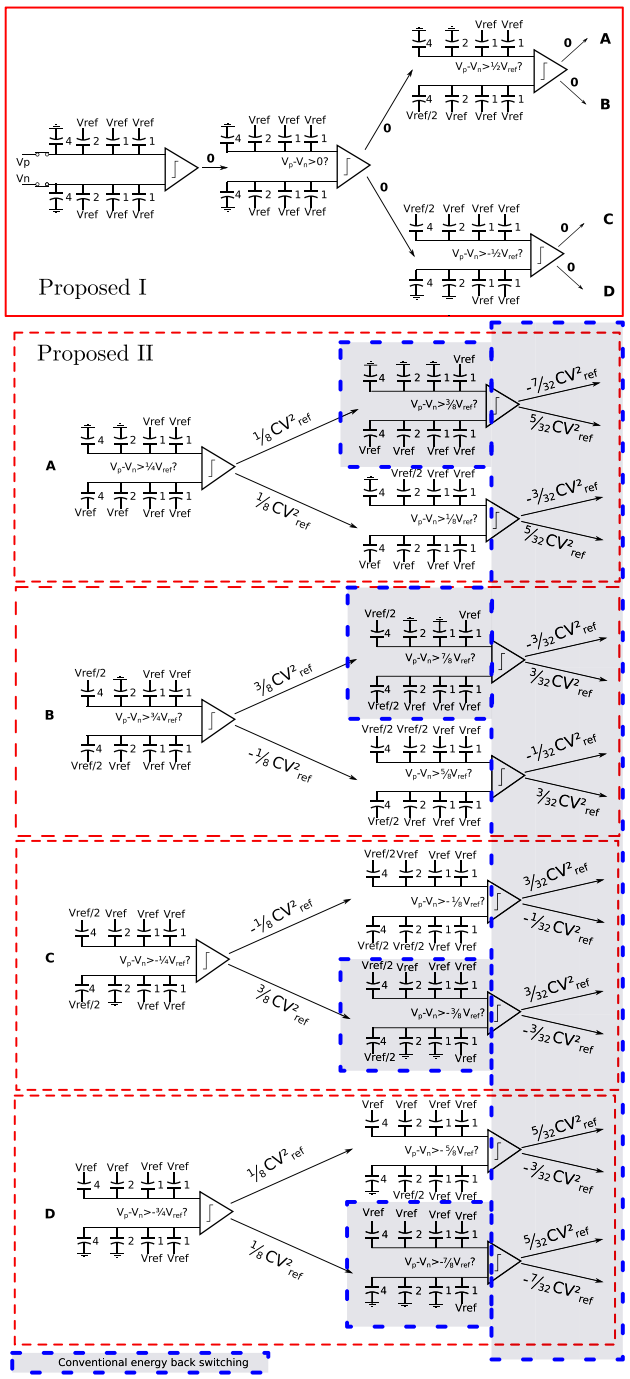

Fig. 6 Proposed switching schemes example for 5-bit ADC

3 Switching energy

3.1 Negative energy

As shown in Fig. 6 during some steps the switching energy becomes negative. The negative energy arising at some DAC switchings is a matter of dispute. Introduced by [5, 16] it was defined as the energy given back from the DAC to voltage sources. But, the possibility to use that energy is questionable. Some authors, like [17], do not take it into

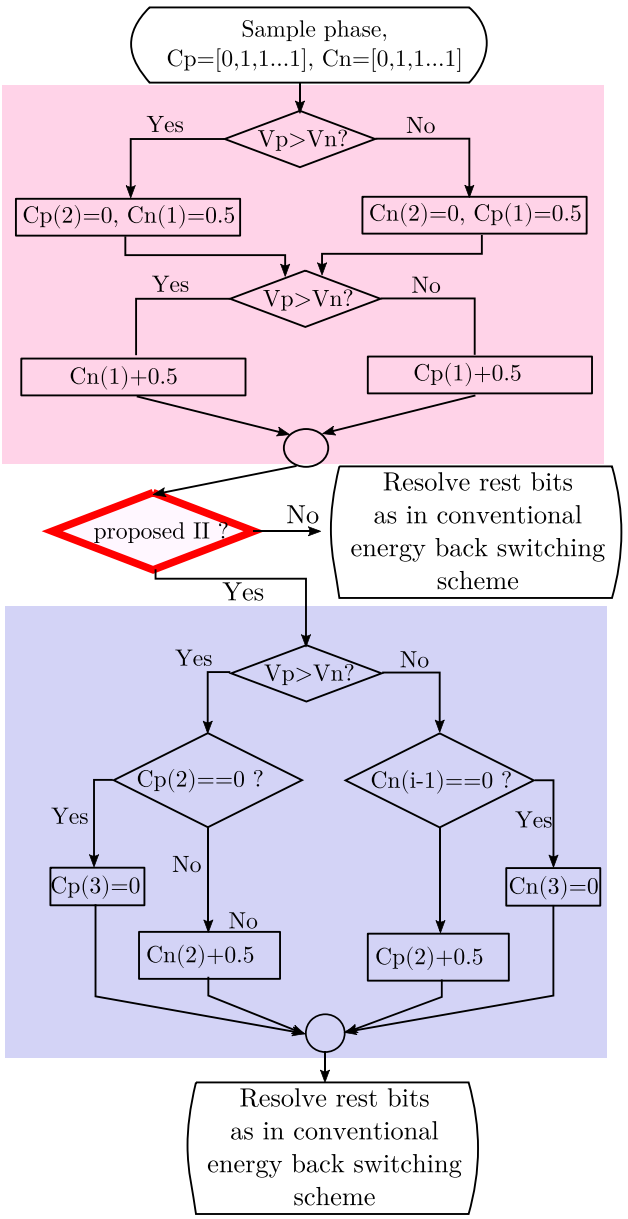

Fig. 7 Flowchart of the proposed switching schemes. Cn(i) + 0.5 means, that that capacitor should be connected to $V_{ref}/2$, if it was previously connected to ground, or to V_{ref}, if it was previously connected to $V_{ref}/2$

account by average power consumption calculations (the negative energy is considered as zero by them).

But, in reality the effect of the negative energy has to be considered with the reference source configuration. The typical voltage reference configuration for the SAR ADC is shown in Fig. 8. If the DAC is disconnected from the voltage buffer, constant current will flow through the load resistors of the operational amplifier. If the capacitors in the DAC are charging from the reference, the additional charge current is drawn from the power rail (Vdd). On the contrary if the capacitors in the DAC are discharging, the discharge current will also flow through the load resistors, thus effectively decreasing the current drawn from the power rail. This consideration shows, that if the load discharge current is lower than the bias current of voltage reference, the negative energy can be added to the average energy calculations. On the other hand, if the bias current value is lower, the negative energy can not be added.

Another opportunity arises, if by the switching of upper and lower capacitor plates the switching energies for upper and lower plates have opposite signs (second switching in the proposed scheme). In that case the current needed to charge the capacitor is drawn from the capacitor on the opposite plate, and that negative energy can be added to power consumption calculations without any additional conductions (if the switching of opposite plates is synchronous).

The behavior of the previously published switching schemes and the proposed scheme was behaviorally simulated in MATLAB. The switching energy comparison for the 10-bit SAR ADC is shown in Fig. 9, in which the switching scheme with the input signal-independent common mode voltage at the comparator is denoted as the "proposed I", and the scheme with the input signal-dependent common mode voltage at the comparator, as the "proposed II". It can be seen that for a small signal input $V_{in} \in (\frac{-V_{ref}}{4}, \frac{V_{ref}}{4})$ the average switching energy for the "proposed II" is even fully negative. The average switching energies are equal to 10.66 and 8.63 CV_{ref}^2, respectively, the latter result is the best among recently published ones.

The switching energy plot, which does not take into account the negative switching energy pushed into the reference from the capacitor array is shown in Fig. 10. The average switching energies for "proposed I" and "proposed II" switching architectures are equal to 12.89 and 11.12 CV_{ref}^2, respectively.

3.2 Reset energy

After completing the evaluation of all the bits the capacitors arrays should be reset to the initial state $[0, 1, 1 \ldots 1]$. That operation also consumes energy, which is not considered in most of the published switching schemes [5, 17–19]. Although it can be significant for the overall power consumption. For example, for the switchback switching method [20], its value achieves $255CV_{ref}^2$, while the switching energy is only $127.5CV_{ref}^2$. It should be noted, that that energy only arises if the bottom plates of the capacitors are connected to different potentials during the sampling phase. And, thus it is always zero in switching schemes, which reset all capacitors bottom plates to one node during the sampling phase [21].

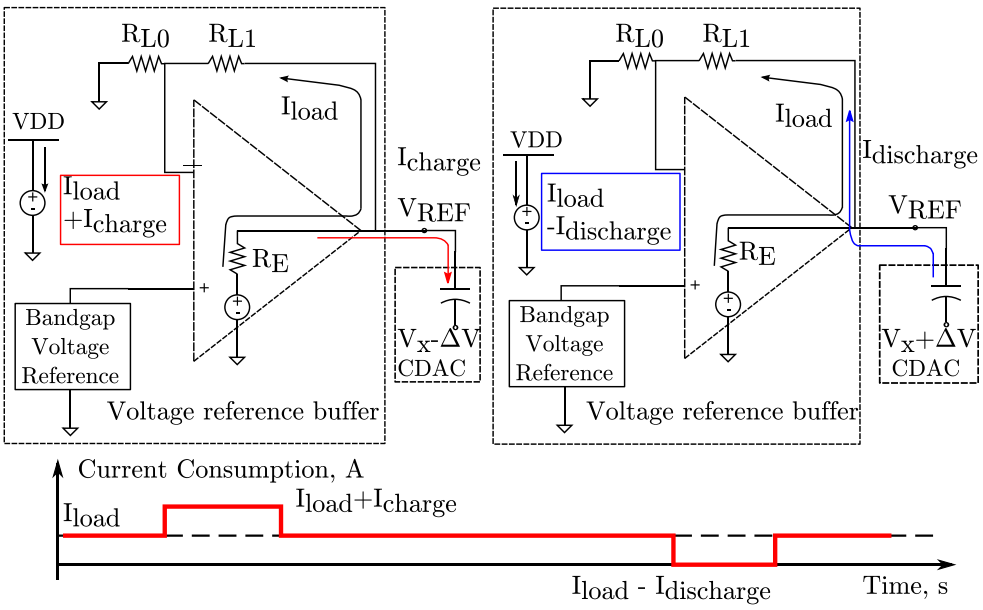

Fig. 8 Current consumption savings of reference buffer by energy back algorithm

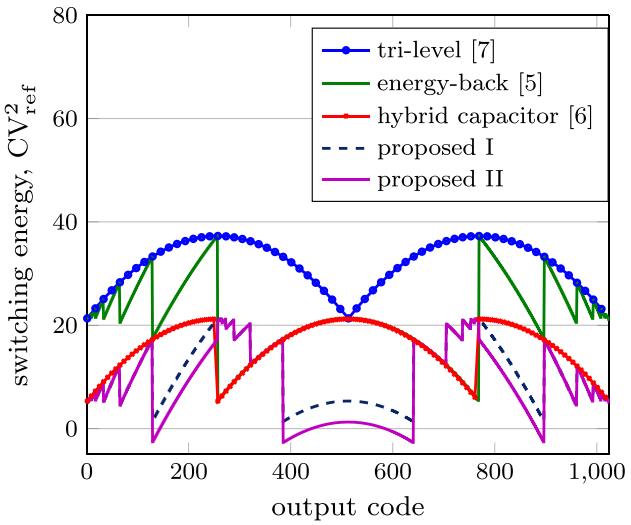

Fig. 9 Switching energy comparison for 10-bit SAR ADC

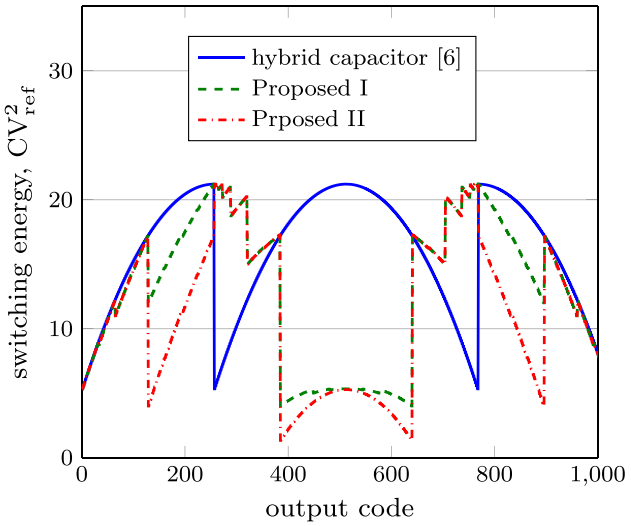

Fig. 10 Switching energy comparison for 10-bit SAR ADC. The negative switching energy pushed into the reference from the capacitor array not taken into account

The reset energy is dependent on the state of the capacitor matrix at the end of the conversion phase. The behavioral simulation of the reset energy for the energy-back [5] and the proposed switching schemes was accomplished in Matlab. Simulation results are shown in Fig. 11. The average reset energy for the 10-bit SAR ADC for the energy back scheme is 95.75 CV^2_{ref}, and 111.75 and 127.5 CV^2_{ref}, for proposed I and proposed II, respectively. Thus, the overall power consumption in the proposed switching schemes is not lower than for the energy back switching scheme. But the proposed schemes provide lower common mode voltage variation, which is considered in the next section.

4 Common mode voltage

The main advantage over other energy saving schemes of energy-back scheme is signal independence of the common mode voltage of the DAC. The proposed I scheme keeps this advantage, while proposed II scheme adds slight dependence on the input voltage.

The variation of the common mode voltage of the DAC is lower for both proposed schemes – $V_{ref}/8$ and $3V_{ref}/16$ against $V_{ref}/4$ in the energy-back scheme. Furthermore the common mode voltage begins to vary only after two first cycles, introducing less errors in the first comparisons. For the proposed I the common mode voltage at the comparator input is independent from the input code. Similar to conventional energy-back procedure, it starts at $V_{ref}/2$, goes up to $5V_{ref}/8$ in the third cycle (instead of the $3V_{ref}/4$ in the second cycle in the conventional energy-back scheme), and gradually converges towards $V_{ref}/2$. In the case of switching further, as shown in Fig. 6, to resolve the fourth bit, for $V_{in} \in \left[-V_{ref}, \frac{-3V_{ref}}{4}\right) \cup \left[\frac{-V_{ref}}{2}, \frac{-V_{ref}}{4}\right) \cup \left[\frac{V_{ref}}{4}, \frac{V_{ref}}{2}\right) \cup \left[\frac{3V_{ref}}{4}, V_{ref}\right)$ the common mode voltage at the comparator input behaves as in the previous case, because the conventional energy back switchings are used her.

For $V_{in} \in \left[\frac{-3V_{ref}}{4}, \frac{-V_{ref}}{2}\right) \cup \left[-\frac{V_{ref}}{4}, \frac{V_{ref}}{4}\right) \cup \left[\frac{V_{ref}}{2}, \frac{3V_{ref}}{4}\right)$ it starts at $V_{ref}/2$, goes up to $5V_{ref}/8$ in the second cycle, then up to $\frac{11V_{ref}}{16}$ in the third, and gradually converges to $5V_{ref}/8$.

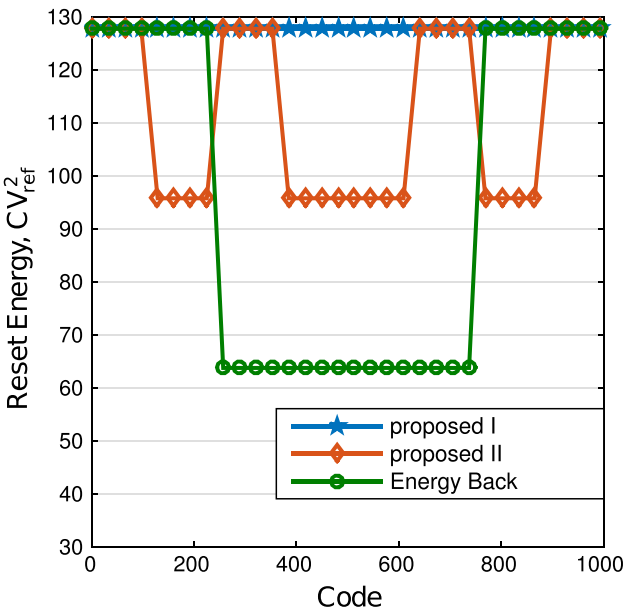

Fig. 11 Reset energy for energy-back and proposed switching schemes for 10-bit SAR

The waveforms of the proposed switching procedure in comparison with the conventional energy back scheme are shown in Fig. 12.

5 Capacitors mismatch and parasitics influence on the SAR ADC characteristics

Based on the method provided in [1, 19] the sensitivity of maximal DNL and INL to the capacitors value variation is given by:

$$\sigma_{DNL,MAX} = \frac{\sqrt{2^N}\sigma_{C_0}}{C_0} LSB,$$

$$\sigma_{INL,MAX} = \frac{\sqrt{2^{N-1}}\sigma_{C_0}}{C_0} LSB,$$

where σ_{C_0} is the standard deviation of the unit capacitor value.

To simulate the influence of capacitors non-idealities random Gauss variations with standard deviation of 1 % were added to capacitors values and 50,000 Monte-Carlo runs were performed for both proposed switching schemes. The simulation results are shown in Fig. 13. It can be seen that although the maximal DNL and INL values are equal for both schemes, the distribution of errors is quite different. The proposed II scheme has more linear transfer function in the mid-scale, which can be important for small signal applications.

Implying the common centroid layout of the capacitor matrix lowers the parasitics capacitors values and their influence on the SAR ADC characteristics [22, 23]. The effect of the parasitics parallel to the matrix capacitors, arising from the metal routes, can be handled as a part of the capacitors mismatch, which was considered previously in this section. The other two types of parasitics are denoted in Fig. 14 as C_{pt} and C_{pb}, for the top plate parasitic capacitor common for matrix capacitors and bottom plate

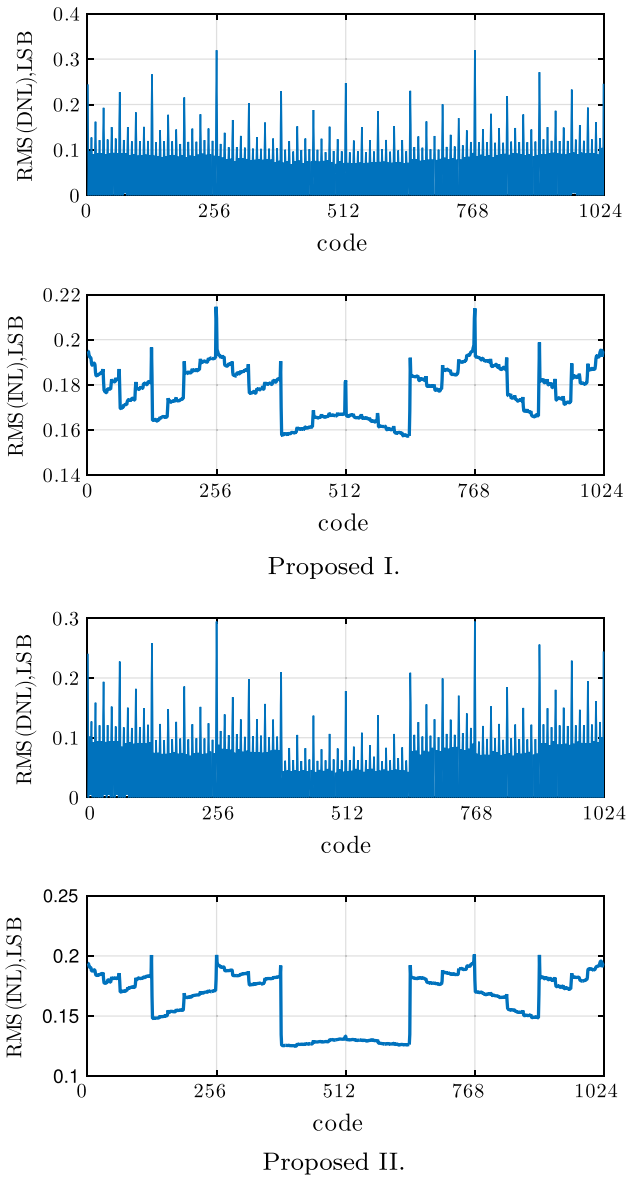

Fig. 13 RMS values of INL and DNL based on 50,000 Monte-Carlo runs

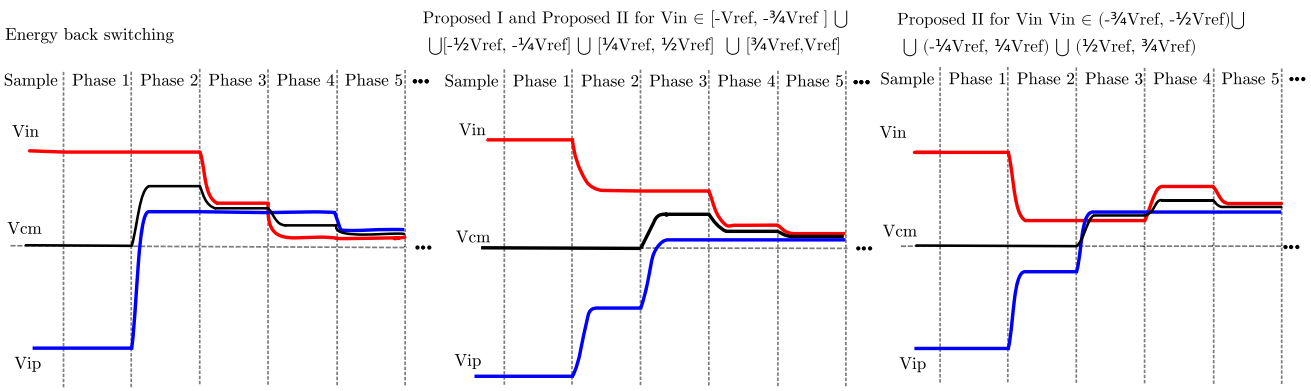

Fig. 12 DAC output waveforms

parasitic capacitors, respectively. The output voltage of the capacitive DAC can be expressed as:

$$V_{out} = V_p - V_n = \frac{\sum_{i=1}^{N-2} 2^i C_0 b_i^p + C_0 b_0^p}{C_{total}} - \frac{\sum_{i=1}^{N-2} 2^i C_0 b_i^n + C_0 b_0^n}{C_{total}},$$

where $b_i^{p,n} = \{0, 0.5, 1\}$ represents the voltage value at the bottom plate of the matrix capacitor, C_{total} is the sum of all matrix capacitors in the upper or bottom part of the array. The C_{pb} capacitors of the bottom and upper parts of the array should be equal with proper common centroid layout design. In that case their value affects only the C_{total}, and introduces the gain error not affecting the linearity of the DAC.

The C_{bp} capacitors do not have direct influence on the linearity of the DAC, only affecting the settling speed of the DAC.

The parasitic capacitors should also be charged during the conversion cycle, which raises the power consumption of the matrix. The analysis of additional power consumption on account of parasitic capacitors for different switching schemes was done in [18]. The comparison of additional power consumption of the proposed scheme with previously published ones is given in Table 1. The difference in calculated energy with [18] for the energy back switching scheme arises because the negative energy was zeroed in [18]. The graphic in Fig. 15 represents the code dependence

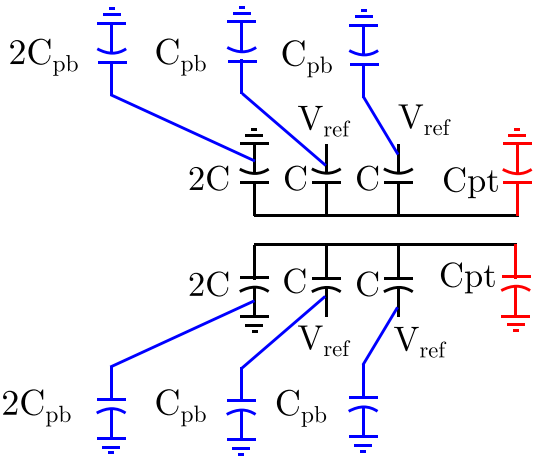

Fig. 14 Parasitics capacitors of the capacitor matrix

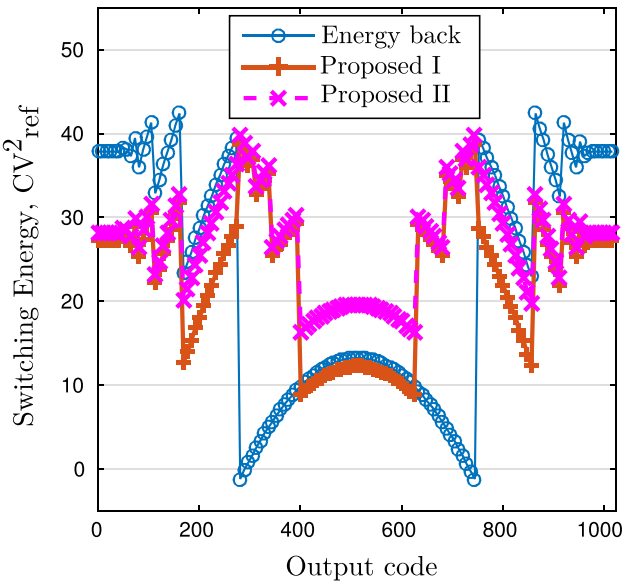

Fig. 15 Switching energy comparison for 10-bit SAR ADC in presence of parasitics ($C_{pt} = 0.1C_{total}$, $C_{pb} = 0.15C0$)

Table 2 Mapped gates comparison for proposed schemes for 10 bit ADC

Switching method	Mapped gates	D-triggers
Monotonic [4]	160	35
Energy back [5]	289	47
Proposed I	285	47
Proposed II	283	47

Table 1 Additional switching energy because of parasitics

Switching method	Switching energy (CV_{ref}^2), $C_{pt=0}$, $C_{pb} = 0$	Switching energy (CV_{ref}^2), $C_{pt} = 0.1C_{total}$, $C_{pb} = 0.15C0$
Conventional	1363.3	1686.1[a]
Monotonic [4]	255.5	255.5[a]
Tri-level [7]	42.4	69.0[a]
Energy back [5]	21.3	33.15
Vcm based monotonic [10]	31.9	56.3[a]
Proposed I	10.66	23.13
Proposed II	8.63	27.04

[a] Simulation data from [18]

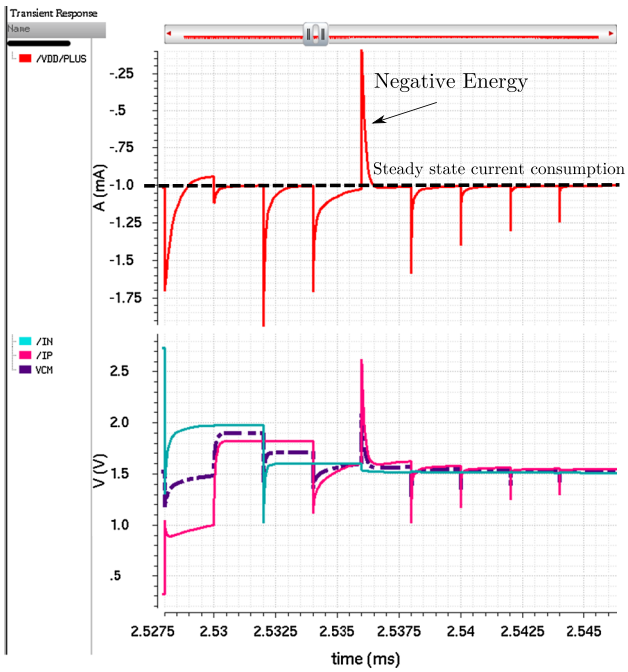

Fig. 16 SPICE simulation of the current consumption savings

of switching energy in the presence of parasitics ($C_{pt} = 0.1C_{total}$, $C_{pb} = 0.15C_0$). It can be seen, that the presence of parasitic capacitor C_{pb} even lowers the plot at some codes, at the cost of gain error and, as a consequence, the decrease in the possible input signal range.

6 SPICE simulation

In order to prove the behavioral Matlab modeling the provident switching schemes were simulated in Cadence Spectre circuit simulator. The ideal Verilog-A models were used for comparators and DAC capacitor switches. The switch connects the bottom plate of the capacitor to one of the voltages $\{0, V_{ref}/2, V_{ref}\}$ based on its 2-bit control signal value. The SAR algorithm was also implemented in Verilog. The SAR is designed as a simple state machine which can be implemented in the conventional way, for example, as a ring counter to define the current state and the code register to store the output code [24]. In that case the switches in the capacitor matrix can be controlled by the combinational logic based on multiplexers. For the proposed switching

Table 3 Comparison of different switching methods for a 10-bit SAR ADC

Switching method	Switching energy (CV_{ref}^2)	Energy savings by switching (%)	Common mode—input signal dependence	Maximum common mode variation	Reset energy (CV_{ref}^2)
Conventional	1363.3	0	No	0	0
Monotonic [4]	255.5	81.2	No	$V_{ref}/2$	0
Tri-level [7]	42.4	96.98	Yes	$V_{ref}/4$	0
Energy back [5]	21.3	98.43	No	$V_{ref}/4$	95.75[a]
Hybrid capacitor [6]	15.88	98.83	Yes	$V_{ref}/2$	N.A.[b]
Merged capacitor [8]	42.67 (noise-matched)	96.9	Yes	$V_{ref}/4$	N.A.[b]
	10.67 (linearity-matched)	99.21			
Tong and Zhang [17]	−0.135 (with neg. energy)	100	Slightly	$V_{ref}/2$	N.A.[b]
	15.8 (no neg. energy)	98.8			
Zhu and Liang [2]	15.8	98.84	No	$V_{ref}/4$	31.2
Proposed I	10.66	99.22	No	$V_{ref}/8$	127.5
Proposed II	8.63	99.37	Slightly	$3V_{ref}/16$	111.75
Proposed I (no neg. energy)	12.89	99.05	No	$V_{ref}/8$	127.5
Proposed II (no neg. energy)	11.12	99.18	Slightly	$3V_{ref}/16$	111.75

[a] Not provident by authors, estimation made in this paper according to the behavioral simulation

[b] The reset energy calculations are not provident by authors

scheme, as for the conventional energy back switching scheme, the control signal at the ith switch is dependent not only on the ith comparison result but also on the state of the $(i-1)$th switch. To estimate the potential complicity of the logic implementation the proposed SAR register logic was synthesized with the Cadence RTL compiler using the AMS 0.35 μm digital cells library, which will potentially be used for the implementing of the proposed SAR. The comparison of the number of the mapped gates for the proposed schemes for 10 bit ADC is given in Table 2. Comparing to the conventional energy back scheme proposed schemes do not lead to the more complicated implementation of the logic part. The monotonic switching procedure is more effective in means of digital control logic complicity because it does not need any information of the previous decision to make the current one.

An example of waveforms on the top plates of capacitor array is given in Fig. 16, the current consumption of the reference configured, as shown in Fig. 8, is also shown. The negative energy peak at the 3th matrix switching is shown. The negative energy lowers the current consumption under the steady-state level.

7 Conclusion

A novel energy-efficient advanced energy-back switching scheme is presented. The quantitative comparison with the previously published schemes is given in Table 3. The scheme saves 99.21 and 99.37 % energy, compared with the conventional technique, for the signal-independent and signal-dependent common mode voltages at the comparator, respectively. The new switching method is used for the first 3 or 4 bits, and the [5] for the remainder. Like [5, 6], the proposed switching scheme also reduces the overall area for the capacitive DAC by a factor of four. Besides the best energy efficiency among published SAR ADC switching architectures the provident architecture can simplify the comparator design, because of the twice lower variation of the common mode voltage at the comparator input among published SAR ADC switching architectures.

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References

1. Zhu, Z., Qiu, Z., Liu, M., & Ding, R. (2015). A 6-to-10-bit 0.5 V-to-0.9 V reconfigurable 2 MS/s power scalable SAR ADC in 0.18 n++ CMOS. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *62*, 689–696.
2. Zhu, Z., & Liang, Y. (2015). A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18-um CMOS for medical implant devices. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *62*, 2167–2176.
3. Bocharov, Y. I., Butuzov, V., & Simakov, A. (2015). A multichannel analog-to-digital converter of signals of silicon photomultiplier arrays. *Instruments and Experimental Techniques*, *58*(5), 623–630.
4. Liu, C.-C., Chang, S.-J., Huang, G.-Y., & Lin, Y.-Z. (2010). A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. *IEEE Journal of Solid-State Circuits*, *45*, 731–740.
5. Sanyal, A., & Sun, N. (2013). SAR ADC architecture with 98 % reduction in switching energy over conventional scheme. *Electronics Letters*, *49*, 248–250.
6. Xie, L., Wen, G., Liu, J., & Wang, Y. (2014). Energy-efficient hybrid capacitor switching scheme for SAR ADC. *Electronics Letters*, *50*, 22–23.
7. Yuan, C., & Lam, Y. (2012). Low-energy and area-efficient tri-level switching scheme for SAR ADC. *Electronics Letters*, *48*, 482–483.
8. Srinivasan, S., & Balsara, P. (2014). Energy-efficient sub-DAC merging scheme for variable resolution SAR ADC. *Electronics Letters*, *50*, 1421–1423.
9. Wei, L., Duona, L., Fengcheng, M., Jiaqi, Y., Libin, Y., Lin, H., et al. (2014). A 0.6 V 10 bit 1 MS/s monotonic switching SAR ADC with common mode stabilizer in 0.13 μm CMOS. *Journal of Semiconductors*, *35*(5), 055006.
10. Zhu, Z., Xiao, Y., & Song, X. (2013). VCM-based monotonic capacitor switching scheme for SAR ADC. *Electronics Letters*, *49*, 327–329.
11. Song, H., & Lee, M. (2014). Asymmetric monotonic switching scheme for energy-efficient SAR ADCs. *IEICE Electronics Express*, *11*(12), 20140345–20140345.
12. Anand, T., Chaturvedi, V., & Amrutur, B. (2010). Energy efficient asymmetric binary search switching technique for SAR ADC. *Electronics letters*, *46*(22), 1487–1488.
13. Wang, H., Zhu, Z., & Ding, R. (2015). Energy-efficient and area-efficient tri-level floating capacitor switching scheme for SAR ADC. *Analog Integrated Circuits and Signal Processing*, *85*(2), 373–377.
14. Wang, H., & Zhu, Z. (2015). Energy-efficient and area-efficient switching scheme based on multi-reference for SAR ADC. *IEICE Electronics Express*, *12*(4), 20141182–20141182.
15. Tong, X., Zhang, W., & Li, F. (2014). Low-energy and area-efficient switching scheme for SAR A/D converter. *Analog Integrated Circuits and Signal Processing*, *80*(1), 153–157.
16. Sanyal, A., & Sun, N. (2014). An energy-efficient low frequency-dependence switching technique for SAR ADCs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *61*, 294–298.
17. Tong, X., & Zhang, Y. (2015). 98.8 % Switching energy reduction in SAR ADC for bioelectronics application. *Electronics Letters*, *51*(14), 1052–1054.
18. Tong, X., & Ghovanloo, M. (2015). Energy-efficient switching scheme in SAR ADC for biomedical electronics. *Electronics Letters*, *51*(9), 676–678.
19. Liang, Y., Zhu, Z., & Ding, R. (2015). SAR ADC architecture with 98.8 % reduction in switching energy over conventional scheme. *Analog Integrated Circuits and Signal Processing*, *84*(1), 89–96.
20. Huang, G.-Y., Chang, S.-J., Liu, C.-C., & Lin, Y.-Z. (2013). 10-bit 30-MS/s SAR ADC using a switchback switching method. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *21*, 584–588.
21. Ding, Z., Bai, W., & Zhu, Z. (2016). Trade-off between energy and linearity switching scheme for SAR ADC. *Analog Integrated Circuits and Signal Processing*, *86*(1), 121–125.
22. Lin, M.-H., He, Y.-T., Hsiao, V.-H., Chang, R.-G., & Lee, S.-Y. (2013). Common-centroid capacitor layout generation

considering device matching and parasitic minimization. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *32*, 991–1002.
23. Bocharov, Y., & Butuzov, V. (2015). A low-power ASIC containing 10 analog-to-digital converters and buffer memory. In *2015 International Siberian conference on control and communications (SIBCON)* (pp. 1–3).
24. Anderson, T. (1972). Optimum control logic for successive approximation analog-to-digital converters. *Deep Space Network Progress Report*, *13*, 168–176.

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