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A review of state-of-the-art and proposal for high frequency inductive step-down DC–DC converter in advanced CMOS

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Abstract This paper reviews the state-of-the-art of high switching frequency, integrated DC–DC converters and presents the main trade-offs and challenges emerging from this review. Various converter structures (1-phase buck, 2-phase buck, 2-phase coupled buck and 3-level converter) are then discussed and analyzed through simulation from a losses point-of-view. Considering the review, the architecture analysis and the technology model, 4 converters are designed for a given set of specifications: 3.3–1.2 V, 280 mA output current at high switching frequency (100–200 MHz) in 40 nm bulk CMOS. A cascode power stage is used in order to enhance power conversion efficiency, and 1-phase and 2-phase structures are designed. Post-layout simulation results are presented, showing an efficiency above 90 % for a 2-phase converter.

Keywords DC–DC conversion · High frequency · CMOS · State-of-the-art · Low voltage · Buck

1 Introduction

Voltage conversion is a key enabler for large digital SoCs (Systems-on-Chip). There is a need to get the converter closer to its load in order to reduce resistive losses through PCB (Printed Circuit Board) traces, enable dynamic voltage scaling for more energy efficient computation and reduce footprint by depopulating the PCB. This translates into the need of integrated power conversion, either in package or on chip (respectively referred to as PSiP for Power Supply in Package and PSoC for Power Supply on Chip) and implies the use of advanced digital CMOS Complementary Metal-Oxide-Semiconductor) for power.

Several solutions are proposed to achieve power supply integration. The switched-capacitor approach allows to eliminate the inductors as it uses only capacitors as energy storage components, which are easily integrated within CMOS technology. However, in order to achieve high efficiency, capacitors must remain almost fully charged during operation as charging and discharging a capacitor is intrinsically lossy [36]. SC (Switched-Capacitor) converters are then limited when there is a need to supply a high current as the required capacitors become too large. There is also a lack of global stability analysis on SC converters [29], and regulation of SC converters is not straightforward. The other approach is the use of inductor-based converters. Their main drawback is the need for an inductor, which is not easily integrated within CMOS technologies.

The design target is an inductor-based DC–DC converter, converting 3.3–1.2 V, 350 mW output power, with a very high switching frequency (100–200 MHz). These design specifications are classical motherboard to microcontroller core power supply. The high switching frequency helps achieving low passive components values, but impacts negatively the efficiency. The goal is to integrate the converter with its digital load, so the manufacturing technology must be an advanced, low voltage technology, raising issues in terms of voltage capability (gate oxide dielectric strength, maximum drain-to-source voltage).

The passive components (namely the inductors and the capacitors) are manufactured using dedicated low-cost, high-density processes. The inductors are using magnetics

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on silicon technologies [20] as air-core inductors are prohibited so far because of EMI (ElectroMagnetic Interferences) issues. The capacitors used are deep-trench devices embedded inside a passive interposer [15]. The use of this passive interposer to interconnect all passive components helps reducing routing parasitics and improves the decoupling effectiveness. This heterogeneous approach of using dedicated technologies for each components allows for better components optimization and limited cost impact as using advanced CMOS technology for passive components manufacturing would require a lot of area.

An analysis is carried out on the current state-of-the-art of low voltage, high frequency, inductive converters in Sect. 2. Section 3 presents a losses model utilized to evaluate both architecture and CMOS technology performances in terms of conversion efficiency. Based on this, a solution is proposed in Sect. 4 using 40 nm bulk CMOS technology, and performance is analyzed based on post-layout simulations and passive models from characterization.

2 State-of-the-art review

The review focuses on steady-state performances, efficiency being the main indicator. In order to have comparable metrics, the scope of the review has been limited to low input voltage (below 5 V), low output power (below 5 W), high switching frequency (above 10 MHz) non-isolated step-down inductive DC–DC converters. This scope has been chosen to enclose the design specifications. Table 1 summarizes the scope of the review.

2.1 Methodology

The first step of a review is to define metrics that can cover most of the converters without loosing too much information. Transient aspects have been knowingly excluded from the review as transient performances are very dependent on the test conditions. Thermal aspects are also not considered as the studied DC–DC converters present losses well below 10 W/cm^2 so thermal drain approaches are generally sufficient.

The discussed fundamental metrics are the following: the input and output voltage, the output current, the output inductance and capacitance and the switching frequency. In addition to that, the technology node and the total converter area (when available) are also discussed. These metrics can be divided into three groups: the functional specifications (input and output voltage, output current and technology node), the performances (efficiency and area) and the design parameters for the rest of the metrics. Additional metrics can be derived from these elementary metrics, such as conversion ratio, output power, power conversion efficiency, or even more intricate indicators such as the Efficiency Enhancement Factor (EEF) defined in [34]. All the metrics are summarized in Table 2.

Landscapes of related metrics highlight various trends, design trade-offs and challenges.

Table 1 Scope of the review

	Value	Unit
Number of papers	33	–
Year range	2004–2014	–
Frequency range	10 –660	MHz
Technology range	22–500	nm
Input voltage range	1.1–5	V
Output voltage range	0.6–3.3	V
Power range	55–5000	mW

2.2 Landscapes

Figure 1 plots for each studied converter its output filter natural frequency (y-axis) versus its switching frequency (x-axis). Dots are parametrized with the number of phases of the converter. The plot clearly shows that increasing the switching frequency leads to an increase in the output filter natural frequency, thus reduces the components values of the output filter (output inductance and/or capacitance). Reducing the components values helps make them smaller, thus it is a step toward more integration (either in package or monolithically).However, going to a higher switching frequency increases the switching losses, reducing the

Table 2 Metrics for the review

Name	Symbol	Unit	Definition
Efficiency	η	%	P_{OUT}/P_{IN}
Switching frequency	F_{SW}	MHz	–
Technology node	-	nm	–
Input voltage	V_{IN}	V	–
Output voltage	V_{OUT}	V	–
Output current	I_{OUT}	mA	–
Conversion ratio	α	–	V_{OUT}/V_{IN}
Output power	P_{OUT}	mW	$V_{OUT}\times I_{OUT}$
Output capacitance	C_{OUT}	nF	–
Number of phases	N_{PH}	–	–
Phase inductance	L_{PH}	nH	–
Filter frequency	F_{LC}	GHz	$1/2\pi\sqrt{L_{PH}C_{OUT}}$

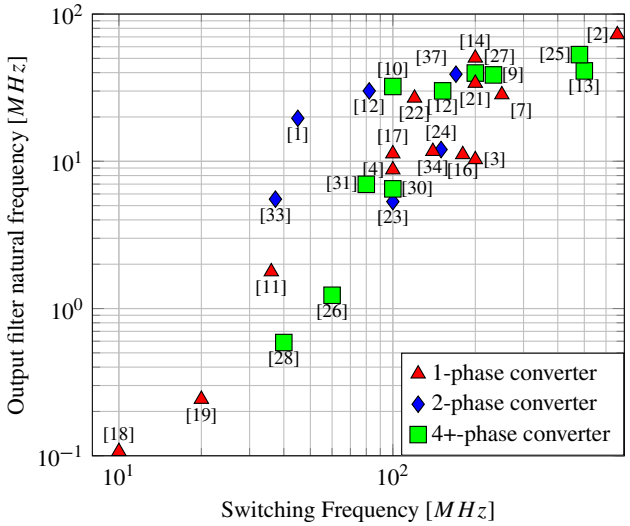

Fig. 1 Output filter natural frequency versus switching frequency

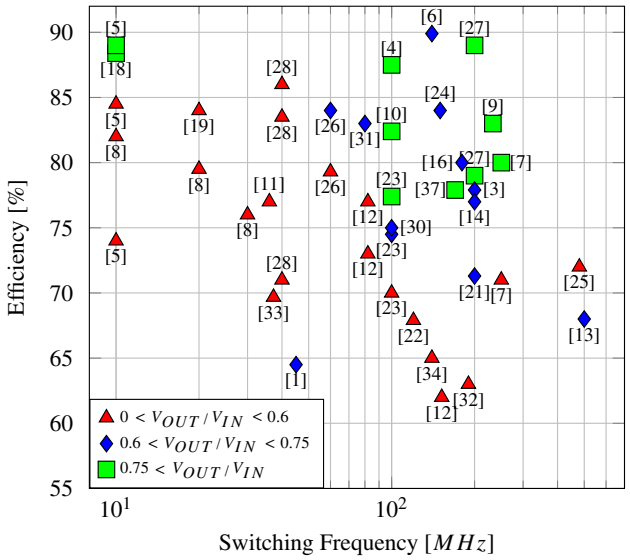

Fig. 2 Efficiency versus switching frequency, parametrized with conversion ratio

converter efficiency. This impact is deduced from Fig. 2, where the efficiency is plotted along with the switching frequency. The dots are parametrized with the conversion ratio. For a given conversion ratio, the efficiency tends to drop when the switching frequency increases. Ref. [2] (660 MHz, 0.455 conversion ratio) does not appear in the graph as it is not in the range of the vertical axis. Its efficiency is 31 %, which confirms the efficiency decrease with the frequency.

Another reading of this plot is the impact of the conversion ratio on the efficiency: at a given switching frequency, converters with lower conversion ratio tend to have a lower efficiency. This trend can be interpreted by

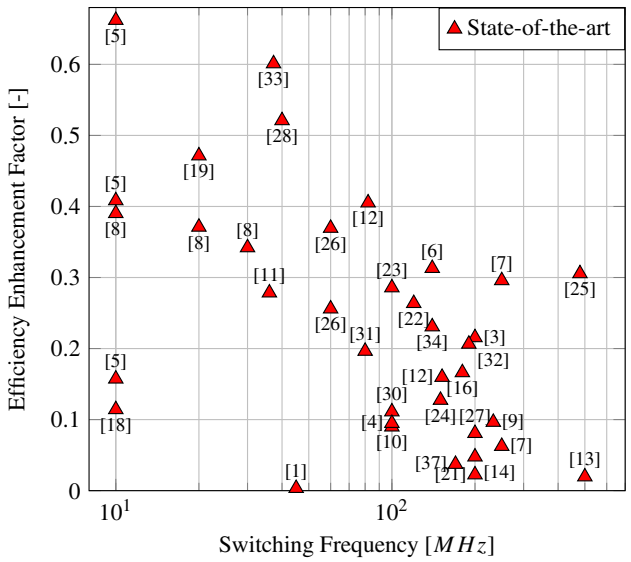

Fig. 3 Efficiency Enhancement Factor versus switching frequency

evaluating the efficiency gap between the converter and a hypothetical linear converter operating in the same conditions. In a first approximation, the efficiency of a linear converter is equal to the conversion ratio. For a given converter, having a high efficiency will put it further from the linear case if the conversion ratio is small.In order to be able to compare various converters against one another, it becomes necessary to use a figure of merit that takes into account both the efficiency and the conversion ratio. The EEF (Efficiency Enhancement Factor, in %) is defined as the power difference between the hypothetical linear converter and the actual converter, divided by the input power of the hypothetical linear converter, considering the same conversion conditions (input and output voltage, output power).

Figure 3 plots the EEF of each converter (calculated according to [34]) against the switching frequency. The maximum achieved EEF tends to reduce when the switching frequency increases, confirming the negative impact of switching frequency on conversion performance.The landscape in Fig. 4 presents the converter efficiency with respect to the output power. Most of the converters are targeting the 100-to-1000 mW power range. When considering the impact of output power on conversion efficiency, no trend can be identified. This means that output power is not a decisive metric for power efficiency.When looking at integrated DC–DC converters, a crucial parameter is the manufacturing technology of the active components. Figures 5 and 6 illustrate how the technology impacts the converters. Figure 5 places the efficiency of each converter against its manufacturing technology (active components). The points are parametrized with the switching frequency, as it impacts the

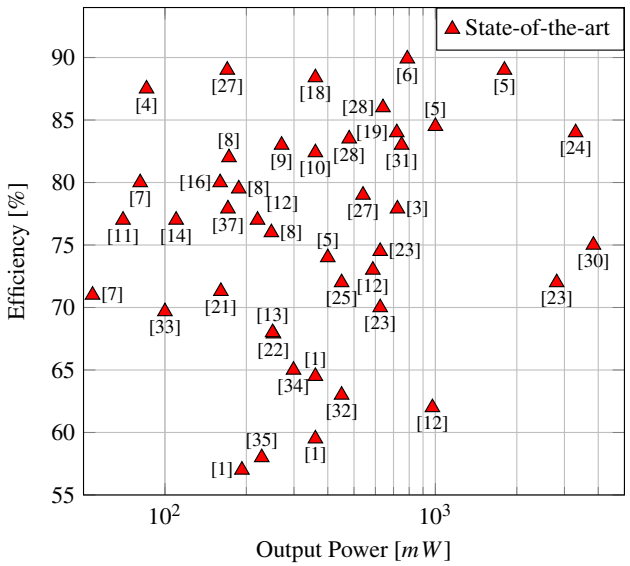

Fig. 4 Efficiency versus output power

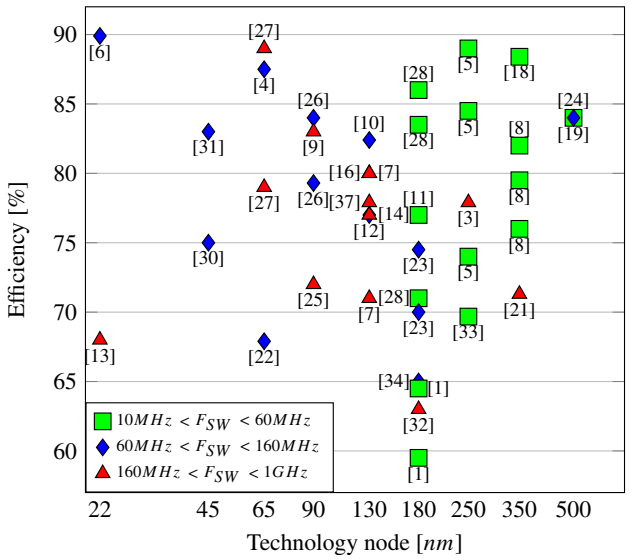

Fig. 5 Efficiency versus switching technology node, parametrized with switching frequency

efficiency. The global trend is that thinner technologies enable higher efficiencies. Furthermore, the use of more advanced technologies also allows for operating at higher switching frequencies.However, as technology shrinks, converters tends to operate with a lower input voltage. Figure 6 plots the input voltage of the converters with respect to their manufacturing technology. There is a noticeable trend that the maximum input voltage for each node is decreasing with the shrinking. Transistors in advanced technologies have shorter gate length and thinner gate oxide, thus maximum operating voltage is reduced.Major design trade-offs appear to be the following:

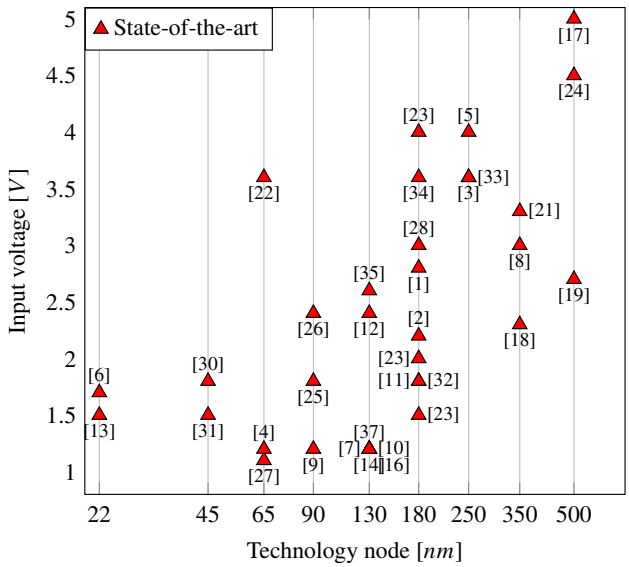

Fig. 6 Input voltage versus technology node

for a given set of specifications (input and output voltage, output power), a high switching frequency is required to reduce the output filter (in terms of components values). If the conversion ratio is small, achieving high efficiency is hard, especially if the switching frequency is really high. However, using an advanced technology helps reducing the losses and achieving high efficiency, but challenges arise when the converter input voltage is higher than the nominal technology voltage.

3 Model of losses

A model of losses has been developed in order to evaluate both the technology and the potential converter architectures regarding the design target. Each architecture has been evaluated in a first time considering only passive components losses and assuming ideal switches (no switching and on-state conduction losses). In a second time, only active components losses are considered, assuming ideal passive components. This two-pass approach allows for simple losses decoupling but is valid only if impact of both passive and active components on the current and voltage waveforms is limited. The losses of active components have been evaluated using classical metrics from the technology (on-state resistance, gate charge and drain-to-source capacitance).

3.1 Architecture evaluation

The architectures considered are 1-phase, 2-phase (uncoupled and coupled) synchronous bucks and 3-level converter, depicted in Figs. 7, 8, and 9 respectively, with waveforms respectively shown in Figs. 10, 11, 12, and 13.

All architectures are evaluated assuming the following conditions: input current (I_{IN}) is constant, switches are considered as ideal (no on-state resistance and switching losses), dead-time is reduced to 0 and the load is a constant current source. In order to develop equations of the circuits, the ESL (Equivalent Series Inductance) of the capacitors are omitted.

The steady-state equations are derived assuming a constant output voltage and the impact of the parasitic resistors on the waveforms is neglected. The converter efficiency is assumed to tend to 100 %, giving the following relations:

$$V_{OUT} = \alpha \times V_{IN}, \quad I_{IN} = \alpha \times I_{OUT} \tag{1}$$

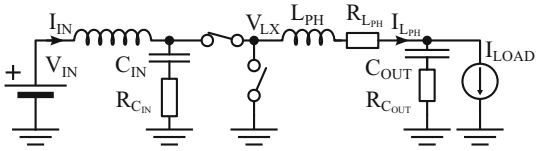

Fig. 7 1-phase buck converter with parasitic elements on passive components

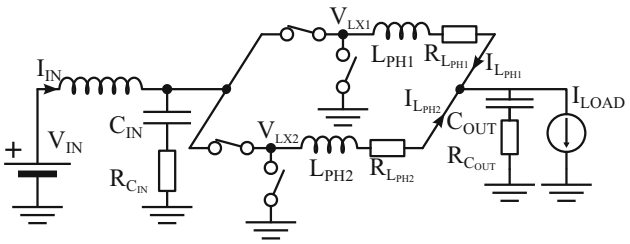

Fig. 8 2-phase buck converter with parasitic elements on passive components

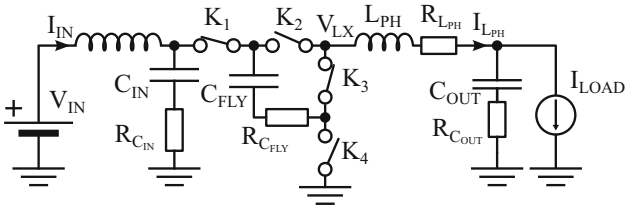

Fig. 9 3-level converter with parasitic elements on passive components

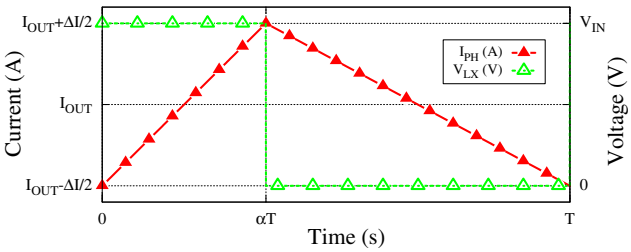

Fig. 10 Current and voltage waveforms for a 1-phase buck converter in CCM

3.1.1 One-phase converter

During the time between 0 and αT, the high-side switch is on (closed), and the low side switch is off (opened). The voltage across the inductor is $V_{IN} - V_{OUT}$. Only continuous conduction mode is considered, discontinuous conduction mode is not discussed here. The current increase through the inductor is calculated with:

$$V_{IN} - V_{OUT} = L_{PH} \times \frac{dI_{L_{PH}}}{dt} \tag{2}$$

$$\Delta I^{+}_{L_{PH}} = \alpha(1-\alpha)\frac{V_{IN} \times T}{L_{PH}} \tag{3}$$

The average current in the inductor is equal to the output current. The RMS (Root Mean Square) current through the inductor is calculated as follows:

$$I^2_{RMS\_L_{PH}} = I^2_{OUT} + \frac{\Delta I^2_{L_{PH}}}{12} \tag{4}$$

The current through the output capacitor for a 1-phase buck is only the AC component of the inductor current. The RMS current through the output capacitor is:

$$I^2_{RMS\_C_{OUT}} = \frac{\Delta I^2_{L_{PH}}}{12} \tag{5}$$

During low-side conduction, the current through the input capacitor is equal to the input current. During high-side conduction, the current through the input capacitor is the difference between the input current and the inductor current. The RMS current through the input capacitor for a 1-phase buck is:

$$I^2_{RMS\_C_{IN}} = \alpha(1-\alpha)I^2_{OUT} + \alpha\frac{\Delta I^2_{L_{PH}}}{12} \tag{6}$$

Passive component losses in a 1-phase buck converter can then be calculated taking into account ESR (Equivalent Series Resistance) of input and output capacitor and ESR of phase inductor.

$$\begin{aligned} P_{PAS\_1ph} = &\frac{\Delta I^2_{L_{PH}}}{12}(\alpha R_{C_{IN}} + R_{C_{OUT}} + R_{L_{PH}}) \\ &+ I^2_{OUT}(\alpha(1-\alpha)R_{C_{IN}} + R_{L_{PH}}) \end{aligned} \tag{7}$$

Equation (7) shows that losses in a 1-phase buck converter depend on 2 major metrics: the phase current ripple and the output current. The phase current ripple is defined by (3), and depends on switching frequency, inductance value and input voltage. When considering only passive components losses, a higher switching frequency helps reducing losses.

3.1.2 Two-phase converter

In a 2-phase buck converter, the current phase ripple is the same than the current ripple in 1-phase buck converter, defined by (3). Thus RMS phase current is:

$$I^2_{RMS\_L_{PH}} = \frac{I^2_{OUT}}{4} + \frac{\Delta I^2_{L_{PH}}}{12}, \tag{8}$$

the RMS current through the output capacitor is (for $\alpha \leq 0.5$):

$$I^2_{RMS\_C_{OUT}} = \frac{(1-2\alpha)^2}{(1-\alpha)^2}\frac{\Delta I^2_{L_{PH}}}{12}, \tag{9}$$

and the RMS current through the input capacitor is (for $\alpha \leq 0.5$):

$$I^2_{RMS\_C_{IN}} = 2\alpha\left(\alpha I_{OUT} - \frac{I_{OUT}}{2}\right)^2 + (1-2\alpha)I^2_{IN} + 2\alpha\frac{\Delta I^2_{L_{PH}}}{12} \tag{10}$$

Losses in a 2-phase buck converter are then:

$$P_{PAS\_2ph} = \frac{\Delta I^2_{L_{PH}}}{12}\left(2\alpha R_{C_{IN}} + \frac{(1-2\alpha)^2}{(1-\alpha)^2}R_{C_{OUT}} + 2R_{L_{PH}}\right) + I^2_{OUT}\left(\alpha(0.5-\alpha)R_{C_{IN}} + 0.5R_{L_{PH}}\right) \tag{11}$$

Using (7) and (11) it is possible to calculate the losses variation when going from a 1-phase to a 2-phase buck converter. It comes:

$$P_{gain} = P_{PAS\_1ph} - P_{PAS\_2ph} \tag{12}$$

$$P_{gain} = I^2_{OUT}\left(0.5\alpha R_{C_{IN}} + 0.5R_{L_{PH}}\right) + \frac{\Delta I^2_{L_{PH}}}{12}\left(-\alpha R_{C_{IN}} + \frac{\alpha(2-3\alpha)}{(1-\alpha)^2}R_{C_{OUT}} - R_{L_{PH}}\right) \tag{13}$$

Equation (13) shows that some losses components are decreasing while some others are increasing. However, even with a negligible $R_{C_{OUT}}$, P_{gain} is positive until $\Delta I_{L_{PH}}$ reaches $\sqrt{6} \times I_{OUT}$, condition which is never satisfied in continuous conduction mode – at the limit, $\Delta I_{L_{PH}}$ is equal to $2 \times I_{OUT}$.

3.1.3 Two-phase coupled converter

Figure 12 depicts the current and voltage waveforms for a 2-phase coupled buck converter.

The currents through the coupled inductors are defined with the following system:

$$\begin{cases} V_{LX1} &= L_{PH1} \times \dfrac{dI_{L_{PH1}}}{dt} + k\sqrt{L_{PH1}L_{PH2}} \times \dfrac{dI_{L_{PH2}}}{dt} \\ V_{LX2} &= L_{PH2} \times \dfrac{dI_{L_{PH2}}}{dt} + k\sqrt{L_{PH1}L_{PH2}} \times \dfrac{dI_{L_{PH1}}}{dt} \end{cases} \tag{14}$$

Solving this system gives the current variation for the different operating times ($0 \leq t \leq \alpha T$, and $\alpha T \leq t \leq T/2$, assuming $\alpha \leq 0.5$).

$$\Delta I_1 = \frac{\alpha(1-\alpha(1-k))}{1-k^2}\frac{V_{IN} \times T}{L_{PH}} \tag{15}$$

$$\Delta I_2 = \frac{-\alpha(k+\alpha(1-k))}{1-k^2}\frac{V_{IN} \times T}{L_{PH}} \tag{16}$$

$$\frac{\Delta I_1 - \Delta I_2}{2} = \frac{-\alpha(0.5-\alpha)}{1+k}\frac{V_{IN} \times T}{L_{PH}} \tag{17}$$

The optimum coupling factor that minimizes the total current ripple (equal to $\Delta I_{L_{PH1,t1}}$) is:

$$k_{opt} = \frac{\sqrt{1-2\alpha} + \alpha - 1}{\alpha} \tag{18}$$

The RMS current through the phase inductor is then:

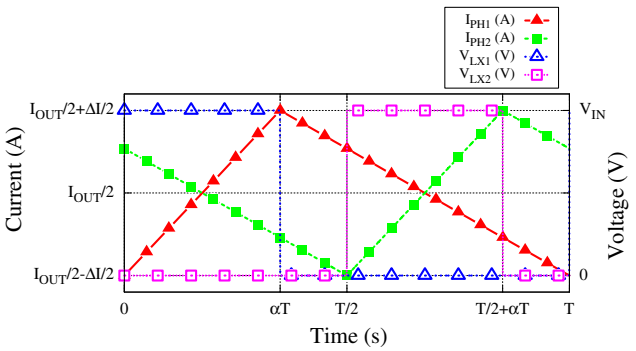

Fig. 11 Current and voltage waveforms for a 2-phase buck converter in CCM

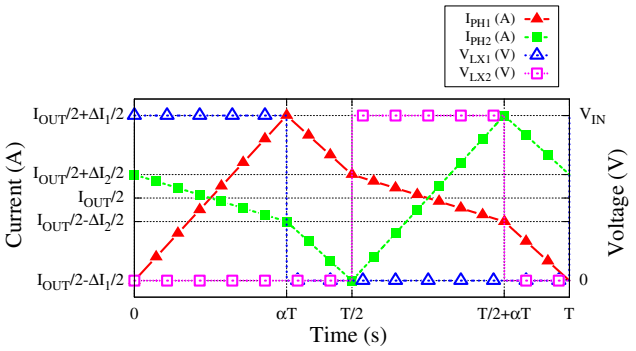

Fig. 12 Current and voltage waveforms of a 2-phase coupled buck converter in CCM

$$I^2_{RMS\_L_{PH1}} = \frac{I^2_{OUT}}{4} + \alpha\frac{\Delta I_1^2}{12} + \alpha\frac{\Delta I_2^2}{12} + (1-2\alpha)\left(\frac{(\Delta I_1 - \Delta I_2)^2}{48} + \left(\frac{\alpha V_{IN} T}{4(1-k)L_{PH}}\right)^2\right) \quad (19)$$

The RMS current through the input capacitor is:

$$I^2_{RMS\_C_{IN}} = 2\alpha\left(I_{IN} - \frac{I_{OUT}}{2}\right)^2 + (1-2\alpha)I^2_{IN} + 2\alpha\frac{\Delta I_1^2}{12} \quad (20)$$

So passive components losses of a 2-phase coupled buck are calculated as

$$P_{PAS\_2ph-cpl} = R_{C_{IN}} I^2_{RMS\_C_{IN}} + R_{C_{OUT}} I^2_{RMS\_C_{OUT}} + 2R_{L_{PH}} I^2_{RMS\_L_{PH}} \quad (21)$$

Comparing losses from (21) for a converter with an optimum coupling factor [calculated using (18)] against the losses of a non-coupled 2-phase converter (11) gives an advantage to the coupled structure.

3.1.4 Three-level converter

In a 3-level converter, the frequency seen by the inductor is twice the switching frequency, and the voltage swing at the input of the inductor is half the input voltage. Voltage and current waveforms are depicted in Fig. 13, for a duty cycle below 0.5. The inductor current ripple is equal to:

$$\Delta I_{L_{PH}} = \alpha(0.5-\alpha)\frac{V_{IN} \times T}{L_{PH}}. \quad (22)$$

As this converter is operating with one phase, inductor and output capacitor RMS currents are calculated with the same equations than for a single phase buck converter [Eqs. (4) and (5) respectively]. The only difference is the current ripple value, lower in a 3-level converter.

The RMS current through the flying capacitor is:

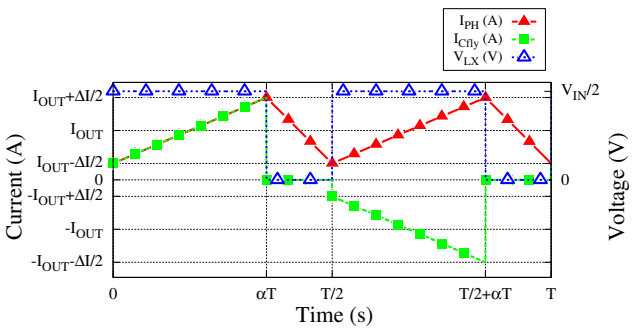

Fig. 13 Current and voltage waveforms for a 3-level buck converter in CCM

$$I^2_{RMS\_C_{FLY}} = 2\alpha\left(I^2_{OUT} + \frac{\Delta I^2_{L_{PH}}}{12}\right) \quad (23)$$

The RMS current through the input capacitor is:

$$I^2_{RMS\_C_{IN}} = \alpha(1-\alpha)I^2_{OUT} + \alpha\frac{\Delta I^2_{L_{PH}}}{12} \quad (24)$$

Total losses of a passive components in 3-level converter are then:

$$P_{PAS\_3lvl} = R_{C_{IN}} I^2_{RMS\_C_{IN}} + R_{C_{OUT}} I^2_{RMS\_C_{OUT}} + R_{C_{FLY}} I^2_{RMS\_C_{FLY}} + R_{L_{PH}} I^2_{RMS\_L_{PH}} \quad (25)$$

Except for the flying capacitor, all losses contributors in (25) are lower than the ones in a 1-phase buck as the current ripple is reduced. The performance gain of this converter will be strongly dependent on the ESR of the flying capacitor.

3.2 Active technology evaluation

Switches have conduction and switching losses. Conduction losses are modeled with the on-state resistance ($R_{DS_{ON}}$) of the switch and switching losses with the gate charge (Q_G) and drain-to-source capacitance (C_{DS}). The gate charge includes the gate-to-source, gate-to-drain and gate-to-body capacitances. Merging these capacitances into a single charge value allows for a simple analytic losses model of the technology, sacrificing a bit of accuracy.

3.2.1 Evaluation of losses

Losses are calculated for a complete switching cycle (turn-on and turn-off) for a switch with a given gate voltage swing (V_{GS}), drain-to-source voltage swing (V_{DS}), and a drain current (I_{DS}). The conduction losses are the ohmic losses of the on-state resistor:

$$P_{COND} = R_{DS_{ON}} \times I^2_{RMS\_DS} \quad (26)$$

During a switching cycle, the gate capacitance is charged up to the energy of $0.5 \times Q_G \times V_{GS}$ with a charging efficiency of 50 % (charging of a fully discharged capacitor with a constant voltage source), and then fully discharged. Thus switching losses due to gate charge are (assuming no charge recycling mechanism):

$$P_{SW\_G} = Q_G \times V_{GS} \quad (27)$$

In the same way, the drain-to-source capacitance is charged with the energy of $0.5 \times C_{DS} \times V_{DS}$ at the beginning of the switching cycle. Then it is fully discharged through the switch, and then charged again with an energy of $0.5 \times C_{DS} \times V_{DS}$ with a charging efficiency of 50 %. In a synchronous buck, the drain-to-source voltage swing is equal

to the input voltage. Switching losses due to drain-to-source capacitance are then:

$$P_{SW\_DS} = C_{DS} \times V_{IN}^2 \tag{28}$$

3.2.2 CMOS devices evaluation

In order to choose the switch that could achieve best efficiency prior to design, it is necessary to evaluate the switch performances with simple simulations. The metrics are the gate charge and the on-state resistance for a given gate-to-source voltage. MOSFETs are compared using normalized values with respect to MOSFET width (gate charge in $\mathrm{fF}/\mu m$ and on-state resistance in $\mathrm{k}\Omega{\cdot}\mu m$). MOSFET losses are then:

$$P_{MOS} = Q_G \times V_{GS} \times W_{MOS} + \frac{R_{DS_{ON}}}{W_{MOS}} \times I_{RMS\_DS}^2 \tag{29}$$

Optimal MOSFET width is equal to:

$$W_{MOS} = \sqrt{\frac{R_{DS_{ON}} \times I_{RMS\_DS}^2}{Q_G \times V_{GS}}} \tag{30}$$

Thus minimal achievable losses are equal to:

$$P_{MOS} = 2 \times I_{RMS\_DS} \sqrt{R_{DS_{ON}} \times Q_G \times V_{GS}} \tag{31}$$

Three MOSFET types are studied: 5, 3.3, and 1.2 V devices. The optimal MOSFET is the one that minimizes the product $R_{DS_{ON}} \cdot Q_G \cdot V_{GS}$. Keeping V_{GS} in the expression allows for performance evaluation of reduced voltage swing. $R_{DS_{ON}}$ and Q_G have been measured in simulation from available devices. Figure 14 shows the simulation circuits to extract gate charge and on-state resistance for a N-MOS device. The on-state resistance is computed using a DC simulation and measuring both drain-to-source current and voltage for a given gate-to-source voltage. The gate charge is computed using a transient simulation and integrating the gate current over time.Figure 15 depicts the performance metrics of the N-type devices. Most power efficient devices are found in the lower left corner, least efficient devices in the upper right corner. Diagonal lines are iso-losses lines. This figure shows that three 1.2 V devices in series (having 3 times the on-state resistance and 3 times the gate energy of a single device) present a better

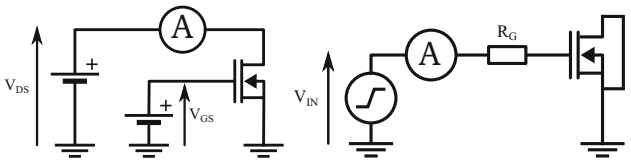

Fig. 14 Simulation circuits for on-state resistance (*left*) and gate charge (*right*) measurements

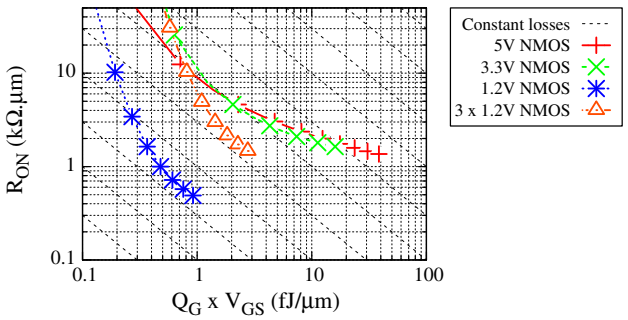

Fig. 15 Power efficiency figure of merit of NMOS devices in 40 nm technology

power efficiency than a single 3.3 V device, while being able to withstand up to 3.6 V (3×1.2 V).A power stage using three MOSFETs in series can then fulfill the requirements. This power stage is referred to a cascode power stage. Figure 16 depicts a standard and a cascode power stage. A cascode power stage requires 3 driver lines in order to ensure a proper switching sequence.

4 Proposed solution

Based on architecture and technology considerations developed in Sect. 3, various converters have been designed in order to assert model relevance. Converters are optimized to achieve best efficiency at nominal power point (3.3–1.2 V, 280 mA output current, based on the specifications presented in Sect. 1). Designed converters are the following:

- 1-phase standard buck at 200 MHz (3.3 V devices),
- 1-phase cascode buck at 200 MHz (1.2 V devices),
- 2-phase standard buck at 100 MHz (3.3 V devices),
- 2-phase cascode buck at 100 MHz (1.2 V devices).

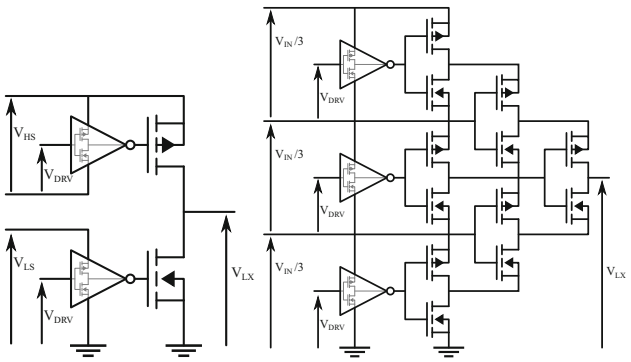

Fig. 16 Standard (*left*) and cascode (*right*) power stage

Table 3 Model-based and Cadence-based optimization results for standard and cascode power stages

	1-phase (μm)		2-phase (μm)	
	W_P	W_N	W_P	W_N
Standard power stages				
Model-based	10,372	7296	7179	5370
Cadence-based	10,200	7650	7200	5400
Cascode power stages				
Model-based	14,357	7706	10,763	5560
Cadence-based	14,880	6360	12,600	5400

4.1 Power stage optimization

In a first step, optimal MOSFETs width is computed using analytical equations developed in Sect. 3.2. Passive components losses are not considered in this optimization and the inductor value is considered sufficient enough to neglect current ripple contribution to losses. MOSFET losses are computed using (26), (27) and (28). Gate voltage swing is equal to 2 V. In order to optimize the cascode power stages, the same model is used, based on the the low-voltage devices characterization which is scaled to represent the 3 MOSFET in series: $3 \times R_{DS_{ON}}$, $3 \times Q_G \times V_{GS}$ and $C_{DS}/3$.

A global optimization is then carried out in the Cadence Virtuoso design environment on the selected converter structure. Optimization aims to maximize converter efficiency at the nominal power point. Table 3 summarizes optimization results in terms of MOSFET width for converters with standard and cascode power stage.Optimization results are consistent with model-based optimization. Model of losses based on $R_{DS_{ON}}$, $Q_G \times V_{GS}$ and C_{DS} allows for an accurate converter design for converter with a standard power stage. The model is also consistent for converters with a cascode power stage, but less accurate. The issue is that the model only takes into account the 2×3 power MOSFETs, while Cadence-based optimization includes all MOSFETs shown in Fig. 16.

4.2 Design and simulation results

The previously optimized converters have been designed and laid out using the CMOS 40 nm bulk technology in Cadence Virtuoso. Parasitic elements (resistors and capacitors) have been extracted from layout and taken into account in simulations.

As transient Post-Layout Simulation (PLS) of the full converter is time consuming, converter circuits have been limited to active components only. Impact of losses components can be calculated using equations developed in Sect. 3.1. Output filter has been replaced by a constant current source. All active components are included: current references, level shifters, drivers and power stage, as well as all metal routing. Converters are simulated in open loop. The output voltage is calculated as the average of the V_{LX} node. Figure 17 presents PLS efficiency of designed converters at nominal output current (280 mA). 1-phase converters are switching at 200 MHz and 2-phase converters at 100 MHz. Converters with cascode power stage presents a significantly better efficiency, confirming the interest of using low voltage devices in series in order to operate at higher voltage.

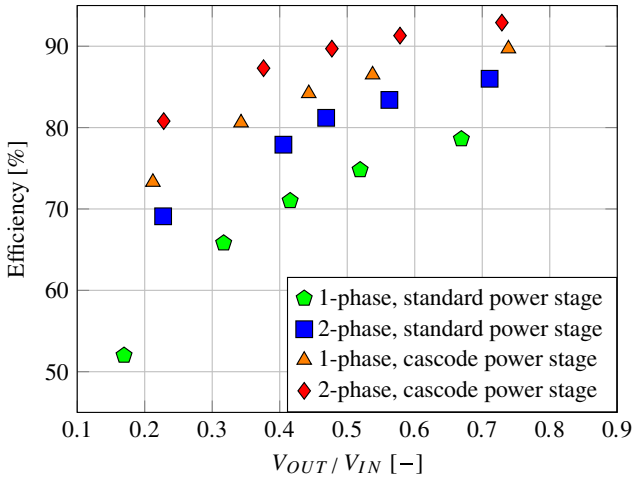

Fig. 17 Post-layout efficiency of active components of converters

5 Conclusion and perspectives

Based on practical implementations and analytical models of converters and technology, various high frequency DC–DC converters have been designed. The interest of multiphase converters has been demonstrated, along with the use of a cascode power stage. A cascode power cell allows for power circuits to benefit from technology shrinking and pushes efficiency significantly higher than standard power cell. Chip measurements should confirm post-layout trends.

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References

1. Abedinpour, S., Bakkaloglu, B., & Kiaei, S. (2007). A multistage interleaved synchronous buck converter with integrated output filter in 0.18 μm SiGe process. *IEEE Transactions on Power Electronics*, *22*(6), 2164–2175. doi:10.1109/TPEL.2007.909288.
2. Alimadadi, M., Sheikhaei, S., Lemieux, G., Mirabbasi, S., Dunford, W., & Palmer, P. (2009). A fully integrated 660 MHz low-

swing energy-recycling DC–DC converter. *IEEE Transactions on Power Electronics*, *24*(6), 1475–1485. doi:10.1109/TPEL.2009.2013624.

3. Bathily, M., Allard, B., & Hasbani, F. (2012). A 200-MHz integrated buck converter with resonant gate drivers for an RF power amplifier. *IEEE Transactions on Power Electronics*, *27*(2), 610–613. doi:10.1109/TPEL.2011.2119380.
4. Bergveld, H., Nowak, K., Karadi, R., Iochem, S., Ferreira, J., Ledain, S., Pieraerts, E., Pommier, M. (2009). A 65-nm-CMOS 100-MHz 87%-efficient DC–DC down converter based on dual-die system-in-package integration. In: *Energy conversion congress and exposition, 2009. ECCE 2009*. IEEE, pp. 3698–3705. DOI 10.1109/ECCE.2009.5316334.
5. Blanken, P., Karadi, R., Bergveld, H. (2008). A 50MHz bandwidth multi-mode PA supply modulator for GSM, EDGE and UMTS application. In: *Radio frequency integrated circuits symposium, 2008*. RFIC 2008. IEEE, pp. 401–404. DOI 10.1109/RFIC.2008.4561463.
6. Burton, E., Schrom, G., Paillet, F., Douglas, J., Lambert, W., Radhakrishnan, K., Hill, M. (2014). FIVR - Fully integrated voltage regulators on 4th generation Intel Core SoCs. In: Applied power electronics conference and exposition (APEC), 2014 29th annual IEEE, pp. 432–439. DOI 10.1109/APEC.2014.6803344.
7. Gong, X., Ni, J., Hong, Z., Liu, B. (2011). An 80% Peak efficiency, 0.84 mW sleep power consumption, fully-integrated DC–DC converter with Buck/LDO mode control. In: Custom integrated circuits conference (CICC), 2011 IEEE, pp. 1–4. DOI 10.1109/CICC.2011.6055338.
8. Hannon, J., Foley, R., Griffiths, J., O'Sullivan, D., McCarthy, K., Egan, M. (2009). A 20 MHz 200–500 mA monolithic buck converter for RF applications. In: *Applied power electronics conference and exposition, 2009*. APEC 2009. 24th Annual IEEE, pp. 503–508. DOI 10.1109/APEC.2009.4802705.
9. Hazucha, P., Schrom, G., Hahn, J., Bloechel, B., Hack, P., Dermer, G., et al. (2005). A 233-MHz 80%87% efficient four-phase DCDC converter utilizing air-core inductors on package. *IEEE Journal of Solid-State Circuits*, *40*(4), 838–845. doi:10.1109/JSSC.2004.842837.
10. Huang, C., Mok, P.: A 100 MHz 82.4% Efficiency Package-Bondwire Based Four-Phase Fully-Integrated Buck Converter With Flying Capacitor for Area Reduction. In: Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International, pp. 362–363 (2013). DOI 10.1109/ISSCC.2013.6487770.
11. Ishida, K., Takemura, K., Baba, K., Takamiya, M., Sakurai, T.: 3D Stacked Buck Converter with 15 μm Thick Spiral Inductor on Silicon Interposer for Fine-Grain Power-Supply Voltage Control in SiP's. In: 3D Systems Integration Conference (3DIC), 2010 IEEE International, pp. 1–4 (2010). DOI 10.1109/3DIC.2010.5751437.
12. Kim, W., Brooks, D., & Wei, G. Y. (2012). A fully-integrated 3-Level DC–DC converter for nanosecond-scale DVFS. *IEEE Journal of Solid-State Circuits*, *47*(1), 206–219. doi:10.1109/JSSC.2011.2169309.
13. Krishnamurthy, H., Vaidya, V., Kumar, P., Matthew, G., Weng, S., Thiruvengadam, B., Proefrock, W., Ravichandran, K., De, V.: A 500 MHz, 68% Efficient, Fully On-Die Digitally Controlled Buck Voltage Regulator on 22 nm Tri-Gate CMOS. In: VLSI Circuits Digest of Technical Papers, 2014 Symposium on, pp. 1–2 (2014). DOI 10.1109/VLSIC.2014.6858438.
14. Kudva, S., & Harjani, R. (2011). Fully-integrated on-chip DC–DC converter with a 450X output range. *IEEE Journal of Solid-State Circuits*, *46*(8), 1940–1951. doi:10.1109/JSSC.2011.2157253.
15. Lallemand, F., Voiron, F.: Silicon Interposers with Integrated Passive Devices, an Excellent Alternative to Discrete Components. In: Microelectronics Packaging Conference (EMPC), 2013 European, pp. 1–6 (2013).
16. Li, P., Bhatia, D., Xue, L., & Bashirullah, R. (2011). A 90–240 MHz hysteretic controlled DC–DC buck converter with digital PLL synchronization. *IEEE Journal of Solid-State Circuits*, *46*(9), 2108–2119. doi:10.1109/JSSC.2011.2139550.
17. Li, Q. (2012). A fully-integrated buck converter design and implementation for on-chip power supplies. *Journal of Computers*, *7*(5), 1270–1277. doi:10.4304/jcp.7.5.1270-1277.
18. Lu, D., Yu, J., Hong, Z., Mao, J., Zhao, H. (2012). A 1500 mA, 10 MHz on-time controlled buck converter with ripple compensation and efficiency optimization. In: *Applied power electronics conference and exposition (APEC), 2012 27th Annual IEEE*, pp. 1232–1237. DOI 10.1109/APEC.2012.6165976.
19. Maity, A., Patra, A., Yamamura, N., Knight, J. (2011). Design of a 20 MHz DC-DC buck converter with 84% efficiency for portable applications. In: *24th International Conference on VLSI Design (VLSI Design)*, pp. 316–321. DOI 10.1109/VLSID.2011.37.
20. Mathuna, S., O'Donnell, T., Wang, N., & Rinne, K. (2005). Magnetics on silicon: An enabling technology for power supply on chip. *IEEE Transactions on Power Electronics*, *20*(3), 585–592.
21. Onizuka, K., Kawaguchi, H., Takamiya, M., Sakurai, T.: Stacked-chip implementation of on-chip buck converter for power-aware distributed power supply systems. In: Solid-State Circuits Conference, 2006. ASSCC 2006. IEEE Asian, pp. 127–130 (2006). doi:10.1109/ASSCC.2006.357868
22. Ostman, K., Jarvenhaara, J., Broussev, S., Viitaniemi, I.: A 3.6-to-1.8-V Cascode Buck Converter With a Stacked LC Filter in 65-nm CMOS. Circuits and Systems II: IEEE Transactions on Express Briefs, PP(99), 1–5 (2014). doi:10.1109/TCSII.2014.2304875
23. Peng, H., Anderson, D., & Hella, M. (2013). A 100 MHz two-phase four-segment DC–DC converter with light load efficiency enhancement in 0.18 μm CMOS. *IEEE Trans. Circuits Syst. I*, *60*(8), 2213–2224. doi:10.1109/TCSI.2013.2239157.
24. Peng, H., Pala, V., Wright, P., Chow, T., & Hella, M. (2011). High efficiency, high switching speed, AlGaAs/GaAs P-HEMT DCDC converter for integrated power amplifier modules. *Analog Integr. Circuits Signal Process.*, *66*, 331–348. doi:10.1007/s10470-010-9543-z.
25. Schrom, G., Hazucha, P., Hahn, J., Gardner, D., Bloechel, B., Dermer, G., Narendra, S., Karnik, T., De, V.: A 480-MHz, Multi-Phase Interleaved Buck DC-DC Converter with Hysteretic Control. In: Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, vol. 6, pp. 4702–4707 Vol. 6 (2004). doi:10.1109/PESC.2004.1354830
26. Schrom, G., Hazucha, P., Paillet, F., Rennie, D.J., Moon, S.T., Gardner, D.S., Kamik, T., Sun, P., Nguyen, T.T., Hill, M.J., Radhakrishnan, K., Memioglu, T.: A 100MHz Eight-Phase Buck Converter Delivering 12 A in 25 mm^2 Using Air-Core Inductors. In: Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE, pp. 727–730 (2007). doi:10.1109/APEX.2007.357595
27. Song, M.K., Dehghanpour, M.F., Sankman, J., Ma, D.: A VHF-Level Fully Integrated Multi-Phase Switching Converter Using Bond-Wire Inductors and On-Chip Decoupling Capacitors and DLL Phase Synchronization. In: 2014 Twenty-Ninth Annual IEEEApplied Power Electronics Conference and Exposition (APEC) (2014)
28. Song, M.K., Sankman, J., Ma, D.: A 6A 40MHz Four-Phase ZDS Hysteretic DC-DC Converter with 118mV Droop and 230ns Response Time for a 5A/5ns Load Transient. In: Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International, pp. 80–81 (2014). doi:10.1109/ISSCC.2014.6757346

29. Souvignet, T., Allard, B., Trochut, S., Hasbani, F.: A Simple Approach to a Linear Control of Switched Capacitor DC-DC Converters in System-on-Chip. In: Control and Modeling for Power Electronics (COMPEL), 2014 IEEE 15th Workshop on, pp. 1–7 (2014). doi:10.1109/COMPEL.2014.6877205
30. Sturcken, N., O'Sullivan, E., Wang, N., Herget, P., Webb, B., Romankiw, L., et al. (2013). A 2.5D integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer. *IEEE J. Solid-State Circuits*, *48*(1), 244–254. doi:10.1109/JSSC.2012.2221237.
31. Sturcken, N., Petracca, M., Warren, S., Carloni, L., Peterchev, A., Shepard, K.: An Integrated Four-Phase Buck Converter Delivering 1A/mm2 with 700ps Controller Delay and Network-on-Chip Load in 45-nm SOI. In: Custom Integrated Circuits Conference (CICC), 2011 IEEE, pp. 1–4 (2011). doi:10.1109/CICC.2011.6055336
32. Sun, J., Lu, J.Q., Giuliano, D., Chow, T., Gutmann, R.: 3D Power Delivery for Microprocessors and High-Performance ASICs. In: Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE, pp. 127–133 (2007). doi:10.1109/APEX.2007.357505
33. Villar, G., Alarcon, E.: Monolithic Integration of a 3-Level DCM-Operated Low-Floating-Capacitor Buck Converter for DC-DC Step-Down Conversion in Standard CMOS. In: Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, pp. 4229–4235 (2008)
34. Wens, M., Steyaert, M.: A Fully-Integrated 0.18 μm CMOS DC-DC Step-Down Converter, Using a Bondwire Spiral Inductor. In: Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE, pp. 17–20 (2008). doi:10.1109/CICC.2008.4672009
35. Wens, M., & Steyaert, M. (2011). A fully integrated CMOS 800-mW four-phase semiconstant ON/OFF-time step-down converter. *IEEE Trans. Power Electron.*, *26*(2), 326–333. doi:10.1109/TPEL.2010.2057445.
36. Wens, M., Steyaert, M.: Basic DC-DC Converter Theory. In: Design and Implementation of Fully-Integrated Inductive DC-DC Converters in Standard CMOS, Analog Circuits and Signal Processing, pp. 27–63. Springer, Netherlands (2011). doi:10.1007/978-94-007-1436-6_2
37. Wibben, J., & Harjani, R. (2008). A high-efficiency DC–DC converter using 2 nH integrated inductors. *IEEE J. Solid-State Circuits*, *43*(4), 844–854. doi:10.1109/JSSC.2008.917321.

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