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MIXED SIGNAL LETTER

High efficiency two-step capacitor switching scheme for SAR ADC

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Abstract A high efficiency two-step capacitor switching scheme for a successive approximation register analogue-to-digital converter is presented. Two-step architecture, split capacitor array, C-2C dummy capacitor and multiple switching schemes are combined in the proposed switching scheme. The proposed switching scheme achieves a 99.75 % reduction in switching energy and the total capacitance is reduced 85.9 % compared with the conventional architecture.

Keywords SAR ADC · Switching scheme · Two-step · High efficiency

1 Introduction

SAR ADCs are widely utilized in low-power field. With the rapid development of semiconductor technology, the energy consumption is smaller and smaller. The switching energy still occupies a high proportion of the total energy consumption of SAR ADC. Recently, many techniques are proposed to reduce switching energy. Compared with conventional architecture, the monotonic [1], V_{cm}-based [2], V_{cm}-based monotonic [3] and energy-efficient hybrid switching scheme [4] reduce the switching energy by 81.26, 87.52, 97.66 and 98.83 %, respectively. The energy efficiency of SAR ADCs which are based on the normal architecture is close to the limitation. To further reduce the switching energy, new architecture should be adopted. Bridge capacitor used in [5, 6] and split capacitor used in [7] are usually adopted to save more energy.

The proposed switching scheme combines two-step architecture, split capacitor array and C-2C dummy capacitor together. The average energy consumption is reduced by 99.75 %, and the total capacitance is reduced by 85.9 %. The proposed switching scheme is described in Sect. 2. The analysis and comparison are provided in Sect. 3, and Sect. 4 gives the conclusion.

2 Proposed switching scheme

Figure 1 shows the architecture of the proposed 10-bit SAR ADC. The proposed SAR ADC adopts the two-step architecture. And the proposed SAR adopts fully differential architecture to suppress the common-mode noise. In addition, the most significant bit (MSB) capacitor is split into capacitors which are the same as the rest of capacitors. The C-2C dummy capacitor are adopted to reduce the total capacitance as reported in [8]. However, [8] uses only two voltage references while the proposed switching scheme utilizes one more voltage reference, the common-mode voltage. Moreover the switching step is changed as well.

For N-bit SAR ADC, the first M bits can be determined by split capacitor array during the first step, and the rest of bits are determined by C-2C capacitor array during the second step. In this switching scheme, M is set as 6. Because the switching scheme of the state that V_{ip} is larger than V_{in} and that of the condition that V_{ip} is smaller than V_{in} are similar, for simplicity, we just introduces the latter.

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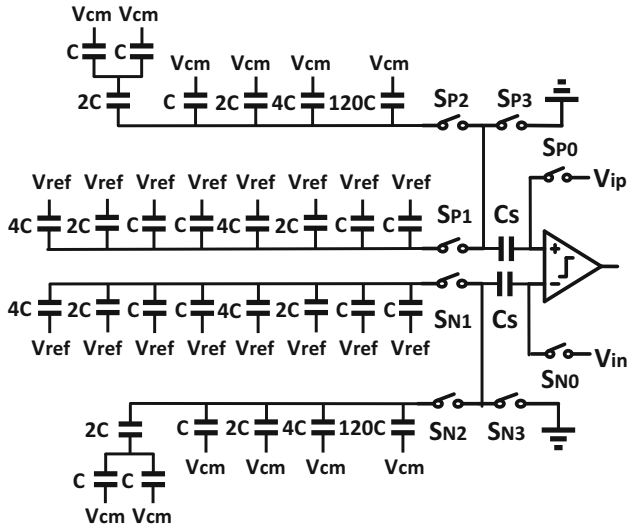

Fig. 1 The architecture of the proposed 10-bit SAR ADC

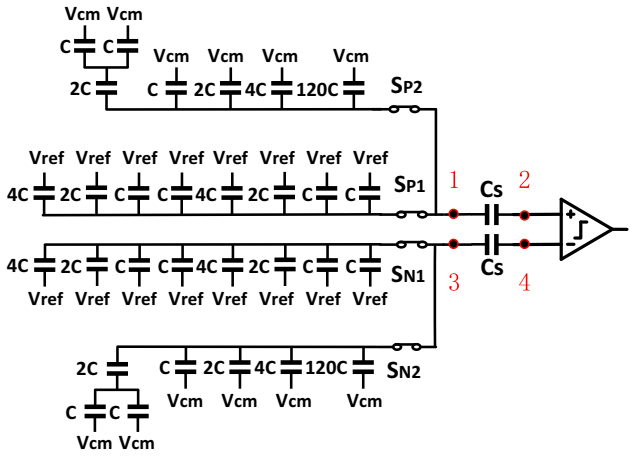

Fig. 2 The simplified architecture of circuit after sampling

2.1 The first step

During the sampling phase, all the switches are on. The differential signal is sampled to the "right" plates of capacitor Cs. The bottom plates of capacitors in the split capacitor arrays are connected to V_{ref}, and the bottom plates of capacitors in C-2C capacitor arrays are connected to V_{cm}. After sampling, S_{P0}, S_{N0} S_{P3} and S_{N3} are off. The circuit can be simplified into Fig. 2.

There is no voltage reference will charge or discharge to points 2 and 4. So the total numbers of charge on the "right" plate of Cs are unchanged. Based on Eq. (1), Eqs. (2) and (3) are always valid.

$$V_{Cs} = \frac{Q_{total}}{Cs} \tag{1}$$

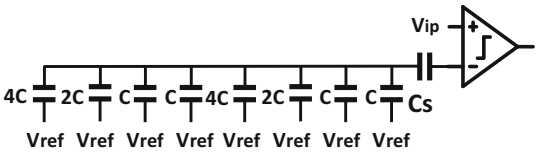

Fig. 3 The simplified architecture of circuit after getting MSB

$$V_2 - V_1 = V_{ip} \tag{2}$$

$$V_4 - V_3 = V_{in} \tag{3}$$

So Cs keeps input signal all the time. The voltage of the "left" plate of Cs follows the top plates of split capacitor array and C-2C capacitor array. The size of Cs won't influence the function of circuit.

Because of the top-plate sampling, MSB is determined without energy consumption. When V_{ip} is smaller than V_{in}, S_{N2} and S_{P1} are off immediately. And the voltage of positive terminal of comparator will not change until the first step is finished. So the circuit can be simplified as Fig. 3 after getting MSB. In this switching scheme, we set M as 6. To explain the switching scheme of the first step after MSB decision clearly, an example in which M equals 4 is given in Fig. 4. In both cases, the principles of the switching scheme during the first step are the same. When V_{ip} is smaller than V_{in}, all the bottom plates of capacitors in the split capacitor array are connected to V_{cm}, and the (MSB-1) bit are determined. The voltages of top plates and bottom plates of capacitors decrease $V_{ref}/2$ at the same time. Thus, there is no energy consumption during the second comparison. In addition, S_{N2} and S_{P1} should be off before changing the voltage of the bottom plates of capacitors in split capacitor array to keep the function of circuit right. According to the result of the second comparison, all the split MSB capacitors are connected to V_{ref} or 0 to determine the third bit, and this step consumes $1/4CV_{ref}^2$. Then, the ADC performs the monotonic switching scheme until the end of the first step as shown in Fig. 4.

The average switching energy for the first step is given below:

$$E_{avg\_first} = \left(2^{M-6} + \sum_{i=0}^{M-4} \frac{2^{M-3-i} - 1}{2^{M-2i}}\right) CV_{ref}^2 \tag{4}$$

2.2 The second step

During the second step, the voltage of V_{in_first} will keep the value of the final result of the first step until all bit are determined. The circuit can be simplified as Fig. 5. If the output of comparator is "1" at the end of first step, the bottom plate of the 4C capacitor is connected to 0. Otherwise, the

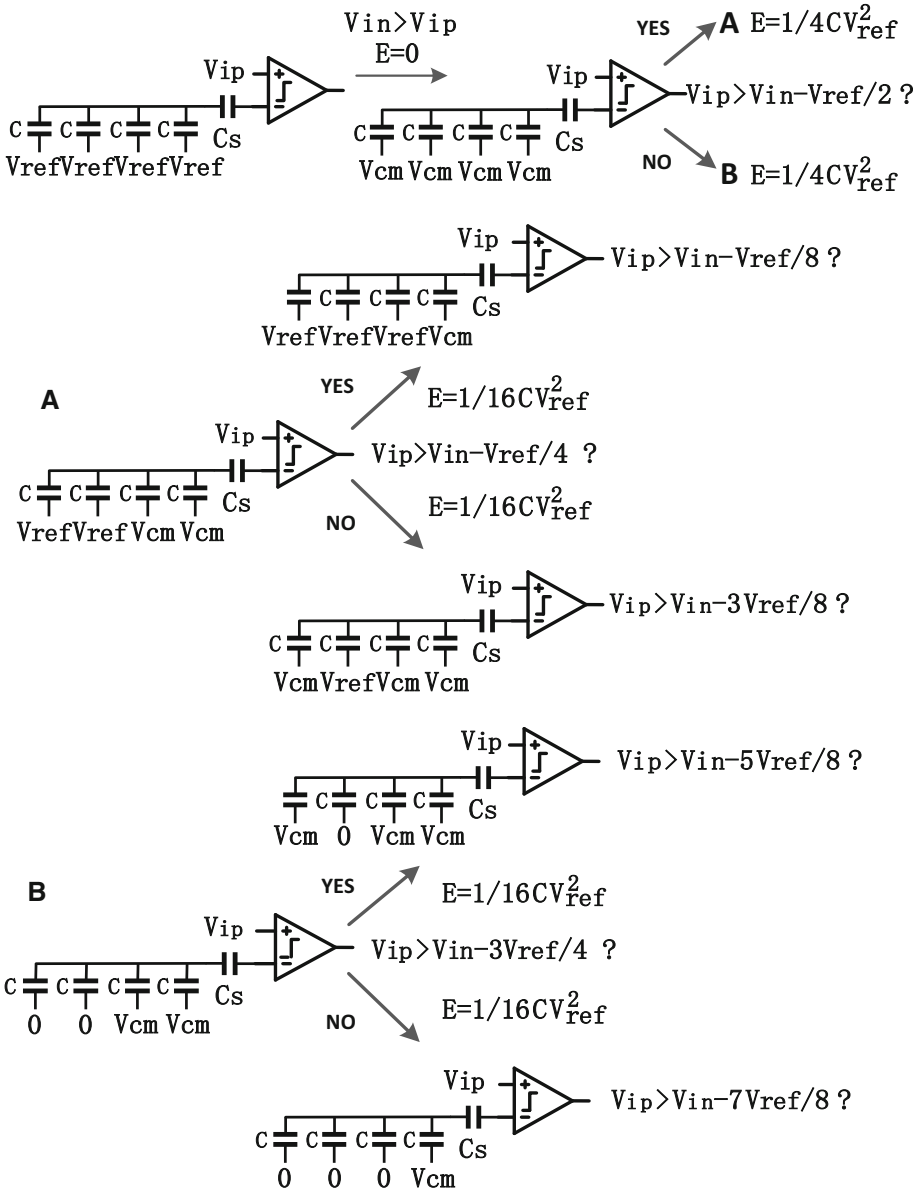

Fig. 4 Switching scheme of the first step after MSB decision when M equals 4

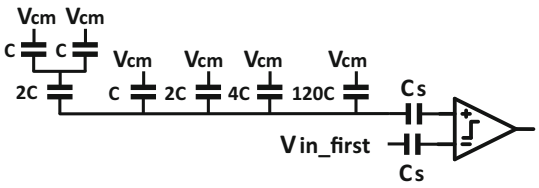

Fig. 5 The simplified architecture of circuit at the end of first step

bottom plate will be connected to V_{ref}. Next, ADC will perform the same procedure. And the last bit is determined by C-2C dummy capacitor. And the waveform of the proposed switching scheme is shown in Fig. 6.

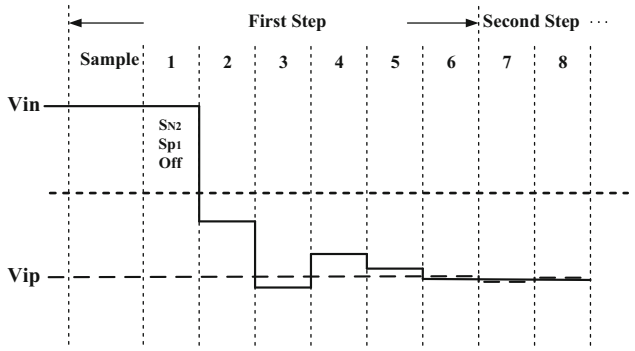

Fig. 6 The waveform of the proposed switching scheme when V_{ip} is smaller than V_{in}

Table 1 Comparison of different switching schemes

Switching scheme	Average switching energy (CV^2_{ref})	Energy saving (%)	Area reduction (%)
Conventional	1363.33	0	0
Monotonic [1]	255.50	81.26	50
V_{cm}-based [2]	170.17	87.52	50
V_{cm}-based monotonic [3]	31.88	97.66	75
Hybrid [4]	15.88	98.83	75
This work	3.44	99.75	85.9

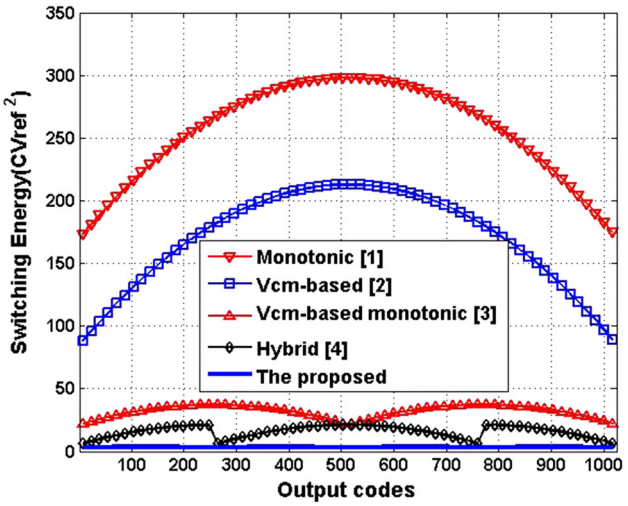

Fig. 7 Switching energy against output code

3 Analysis and comparison

For a 10-bit SAR ADC, there is more than one choice for the value of M. The average energy consumption and the total capacitance are dependent on the value of M. There is a trade-off between energy consumption and area. Comparing with other cases, M is set as 6 for higher energy efficiency. The behaviour simulation of different switching schemes for a 10-bit differential SAR ADC was performed in MATLAB for comparison with the proposed switching scheme as shown in Fig. 7.

The average switching energy for the proposed switching scheme is $3.44CV^2_{ref}$ which achieves a 99.75 % reduction compared with the conventional SAR. The total energy consumed by capacitor arrays are reduced effectively. Table 1 shows the comparison of different switching schemes for a 10-bit SAR ADC. It is obvious that the proposed scheme achieves the highest energy efficiency. In addition, the proposed scheme saves more area than the others.

4 Conclusions

A novel architecture low-power switching scheme is proposed. The proposed switching scheme combines two-step architecture, split capacitor array, C-2C dummy capacitor and more than one switching schemes together. This scheme with new architecture achieves a 99.75 and 85.9 % reduction in switching energy reduction and area, respectively. So far, the energy efficiency of this scheme is the highest.

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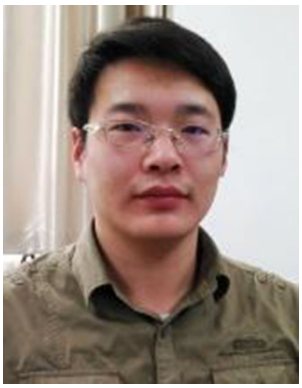

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