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# Design of a high efficiency and low EMI boost converter using bi-frequency PFM control scheme

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**Abstract** A bi-frequency PFM controlled boost DC–DC converter, combining the respective advantages of the conventional PWM and PFM, is designed and implemented in this paper to improve the electro-magnetic interference (EMI) and efficiency of the system in a wide load range. The spectral energy of proposed bi-frequency PFM controlled converter is distributed to more frequency points to decrease the discrete harmonic peak, achieving low EMI and noise level. By detecting load changes, the proposed converter operates at a corresponding frequency at light load or heavy load and switches between the two frequencies at medium load to improve full-load efficiency. A control IC for the boost converter has been fabricated in Founder Microelectronics 0.5 μm CMOS process. The layout area is 800 × 640 $\mu m^2$. Experimental results show that the full-load conversion efficiency is over 80 %, and the quiescent current is under 10 μA. Meanwhile, the converter has fine EMI characteristics.

**Keywords** Bi-frequency modulation · Dual-oscillator · Boost DC–DC converter · EMI · Full load efficiency

## 1 Introduction

In recent years, high efficiency and small EMI of DC–DC converter have become hot research directions with the continuous development of portable electronic products. Pulse width modulation (PWM) and Pulse frequency modulation (PFM) are two popular control modes in DC–DC converters. In order to make sure that the system can operate properly at heavy load, higher frequency in the PWM controlled converter should be chosen. However, it will result in low efficiency under light load. As portable electronic products mostly work in the light load or standby mode, the PFM control scheme is more widely adopted than PWM control scheme in the DC–DC converter to reduce power consumption, effectively.

There are many kinds of PFM modes to regulate the output voltage by changing its frequency, such as forced PFM mode [1], burst mode [2], and skip mode [3]. But PFM also has some disadvantages, such as narrow frequency spectrum [4], large output ripple and large EMI [5]. As a relatively novel pulse control scheme, bi-frequency control technique, combining advantages of the frequency dithering control [6] and fixed frequency PWM control technology, appears firstly in [7] to reduce the EMI. Though this paper only illustrates the single working condition of soft-switching quasi-resonant converter, it is of considerable significance for further studies. A bi-frequency controlled buck converter has been proposed in [8] which has low-frequency and high-frequency switches, as a compromise solution to the contradiction between "high frequency" and "efficiency". This method is applicable to medium and high power occasions, but its circuit is very complex. A bi-frequency controlled DC–DC converter has been presented in [9], which only gives system model and simulation verification of the boost converter based on the control technique. A new bi-frequency constant real-time control technology has been proposed in [10], but the mainly focus on theoretical study and system analysis, without specific actual circuit design, is its drawback.

Based on the above analysis, this paper proposes a boost converter, adopting bi-frequency control scheme, to obtain

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better EMI performance and higher conversion efficiency. The operation principle of proposed Bi-frequency PFM controller for DC–DC boost converter is analyzed in Sect. 2, and circuit design consideration is given in Sect. 3. Section 4 shows the layout and test results, based on Founder Microelectronics 0.5 μm CMOS process.

## 2 Operation principle of a bi-frequency PFM controller

The system diagram of proposed boost converter is shown in Fig. 1. The voltage comparator [11, 12] generates different control signals $V_{comp}$ to select different frequencies, depending on the load conditions. By detecting $V_{comp}$, the bi-frequency oscillator outputs a corresponding switching signal *CLK* to the driving circuit, adjusting the output voltage $V_o$. *EN* is the enable signal determining whether the bi-frequency PFM controller works or not. The hysteresis comparator disables the *CLK* signal at extreme light load, when the low frequency may not be low enough to stabilize the output voltage $V_o$.

Figure 2 shows the typical operation waveform of proposed bi-frequency control scheme. Where $f_H$ is the high frequency of bi-frequency oscillator, $T_H$ is the corresponding period; $f_L$ is the low frequency of bi-frequency oscillator, $T_L$ is the corresponding period; *Ton* is the turn-on time of the power switch. The basic working principle can be illustrated as follows: the bi-frequency PFM controller outputs high frequency signal to the driving circuit when feedback voltage $V_{fb}$ (see in Fig. 1) is lower than the reference voltage $V_{ref}$; otherwise outputting low frequency signal.

The efficiency of the PWM converter is:

$$\eta_{pwm} = \frac{\frac{V_o^2}{R_L}}{\frac{V_o^2}{R_L} + W_{LOSS}} = \frac{V_o^2}{V_o^2 + (f_e \times W_{SW} + W_{CON}) \times R_L} \quad (1)$$

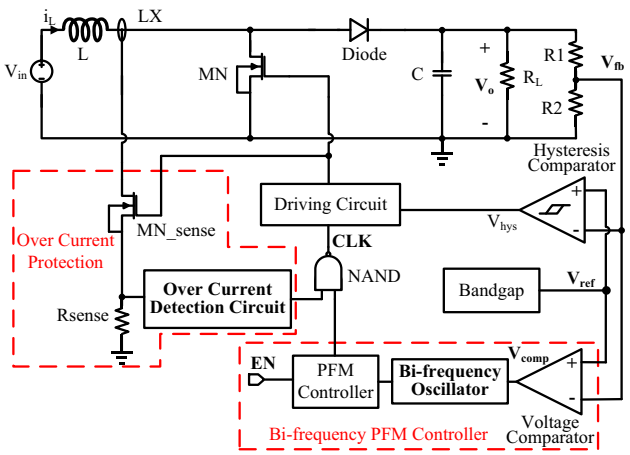


**Fig. 1** System diagram of proposed boost converter

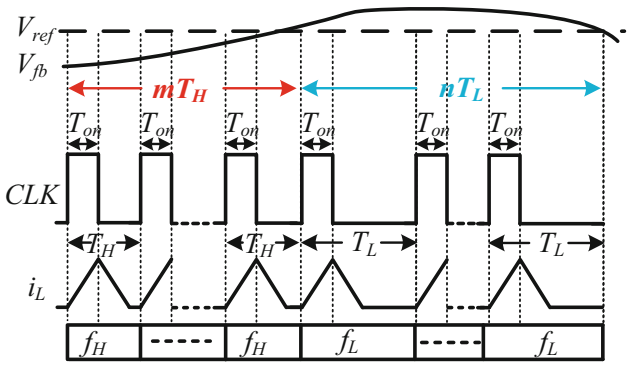


**Fig. 2** Operation waveform of proposed bi-frequency control scheme

The efficiency of the bi-frequency PFM converter is:

$$\eta_{bif} = \frac{\frac{V_o^2}{R_L}}{\frac{V_o^2}{R_L} + W_{LOSS}} = \frac{\frac{V_{in}T_{on}V_o(1-D_{on})}{2L}}{\frac{V_{in}T_{on}V_o(1-D_{on})}{2L} + (f_e \times W_{SW} + W_{CON})} \quad (2)$$

where $W_{SW}$ is equivalent to the switching loss, $W_{CON}$ is the conduction loss of power tube, $W_{LOSS}$ is the sum of switching loss and conduction loss, $D_{on}$ is the equivalent duty ratio, $f_e$ is the equivalent frequency.

It can be seen from (1) and (2) that the efficiency of the PWM control scheme will be significantly reduced with the increasing of load resistance $R_L$, because its frequency is constant under light load operation. However, the efficiency of the bi-frequency PFM control scheme is only determined by the equivalent frequency $f_e$ ($f_e$ is relatively low), which is independent from $R_L$. Therefore, the bi-frequency PFM scheme can effectively improve the efficiency under light load.

In addition, the bi-frequency PFM control signal *CLK* consists of *m* high-frequency pulses of $f_H$ and *n* low-frequency pulses of $f_L$ according to the load condition.

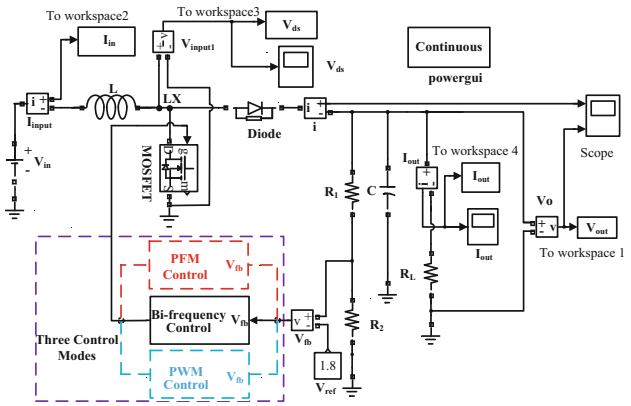


**Fig. 3** System model of the boost converter using three control schemes, respectively

Therefore, the Fourier transform of the proposed bi-frequency PFM control signal is:

$$F_{BF}(f) = 2\pi f_M \sum_{n=-\infty}^{+\infty} \left|F_{f_1(t)}(nf_M)\right| \delta(f - nf_M) \tag{3}$$

$$F_{f_1(t)}(f) = T_{on} Sa(\pi f T_{on}) \left( \frac{1 - e^{-j2\pi f m T_H}}{1 - e^{-j2\pi f T_H}} + e^{-j2\pi f m T_H} \frac{1 - e^{-j2\pi f n T_L}}{1 - e^{-j2\pi f T_L}} \right) \tag{4}$$

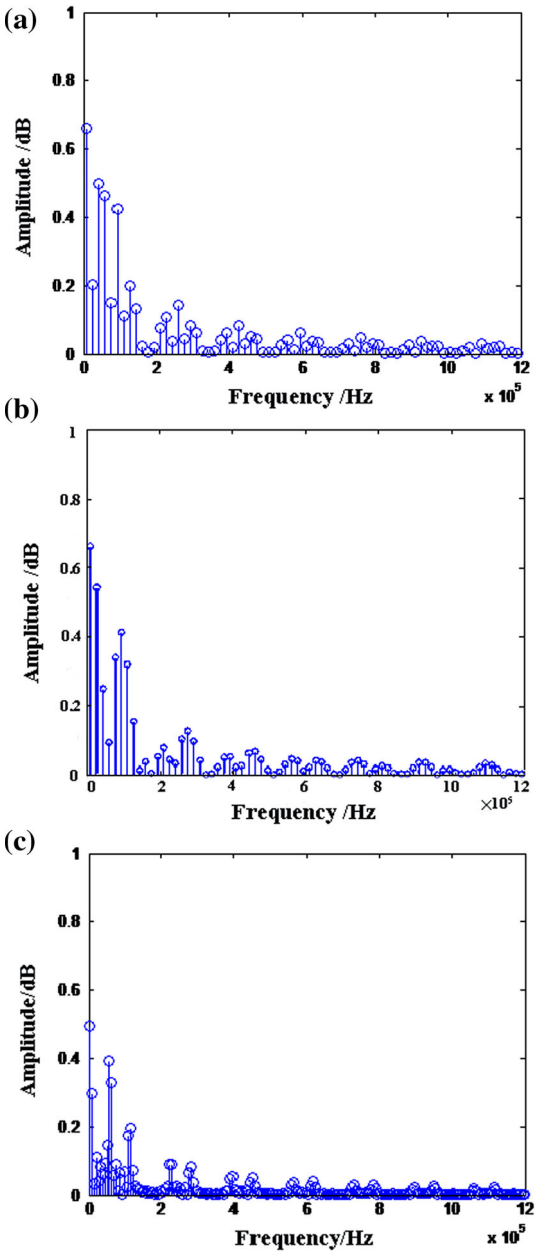


**Fig. 4** Frequency spectrum of *LX* signal under different control schemes. **a** PWM control scheme. **b** PFM control scheme. **c** BF-PFM control scheme

where $f_M = 1/(mT_H + nT_L)$, $|\cdot|$ is modular arithmetic.

While the Fourier transform of the PWM and PFM control signals are:

$$F_{PWM}(f) = 2\pi D \sum_{n=-\infty}^{+\infty} \left|\frac{\sin(n\pi D)}{n\pi D}\right| \delta(f - nf_S) \tag{5}$$

$$F_{PFM}(f) = 2\pi f_e \sum_{n=-\infty}^{+\infty} \left|Sa\left(\frac{n\pi f_e}{2}\right)\right| \delta(f - nf_e) \tag{6}$$

where $D$ is the duty cycle, $f_S$ is the switching frequency.

Compared with traditional PFM mode and PWM mode, the spectrum of the bi-frequency PFM control signal is no longer isolated and scattered. Besides, it has a large number of side frequencies and the spectrum energy is distributed to more frequency points to decrease the discrete harmonic peak, achieving low EMI and noise level. Consequently, the DC–DC converter with bi-frequency PFM mode is easier to meet the EMI standards.

## 3 Circuit design consideration

The proposed Bi-frequency PFM controller needs to generate two frequency signals $f_L$ and $f_H$, corresponding to two duty cycle $D_L$ and $D_H$, to meet different input voltages and load changes. The relationship between the input voltage $V_{in}$ and output voltage $V_o$ of the boost circuit is given by [13]:

$$V_{in} \frac{1}{1 - D_{on}} = V_o \tag{7}$$

If the circuit can work properly at 2 V, and the output voltage $V_o$ can achieve 5 V, then the minimum $D_{on}$ is 60 %. Another case, if the input voltage is 4 V and output voltage is 5 V, the corresponding $D_{on}$ will be about 20 %. In actual bi-frequency PFM control scheme, the paper sets a low frequency $f_L$ and a high frequency $f_H$. $T_{on}$ is a fixed value, i.e. $f_L T_{on} = D_L = 20\ \%, f_H T_{on} = D_H = 60\ \%$. Thus

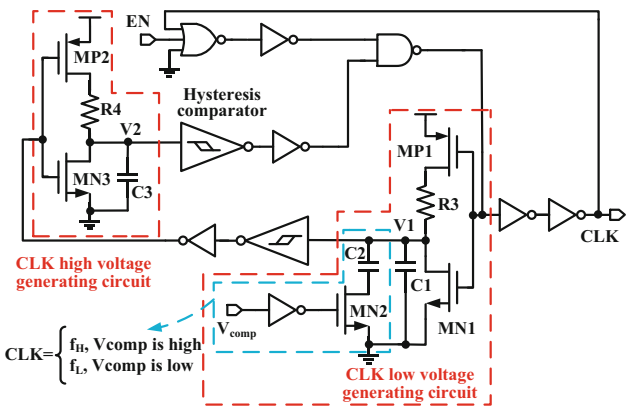


**Fig. 5** Circuit of bi-frequency oscillator

$f_L$:$f_H$ = 1:3. Considering the ripple and efficiency factors, the two frequencies of the oscillator are set as $f_L$ = 50 kHz, $f_H$ = 150 kHz.

### 3.1 System design consideration

Based on the above analysis, the system model of the boost converter, respectively using three control modes, is built in Matlab/Simulink as shown in Fig. 3.

The frequency spectrums of voltage signal *LX* of boost converter, using different modulation methods, are compared in Fig. 4. The comparison of Fig. 4(a), (b), (c) shows that frequency spectrum of *LX* of the boost converter with bi-frequency PFM controller has the most numerous harmonic components, which means that its spectral energy can be dispersed into more frequency points than that of PWM and PFM, so that its discrete harmonic peaks are lower. Consequently, the boost converter has less EMI

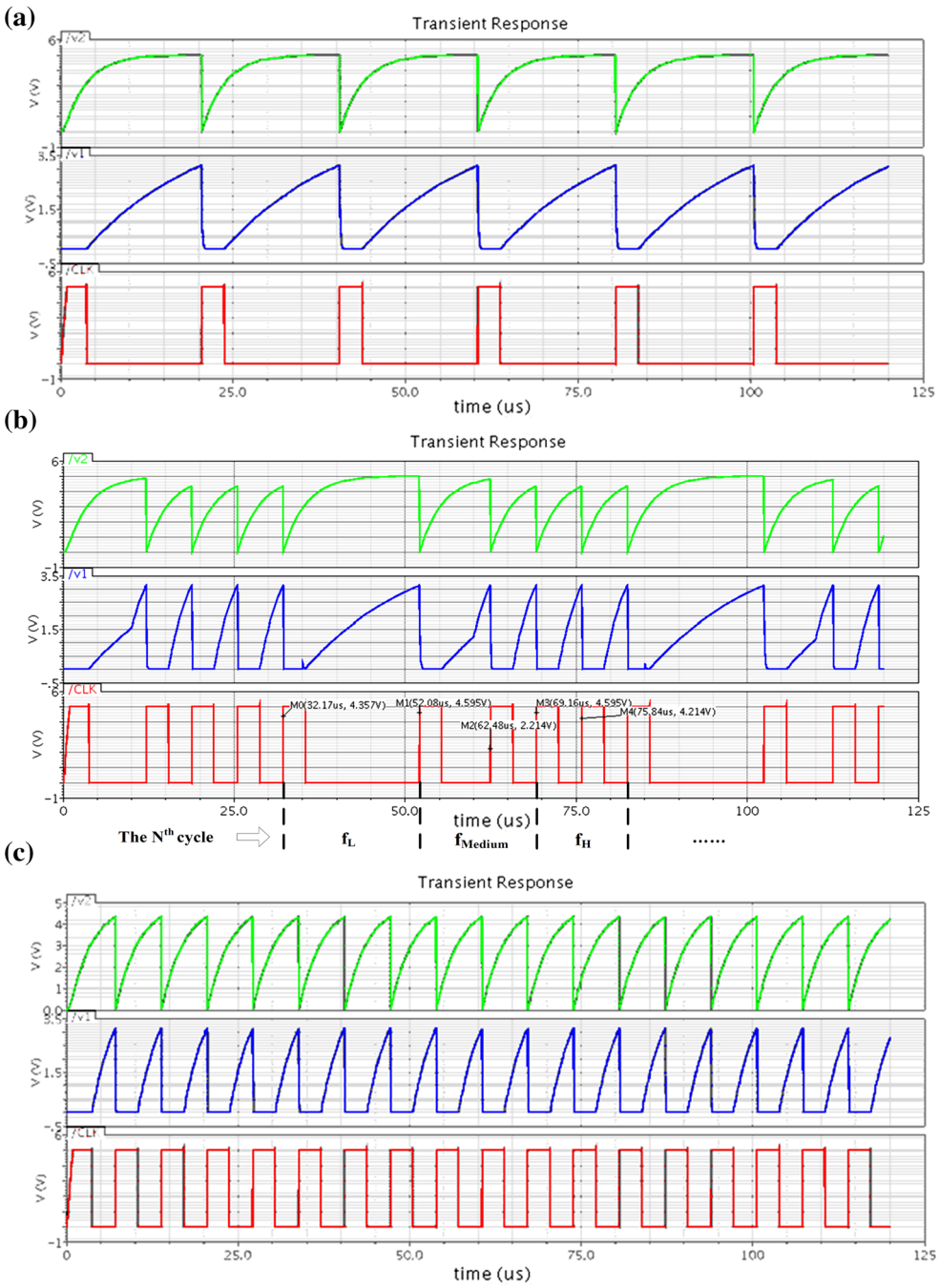


**Fig. 6** *CLK* signal output waveforms under different load currents. **a** Light load ($I_{load}$ = 50 mA). **b** Medium load ($I_{load}$ = 120 mA). **c** Heavy load ($I_{load}$ = 170 mA)

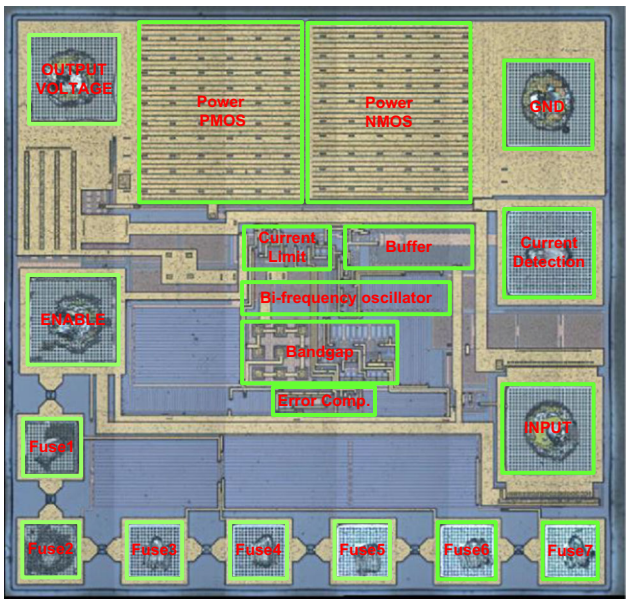


**Fig. 7** Chip layout micro photograph

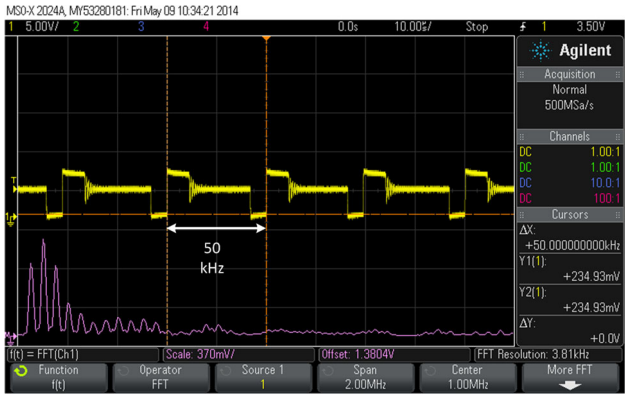


**Fig. 8** The *LX* and $V_o$ waveforms under light load (50 mA)

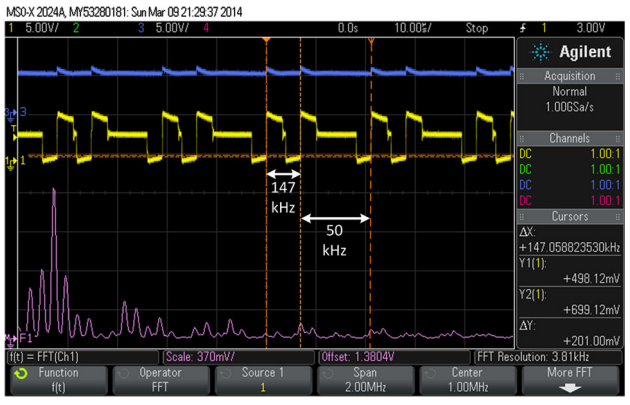


**Fig. 9** The *LX* and $V_o$ waveforms under medium load (120 mA)

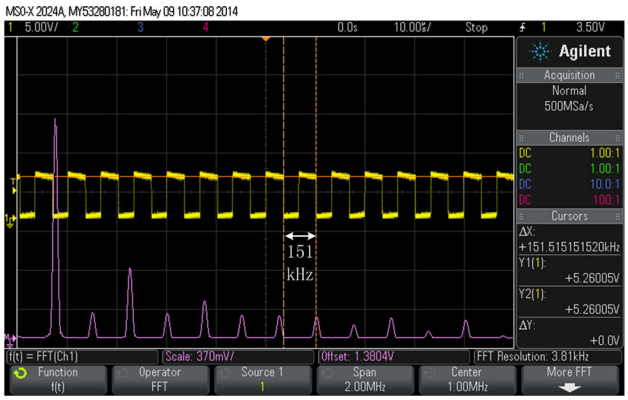


**Fig. 10** The *LX* and $V_o$ waveforms under heavy load (170 mA)

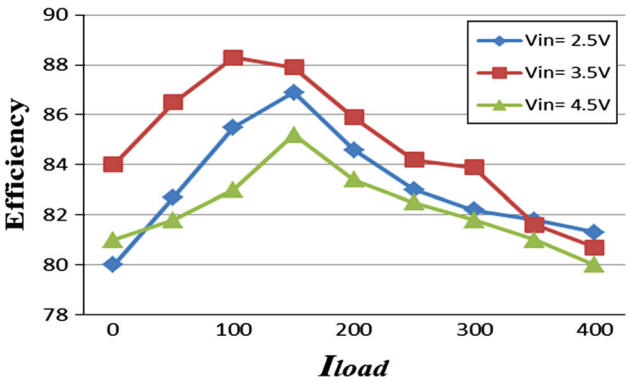


**Fig. 11** Relationship of load current versus conversion efficiency

**Table 1** Main performance of the proposed converter

| Parameter | Text |
|---|---|
| Input voltage range | 2–5 V |
| Operating frequency | $f_L$: 50 kHz; $f_H$: 150 kHz |
| Maximum conversion efficiency | 88.3 % |
| Load regulation ($I_{load}$ = 5–300 Ma) | 2.23 (%/mA) |
| Typical output voltage | 5 V |
| Overall conversion efficiency | >80 % |
| Line regulation (Vin = 2–5 V) | 2.85 (%/V) |

noise and can be easier to meet corresponding EMI standards.

### 3.2 Key circuit design

As shown in Fig. 5, the proposed bi-frequency oscillator is mainly composed by *CLK* low voltage generating circuit, *CLK* high voltage generating circuit, two hysteresis comparators, six inverters, a Nor gate and a Nand gate. $V_{comp}$ is the output signal of voltage comparator in Fig. 1, which

is low when $V_{fb}$ is higher than $V_{ref}$ and high on the opposite. When $V_{comp}$ is high, capacitor C2 does not work, the output signal of *CLK* will be $f_H$, and *CLK* will be $f_L$ when $V_{comp}$ is low. V1, V2 is the output voltage of low voltage generating circuit and *CLK* high voltage generating circuit, respectively. In the bi-frequency oscillator, *CLK* high voltage generating circuit is designed to implement the $T_{on}$ part of the *CLK* signal, while *CLK* low voltage generating circuit, based on the load condition represented in $V_{comp}$, generates the low voltage part of *CLK* to obtain two specific frequency $f_L$ and $f_H$ by changing the charging capacitor between *C1* and *C1* + *C2*, respectively.

The general operation principle is as follows: when the voltage signal *CLK* is low at the beginning, capacitors *C1*, *C3* or *C1*, *C2*, *C3* are charged, the corresponding voltage *V1* and *V2* increase. The increasing speed of *V2* is faster than that of *V1,* but *CLK* does not step to high voltage until *V1* passes the reverse voltage of the hysteresis comparator. Meanwhile, both the voltages of *CLK* and *V1* are high, capacitors discharge quickly, *V1* and *V2* decrease to zero. And then, *C3* is charged, *V2* starts to increase. When *V2* passes the reverse voltage of the hysteresis comparator, *CLK* turns to be low voltage. And that cycle repeats. Therefore, the bi-frequency oscillator outputs low frequency signal $f_L$ at light load, high frequency signal $f_H$ at heavy load, and switches between $f_L$ and $f_H$ to regulate the output voltage $V_o$ at medium load. As Eqs. (3) and (4) illustrate: *CLK* consists of $m$ cycles of $f_H$, and $n$ cycles of $f_L$, the lighter load is, the smaller m and bigger n are, correspondingly, which is consistent with the simulation results in Fig. 6.

Furthermore, input voltage of the circuit is 2.5 V, while output voltage under different load conditions are maintained at about 5 V, so the system can achieve step-up and regulator function.

## 4 Layout design and testing

The proposed controller is fabricated in Founder Microelectronics 0.5 μm CMOS process and the area is 800 μm × 640 μm, as is shown in Fig. 7. Test conditions of the bi-frequency controlled converter are as follows: the input voltage $V_{in} = 2.5$ V, load current $I_{load}$ varies from 0 to 300 mA and the selected central frequency is 1 MHz. Meanwhile, it sweeps from 0 to 2 MHz.

When load current is 50 mA (light load), the LX and $V_o$ waveforms are shown as Fig. 8: the LX square waves are all low frequency signals. A diode connects the output and LX, so there is a certain voltage drop between them. It can be seen that, considering the LX output waveform under medium load (120 mA) in Fig. 9, some high frequency signals appear in the original low frequency signals when increasing the load current. When load current increases to 170 mA (heavy load), all the LX output signals become high frequency, shown in Fig. 10.

The experimental results show that the controller can generate the control signal which switches between two fixed operating frequencies according to load changes: mainly in low frequency under light load, mainly in high frequency under heavy load, and two frequencies coexist in medium load. Therefore, the design of circuit is proved to be valid. In addition, according to the frequency spectrums of voltage signal *LX* showed from Figs. 8, 9, 10, the proposed bi-frequency control scheme is verified to have low EMI.

Figure 11 shows the relationship between the load current and the conversion efficiency, which refers to the ratio of output power and input power. According to Fig. 11, the conversion efficiency is more than 85 % when the load current is 120 mA. Meanwhile, Table 1 also shows that the test results basically meet the requirements of design specification.

## 5 Conclusion

In this paper, a bi-frequency PFM controller for boost DC–DC converter is designed and implemented. The detailed operation principle and design process are presented in this paper. The controller is fabricated in Founder Microelectronics 0.5 μm CMOS process. The experimental results show that the maximum conversion efficiency is up to 88 %, and the quiescent current is under 10 μA. Meanwhile, the spectrum energy is distributed to more frequency points. Therefore, the converter has fine EMI characteristics. So the performance of the prototype can meet the design requirements.

This control method only needs two frequencies, which means that the spectrum peak is more regular, and will be easier for the follow-up filter design to reduce EMI. In essence, the design takes full advantage of the conventional PWM and PFM. However, how to tradeoff efficiency, EMI performance and optimization of the circuit's design, still needs further study.

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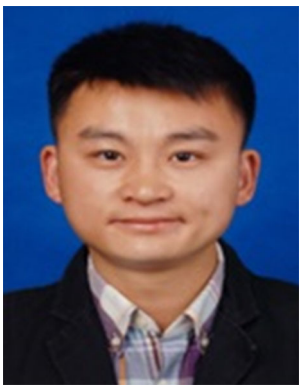

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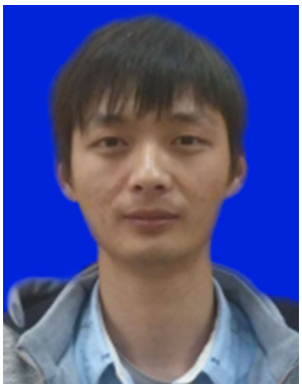

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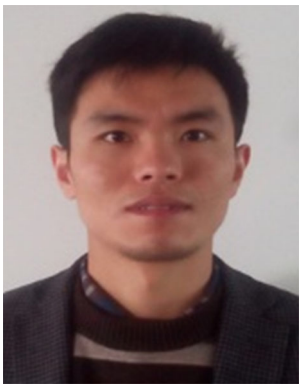

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