

A novel cascading scheme to improve the performance of voltage multiplier circuits

Shailesh Singh Chouhan¹ · Kari Halonen¹

Received: 26 January 2015 / Revised: 15 May 2015 / Accepted: 19 June 2015 / Published online: 5 July 2015
© Springer Science+Business Media New York 2015

Abstract The voltage multiplier (VM) circuit is a cascade arrangement designed from a series of rectifiers to obtain high DC output voltage. In this classical approach, the DC voltage which is getting generated in the present stage contributes to the next stage. This phenomenon is recurring at every stage resulting into higher DC output voltage than previous. The proposed signaling scheme enables the use of the rectified DC voltage/stage in a classical way along with the involvement of instantaneous input RF voltage. As a result, higher output DC voltage and improved power conversion efficiency (PCE) will be achieved as compared to a conventional VM circuit signaling scheme. The conventional VM circuit used in this work was designed by stacked series arrangement of three standard differential drive rectifiers. Similarly, the proposed VM circuit was formed by implementing proposed signaling scheme into the conventional VM circuit. These architectures were implemented in a standard 0.18 μm CMOS technology. The measurements were done by using input RF signal frequency of 433 MHz for resistive load values of 30, 100 $\text{k}\Omega$, and 1 $\text{M}\Omega$ respectively. The measured results show that the proposed VM scheme has 22–32 % better power conversion efficiency than the conventional VM scheme.

Keywords CMOS implementation · RF energy harvesting · Voltage multiplier circuit · Power conversion efficiency · Differential drive rectifier · RF-to-DC converter · Rectifier

1 Introduction

The use of RF energy harvesting is widely spreading in wireless sensor nodes and radio frequency identification (RFID) applications [1]. An RF-to-DC converter or rectifier is one of the primary key components which is present in a harvesting unit. It is used to convert the received RF energy into a DC voltage to power up the associated system [2]. Various architectures are available in literature to implement the RF-to-DC converter or rectifier. The most common method is the use of Schottky diode, as it offers low forward voltage and high switching speed [3, 4]. But the requirement of additional manufacturing steps limits its ON-chip usage. As an alternative to Schottky diodes, complementary metal oxide semiconductor (CMOS) transistors are used since it offers ease in bulk manufacturing. But, the performance of a CMOS based rectifier gets limited by the threshold voltage (V_{th}) of metal oxide semiconductor field effect transistor (MOSFET) used in implementation. In order to overcome this limitation two approaches are suggested in literature.

First is the device based approach, where special transistors like zero- V_{th} transistors [5] are used in designing the rectifier circuit.

In the second method, threshold voltage influence in MOSFET has been reduced by the use of circuit based arrangements. This approach is broadly classified into three parts; internal V_{th} cancellation (IVC), external V_{th} cancellation (EVC) and self V_{th} cancellation (SVC) based schemes. In the internal V_{th} cancellation scheme, threshold voltage has been reduced by the use of an additional CMOS circuit, which is powered up by using the rectified DC voltage [6]. While in the external V_{th} cancellation approach, the threshold voltage effect in MOSFET is reduced by the use of additional DC sources [7]. Finally in self V_{th} cancellation scheme, threshold voltage of

✉ Shailesh Singh Chouhan
sirshailesh@gmail.com; shailesh.chouhan@aalto.fi

Kari Halonen
kari.halonen@aalto.fi

¹ Department of Micro and Nano Sciences, Aalto University, Espoo, Finland

transistors has been reduced by utilizing positive feedback mechanism [8].

In general, a DC voltage level attended by the rectifier is not sufficiently high ($<3 V_{th}$). Thus to obtain higher DC voltage level, the multistage rectifier implementation has been adopted. This implementation is often known as the voltage multiplier (VM) circuit in literature. Most of the VM circuits are based on the classical Dickson’s charge pump topology [9, 10]. The performance of the multistage rectifier is affected more due to the threshold voltage of the transistor as compared to a single stage rectifier. In [11], various architectures for the voltage multiplier circuit have been proposed, which are suitable for a low input power levels. Similarly, the use of capacitor-bootstrapped transistors have been proposed in [12], to overcome the threshold voltage influence in the rectifier. The implementation by using cross-coupled rectifier proposed in [13], which offers improved power efficiency and reduction in loss due to the threshold voltage in a voltage multiplier circuit.

The RF-to-DC module which has used in this work for the implementation of voltage multiplier arrangement (Fig. 1) was selected from [14]. The rectifier circuit arrangement proposed in [14] is the cross-coupled bridge configuration and also known as differential drive rectifier.

It was suggested in the work that due to the differential drive active gate bias mechanism, the rectifier is capable of achieving low ON-resistance and small reverse leakage during the forward and the reverse conduction modes respectively. The measurement results of a three stage voltage multiplier were also presented in [14]. The measured performance has exhibited the peak power conversion efficiency of 65 % at a resistive load of 30 K Ω for an input RF power level of -6 dBm at 953 MHz RF frequency.

Here in this work, the VM arrangement proposed in [14] has been modified by attaching a storage capacitor after each stage and is designated as the conventional VM circuit. This architecture is present ON-chip for the comparison purpose.

In this work, a signaling scheme is proposed to be used in forming multistage rectifier. It has been found by the measurement that the voltage multiplier circuit, which was

designed by using the proposed signaling scheme has shown an improved performance over the voltage multiplier circuit that was formed by using conventional cascading method. The paper is organized as follows: the voltage multiplying action of the conventional VM circuit has been discussed in Sect. 2. The proposed signaling scheme is presented in Sect. 3. The results have been discussed in the Sect. 4 and the conclusions are in Sect. 5.

2 Architecture of the conventional voltage multiplier circuit

The N-stage conventional VM circuit based on [14] is shown in Fig. 1. The circuit is modified by connecting a storage capacitor (C_s) per stage. The storage capacitor is responsible to minimize the ripple voltage of the rectified DC output.

The working principle of the conventional VM circuit is explained by using a conceptual diagram shown in Fig. 2. In the figure, $\pm V_p$ are the peak input RF signal amplitudes, V_{dn} and V_{dp} represents the voltage drop across nMOSFET and pMOSFET respectively, C_p is the pumping capacitor, V_{dcx} represents the rectified DC voltage per stage of the VM circuit where $x = 1, 2, \dots, (N - 1)$, and C_s is the storage capacitor.

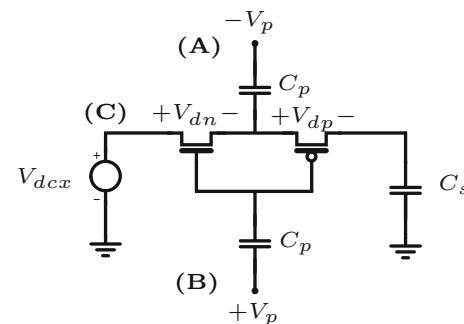
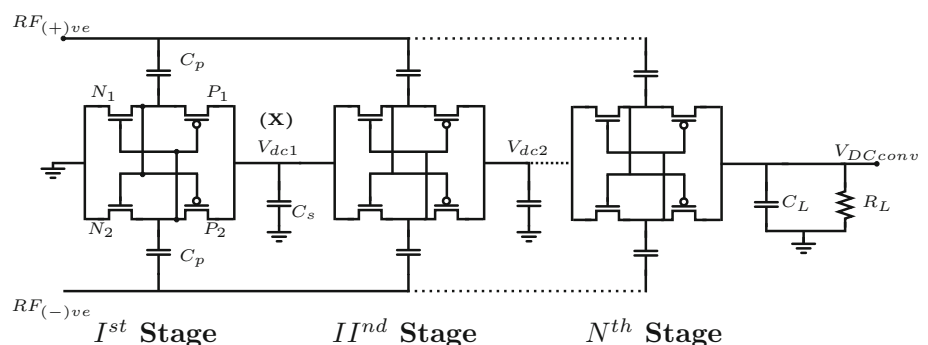


Fig. 2 Conceptual circuit diagram of the Nth stage of the voltage multiplier circuit

Fig. 1 Conventional method to form voltage multiplier



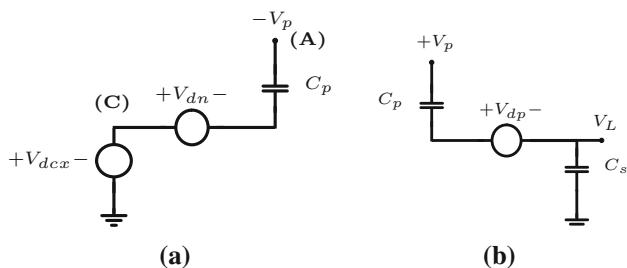


Fig. 3 **a** Charging and **b** discharging phase of the single stage differential drive rectifier

It should be noted that the analysis of charge transfer in a typical rectifier is quite complex as explained in [15] for a complete RF input cycle. This complexity is due to different operation regions of the transistors used in the rectifier design. Hence, to develop a simple working model two assumptions have been made. First, the RF signal amplitude is greater than the threshold voltage (V_{th}) of the transistor. Second, the lossless transfer of electronic charge will occur during charging and discharging cycles of the capacitor.

When the positive-RF signal amplitude will appear at terminal (B) (Fig. 2) nMOSFET will turn ON and hence, the rectifier will enter into the charging phase as shown in Fig. 3.

By applying Kirchoff’s Voltage Law (KVL) in the charging path (Fig. 3a),

$$-V_p = V_{cp} - V_{dn} + V_{dcx} \tag{1}$$

The peak voltage (V_{cp}) developed across the capacitor C_p during the charging phase will be,

$$V_{cp} = -V_p + V_{dn} - V_{dcx} \tag{2}$$

Similarly, when a negative-RF voltage signal will appear at the terminal (B), pMOSFET will turn ON and hence, the rectifier will enter into the discharging phase (Fig. 3b). In this phase, charges stored in C_p will be transferred to C_s without any loss. By applying KVL in the discharging path,

$$V_p = V_{cp} + V_L + V_{dp} \tag{3}$$

and substituting (2) in (3),

$$V_p = -V_p + V_{dn} - V_{dcx} + V_L + V_{dp} \tag{4}$$

rearranging (4) will result as,

$$V_L = 2 \cdot V_p + V_{dcx} - (V_{dn} + V_{dp}) \tag{5}$$

The condition $V_{dcx} = 0$ signifies the charging/discharging operation of the 1st stage. Hence, the rectified DC voltage (V_{dc1}) from 1st stage will be obtained by substituting this condition in (5),

$$V_{dc1} = V_L = 2 \cdot V_p - (V_{dn} + V_{dp}) \tag{6}$$

The voltage V_{dc1} will act as a DC source for second stage. Thus, voltage developed across C_p during charging phase will be obtained by substituting (6) in (2)

$$V_{cp} = -3 \cdot V_p + 2 \cdot V_{dn} + V_{dp} \tag{7}$$

The rectified DC-output voltage from the second stage after discharging phase will be,

$$V_{dc2} = 4 \cdot V_p - 2 \cdot (V_{dn} + V_{dp}) \tag{8}$$

By referring (5) and (7), and using the principle of recursion, the DC-output voltage after N th stage of the conventional VM will be,

$$V_{DCconv} = \underbrace{2N \cdot V_p}_a - \underbrace{N \cdot (V_{dn} + V_{dp})}_b \tag{9}$$

Three observations can be obtained from the equation (9); first, the presence of the multiplying factor of 2 indicates that the differential drive rectifier is the voltage doubler architecture. Second, part (a) in (9) is the ideal DC output voltage from the voltage multiplier. Finally, part (b) is the total voltage loss that occurs in pMOSFET and nMOSFET due to the threshold voltage. It can be noticed that the loss will increase with the increase in the number of stages (N).

Part (b) is one of the main reasons that, restricts the number of stages in the VM circuit [11].

3 Proposed cascading scheme

In the literature two approaches have been suggested in order to eliminate or reduce part (b) of equation (9). First, the use of zero- V_{th} transistors [5, 16] but this will increase power conversion efficiency at a cost of high reverse/OFF-state leakage current. Second approach is the use of auxiliary voltage source to compensate part (b), which is as shown follows,

$$V_{dc} = 2N \cdot V_p - N \cdot (V_{dn} + V_{dp}) + V_{aux} \tag{10}$$

where V_{aux} is the auxiliary voltage source that can be obtained either externally [7] or internally [16].

Figure 4 shows the schematic of the proposed signaling scheme to develop the auxiliary voltage V_{aux} by using the input RF signal. In this architecture (Fig. 4) two simple modifications have been implemented in the conventional VM circuit (Fig. 1). First, the storage capacitor (C_s) has been split into two capacitors (C_{s1}, C_{s2}) with a capacitance value of $C_s/2$ to maintain equal layout area. This arrangement is possible due to the differential architecture of the rectifier, as only an opposite pair of transistors are active i.e. P_1 and N_2 in first half cycle where as P_2 and N_1 in other half cycle (Fig. 1). Second, one terminal of the capacitor

Fig. 4 Proposed cascade arrangement method to form voltage multiplier

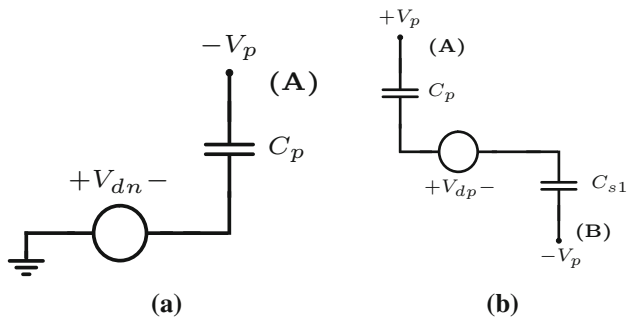
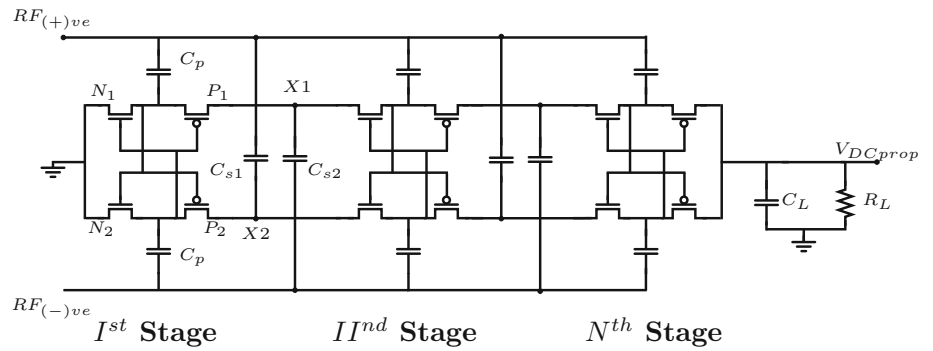


Fig. 5 **a** Charging and **b** discharging phase of first stage of proposed arrangement

(C_{s1}, C_{s2}) has been connected to complementary RF signal line. As a result, during discharging phase, the complementary input RF signal will also contribute in the development of an additional DC voltage.

The charging and discharging phase of the first stage is shown in Fig. 5. The voltage across pumping capacitor (C_p) during the charging phase will be given by,

$$V_{cp} = -V_p + V_{dn} \tag{11}$$

Similarly, by applying KVL in the discharging path (Fig. 5b) will result in,

$$V_p = V_{cp} + V_{dp} + V_{cs1} - V_p \tag{12}$$

Voltage (V_{cs1}) generated across the smoothing capacitor (C_{s1}) during the discharging phase can be obtained by substituting (11) in (12),

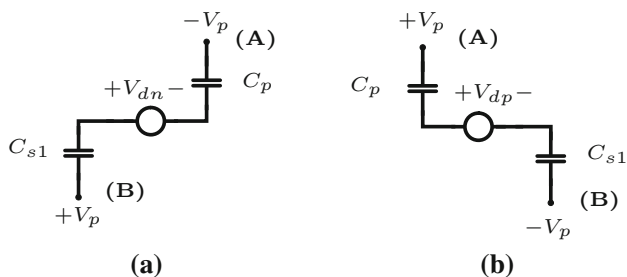


Fig. 6 **a** Charging and **b** discharging phase of the second stage of proposed arrangement

$$V_{cs1} = 3 \cdot V_p - (V_{dn} + V_{dp}) \tag{13}$$

In the proposed circuit the charging and discharging phase from the second stage (Fig. 6) will be different from the first stage, since now C_{s1} is also contributing in pumping the charges. By applying KVL in the charging path (Fig. 6a) of the second stage, it is obtained that,

$$-V_p = V_{cp} - V_{dn} + V_{cs1} + V_p \tag{14}$$

The voltage generated across C_p during the charging phase at the second stage can be obtained by substituting (14) in (13). It will result as,

$$V_{cp} = -5 \cdot V_p + V_{dn} + (V_{dn} + V_{dp}) \tag{15}$$

Similarly, the voltage developed across C_{s1} during the discharging phase can be obtained by substituting (15) in (16). The resultant equation for this voltage (V_{cs1}) is shown in (17).

$$V_p = V_{cp} + V_{dp} + V_{cs} - V_p \tag{16}$$

$$V_{cs1} = 7 \cdot V_p - 2 \cdot (V_{dn} + V_{dp}) \tag{17}$$

Hence, referring to (13), (17) and using the principle of recursion analysis, the voltage, which will appear across C_{s1} at the start of the charging phase of N th stage will be given by,

$$V_{cs1} = (4N - 1) \cdot V_p - N \cdot (V_{dn} + V_{dp}) \tag{18}$$

The conceptual diagrams shown in Fig. 6 for charging and discharging phases are also applicable to N th stage. Hence, by applying KVL in the charging path and using (18), the voltage developed across C_p will be given as,

$$V_p = -2 \cdot V_p - (4N - 1) \cdot V_p + 2N \cdot (V_{dn} + V_{dp}) + V_{dn} \tag{19}$$

Finally, the output DC voltage of the proposed voltage multiplier arrangement will be obtained by applying KVL in the discharging path and using (19) as,

$$V_{DCprop} = (4N + 2) \cdot V_p - N \cdot (V_{dn} + V_{dp}) \tag{20}$$

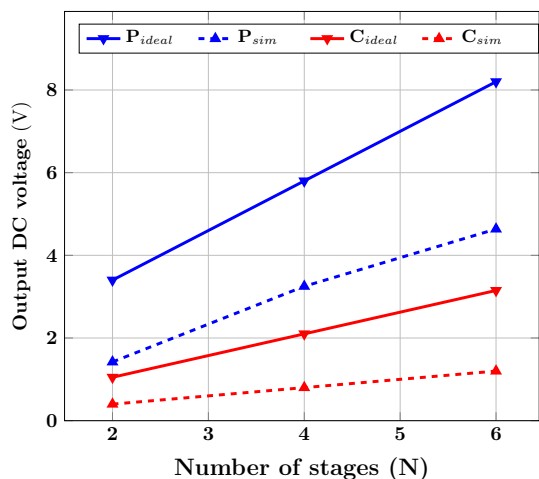
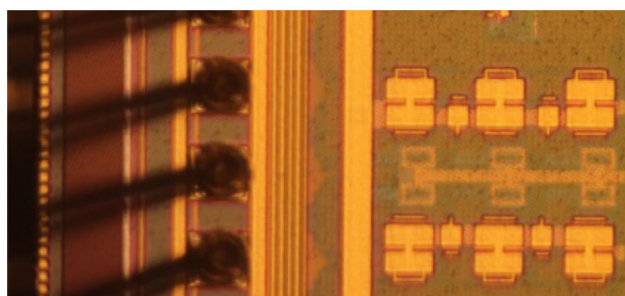
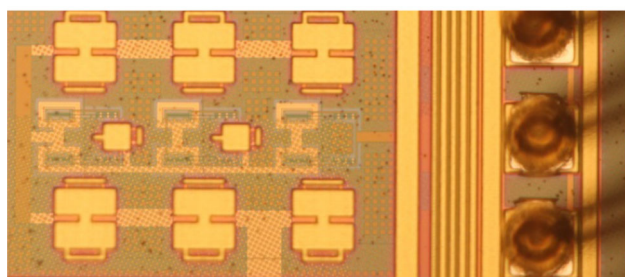


Fig. 7 Ideal and simulated plots of conventional (C_{ideal} and C_{sim}) and proposed (P_{ideal} and P_{sim}) voltage multiplier circuits



(a)



(b)

Fig. 8 Micrograph of **a** conventional and **b** proposed voltage multiplier circuit

The plot for an ideal DC voltage from the conventional and proposed voltage multipliers by using (9) and (20) respectively is shown in Fig. 7. In this plot equation (9) is marked as C_{ideal} and P_{ideal} respectively. These plots are made for peak input voltage $V_p = 0.5$ V, with the voltage loss of $(V_{dn}, V_{dp}) = 0.3$ V. It should be noted that this voltage loss across transistors has been estimated from the transient simulations. Similarly, the simulated values of output DC voltages obtained from the various number of stages of the proposed and the conventional voltage

Table 1 Device dimensions of the CMOS components

S. No.	Device	Size
1	pMOSFET	$2 \times 20/0.2 \mu\text{m}$
2	nMOSFET	$2 \times 20/0.2 \mu\text{m}$
3	C_p	5 pF
4	C_s	1 pF

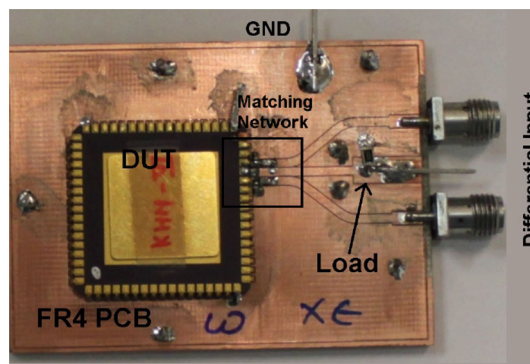


Fig. 9 Printed circuit board used in the measurement

multipliers are shown as P_{sim} and C_{sim} respectively for capacitive load of 5 pF. These transient simulations were done in the Cadence environment using Spectre simulator.

It can be observed in Fig. 7 that the simulated behaviours trend of voltage multipliers is in agreement with the ideal equations (9) and (20).

4 Measurement results

The proposed and the conventional VM circuits were fabricated in standard 0.18 μm CMOS technology. The micrographes of the designs are shown in Fig. 8. The layout area of each circuit is $250 \mu\text{m} \times 350 \mu\text{m}$. In the implementations, the body terminal of the transistors was tied to the source terminal to avoid body effect and the gate-oxide stress from gate to bulk. The dimensions of the CMOS components used in the architecture are listed at Table 1. These dimensions were determined by using simulation based approach. The simulations were done by using the Cadence Spectre simulator. The transient and the harmonic balance analysis were used in finalizing the device sizes.

4.1 Measurement setup

A printed circuit boards (PCB) (Fig. 9) with standard FR4 substrate, which have been used in the measurements were milled in the laboratory. The length of the RF signal feed line used in the PCB was determined using the Agilent

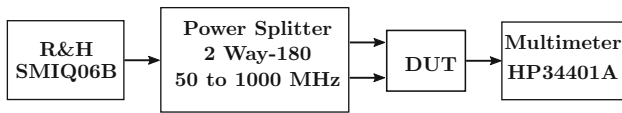


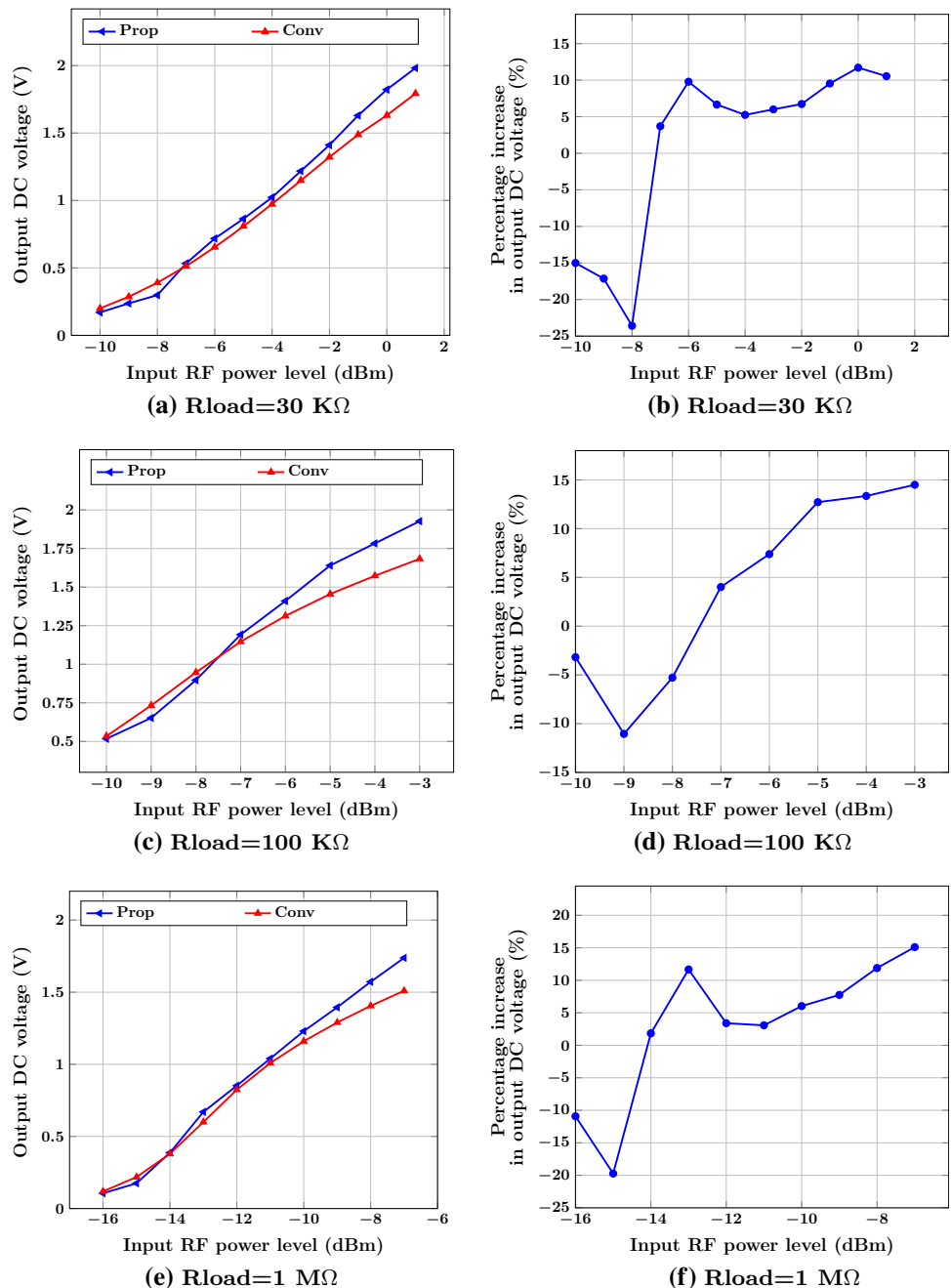
Fig. 10 Block diagram of the measurement setup

ADS simulator. The ICs were directly soldered on the board to minimize parasitic effects during measurements. The single port S-parameters were measured using the port extension feature of Agilent 8722ES network analyzer. These S-parameters were converted into mixed mode

S-parameters by using the Matlab program in order to determine the input impedance of the rectifiers. Later, these impedance values were used in the Agilent ADS simulator to determine the discrete component’s values required to design the matching network for each of the rectifier. It should be noted that, the matching networks were designed individually for each rectifier only for the resistive load of 30 KΩ. The load characterization of the rectifiers were done without changing matching networks.

The block diagram of the measurement setup is shown in Fig. 10. The input RF signal of frequency 433 MHz was provided by R&H SMIQ06B signal generator and split into

Fig. 11 The measured output DC voltage values and percentage increase in output DC voltage values for the various input RF power level at different resistive load values



the differential signal using the 50 Ω balun [17]. This differential signal was fed into the device under test (DUT) and the rectified DC output values were measured using multimeter HP34401A.

4.2 Measurement results

In the measurement, the load conditions were emulated using the surface mount resistors of values 30, 100 KΩ and 1 MΩ. The measured output DC voltages for both architectures are shown in Fig. 11. The percentage

increase in the output DC voltage after implementing proposed scheme are also shown in Fig. 11. It can be noticed in Fig. 11 that the proposed VM is capable of generating higher DC voltage values compared with the conventional architecture. These improvements in output DC voltages are approximately in the range of 100 to 500 mV depending on input power level and load condition. The measured output DC voltage values obtained from the proposed VM circuit were not as high as expected in the first order theoretical analysis (20) and (9).

Fig. 12 The measured power conversion efficiency (PCE) and the percentage increase in PCE values for the various input RF power level at different resistive load values

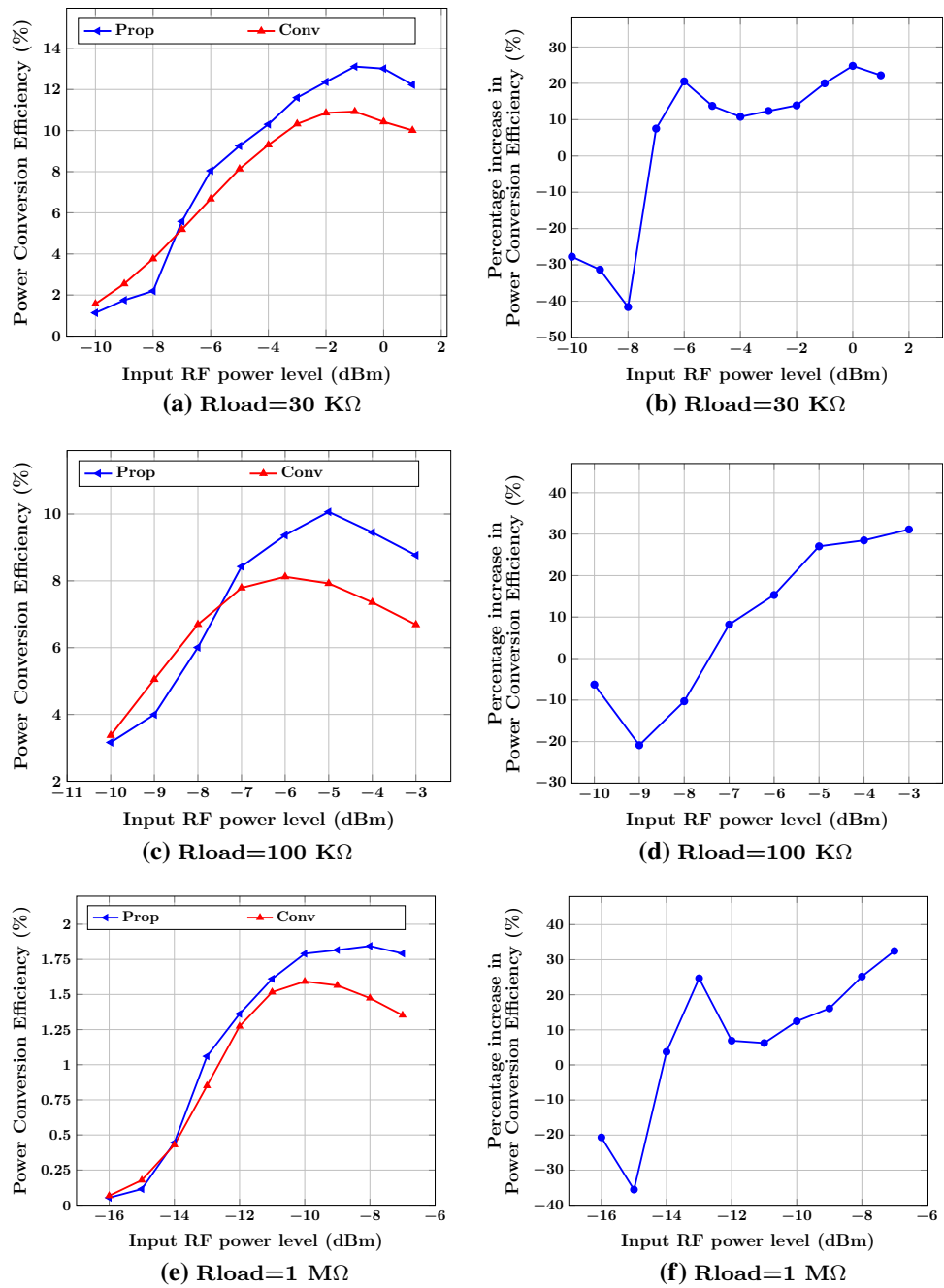


Table 2 Mixed mode parameters

Architecture	$ S_{dd11} $	$ S_{cd11} $
Conventional VM	0.3745	0.0263
Proposed VM	0.3929	0.0247

To further improve the performance of the proposed rectifier following guidelines are suggested. These guidelines were determined by performing a schematic-level, simulations-based optimization of the proposed three stage voltage multiplier. These simulations were performed by considering following constraints to maximize PCE.

increase in the power conversion efficiency performance is 22–32 %. These values can be further improved by applying the modifications suggested above.

It can also be noticed from Fig. 12, that the numerical values of the measured power conversion efficiencies for both of the architectures are less compared with the power conversion efficiency values reported in [14]. One of the primary reasons for these reductions were the difference in the measurement setup used. The authors from [14] used probing and the mixed mode S-parameters were obtained directly from the fully differential Agilent PNA-X vector analyser.

$$PCE(\%) = f \begin{cases} W_{1,2,3} & \text{Width of transistors of Stage – I, II, and III} \\ C_{p1,p2,p3} & \text{Sizes of pumping capacitors used in Stage – I, II, and III} \\ C_{s1,s2,s3} & \text{Sizes of storage capacitors used in Stage – I, II, and III} \end{cases} \quad (21)$$

Following conclusions were resulted from the simulations,

1. Select $W_3 > W_2 > W_1$ but this increment should not be more than 25 % per stage.
2. Select pumping capacitor (C_p) of same size i.e. $C_{p1} = C_{p2} = C_{p3}$, but with large value of capacitance as it will decide the size of storage capacitors.
3. Select $C_{s1} > C_{s2} > C_{s3}$ and the value of storage capacitor (C_s) should be small ($\approx 1/30$) as compared to pumping capacitor (C_p).

The performance of both of these architectures were also measured in terms of power conversion efficiency (PCE) which is expressed as follows,

$$PCE(\%) = 100 \cdot \frac{P_{out}}{P_{in}} \quad (22)$$

where P_{out} is the output DC power given by,

$$P_{out} = \frac{V_{dc}^2}{R_L} \quad (23)$$

While the input power P_{in} was selected from [8],

$$P_{in} = P_s \cdot [1 - |S_{dd11}|^2 - |S_{cd11}|^2] \quad (24)$$

where P_s is the RF power level after balun, S_{dd11} and S_{cd11} are the mixed mode differential-to-differential and differential-to-common mode reflection coefficients respectively.

The measured PCE plots and the corresponding percentage increase in PCE over the conventional architecture are shown in Fig. 12. It can be observed that the proposed method is capable of improving the performance of the conventional cascading arrangement. The percentage

In this work, the DUT was soldered on the PCB (Fig. 9) and a single ended S-parameters were first measured using the Agilent 8722ES network analyzer. These S-parameters were then converted into the mixed mode S-parameters using a Matlab program, which are listed in Table 2.

5 Conclusion

In this work a signalling scheme was proposed which is capable of increase performance of the conventional VM circuit. The implementation of the proposed scheme was done in the three stage conventional voltage multiplier circuit. The effectiveness of this scheme was verified by measurements for different resistive load values. The measured results show that the output DC voltage and the power conversion efficiency of the conventional voltage multiplier circuit has been improved after implementing proposed scheme in it. The design strategy is suggested to further improve the performance of the proposed architecture. It is noted that, the proposed scheme is also suitable for other existing differential rectifier architectures which are used in the application of RF energy harvesting. Based on measured statistics the proposed VM architecture is useful for high proximity RFID applications such as logistic tags, smart cards and healthcare.

Acknowledgments This work is funded by the projects AUTO-VOLT of the Academy of Finland and EFFINANO of the Aalto University, Finland.

References

- Pinuela, M., Mitcheson, P., & Lucyszyn, S. (2013). Ambient RF energy harvesting in urban and semi-urban environments. *IEEE Transactions on Microwave Theory and Techniques*, 61(7), 2715.
- Finkenzeller, K. (2003). *RFID handbook: Fundamentals and applications in contactless smart cards and identification*. New York: Wiley.
- Jabbar, H., Song, Y. S., & Jeong, T. T. (2010). RF energy harvesting system and circuits for charging of mobile devices. *IEEE Transactions on Consumer Electronics*, 56(1), 247.
- Chen, L. Y., Mao, L. H., & Huang, X. Z. (2011). Design and analysis of a low power passive UHF RFID transponder IC. *Analog Integrated Circuits and Signal Processing*, 66(1), 61.
- Theilmann, P. T., Presti, C. D., Kelly, D. J., & Asbeck, P. M. (2012). A μW complementary bridge rectifier with near zero turn-on voltage in SOS CMOS for wireless power supplies. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 59(9), 2111.
- Nakamoto, H., Yamazaki, D., Yamamoto, T., Kurata, H., Yamada, S., Mukaida, K., et al. (2007). A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35 μm technology. *IEEE Journal of Solid-State Circuits*, 42(1), 101.
- Umeda, T., Yoshida, H., Sekine, S., Fujita, Y., Suzuki, T., & Otaka, S. (2006). A 950-MHz rectifier circuit for sensor network tags with 10-m distance. *IEEE Journal of Solid-State Circuits*, 41(1), 35.
- Kotani, K., Ito, T. (2007). High efficiency CMOS rectifier circuit with self-V_{th}-cancellation and power regulation functions for UHF RFIDs. In: *IEEE Asian solid-state circuits conference* (p. 119).
- Dickson, J. F. (1976). On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique. *IEEE Journal of Solid-State Circuits*, 11(3), 374.
- Joonhyung, L., Cho, H., Cho, K., Tahjoon, P. (2009). High sensitive RF-DC rectifier and ultra low power DC sensing circuit for waking up wireless system. In: *Asia Pacific microwave conference* (p. 237).
- Papotto, G., Carrara, F., & Palmisano, G. (2011). A 90-nm CMOS threshold-compensated RF energy harvester. *IEEE Journal of Solid-State Circuits*, 46(9), 1985.
- Ebrahimian, M., El-Sankary, K., & El-Masry E. (2010). Enhanced RF-to-DC CMOS rectifier with capacitor-bootstrapped transistor. In: *IEEE international symposium on circuits and systems* (p. 1655).
- Karolak, D., Taris, T., Deval, Y., Begueret, J. B., & Mariano, A. (2012). Design comparison of low-power rectifiers dedicated to RF energy harvesting. In: *IEEE international conference on electronics, circuits and systems* (p. 524).
- Koji, K., Atsushi, S., & Ito, T. (2009). High-efficiency differential-drive CMOS rectifier for UHF RFIDs. *IEEE Journal of Solid State Circuits*, 44(11), 3011.
- Yi, Jun, Ki, Wing-Hung, & Tsui, Chi-ying. (2007). Analysis and Design Strategy of UHF Micro-Power CMOS Rectifiers for Micro-Sensor and RFID Applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 54(1), 153.
- Matias, M. L., Cunha, J. P. C., Dal Fabbro, P. A., Mioni, D., Prodanov, W., Pessatti, M., Leite, B., & Mariano, A. (2014). A comparison of high-efficiency UHF RFID rectifiers using internal voltage compensation and zero-threshold-voltage MOSFETs. In: *Latin American symposium on circuits and systems* (p. 1).
- Data sheet for 2 way-180°, 50 Ω , 50 to 1000 MHz Coaxial power splitter/combiner from mini circuits, Retrieved from <http://194.75.38.69/pdfs/ZFSCJ-2-4+>.



Shailesh Singh Chouhan received the B.E. and M.E. degrees in Electronics Engineering from the Institute of Engineering and Technology, Devi Ahilya University, Indore, India, in 2001 and 2006, respectively. He has been served as assistant professor in the Department of Electronics and Telecommunication IET Devi Ahilya University Indore, India during 2001–2010. Since 2011 he is with ECD group, Department of Micro and Nano sciences, Aalto University and is working towards his doctoral degree. His research interests involve design of RF energy harvesting circuits, integrated temperature sensors and ADCs.



Kari Halonen received the M.Sc. degree in Electrical Engineering from the Helsinki University of Technology, Finland, in 1982, and the Ph.D. degree in electrical engineering from the Katholieke Universiteit Leuven, Belgium, in 1987. Since 1988 he has been with the Electronic Circuit Design Laboratory, Helsinki University of Technology (since 2011 Aalto University). From 1993 he has been an associate professor, and since 1997 a full professor at the Faculty of Electrical Engineering and Telecommunications. He became the Head of Electronic Circuit Design Laboratory in 1998 and he was appointed as the Head of Department of Micro and Nano Sciences, Aalto University, in 2007–2013. He specializes in CMOS and BiCMOS analog and RF integrated circuits, particularly for telecommunication and sensor applications. He is author or co-author over 450 international and national conference and journal publications on analog and RF integrated circuits. Prof. Kari Halonen has been an associate editor of *IEEE Journal of Solid-State Circuits*, and an associate editor of *IEEE Transactions on Circuits and Systems I*, a guest editor for *IEEE Journal of Solid-State Circuits*, and the Technical Program Committee Chairman for European Solid-State Circuits Conference 2000 and 2011. He has been awarded the Beatrice Winner Award in ISSCC Conference 2002. He has served as a TPC member of ESSCIRC and ISSCC.