Analog Integr Circ Sig Process (2015) 84:215–222
DOI 10.1007/s10470-015-0551-x

A 2:1 switched-capacitor DC–DC converter for low power circuits

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Received: 8 August 2014 / Revised: 18 April 2015 / Accepted: 25 April 2015 / Published online: 10 May 2015

Abstract This paper presents a 2:1 low power switched-capacitor DC–DC converter designed in 180 nm Standard CMOS technology. The converter operates from 1.8 V input and delivers a 0.8 V power supply with 50 mA load current. Simplicity and power efficiency improvement is the main goal of this design. The achieved efficiency of the converter is more than 80 %. Also, high power efficiency, high current delivery, small size, low output voltage ripples are some main properties of the proposed DC–DC converters. The converter occupies about an area of 1 mm^2. Besides, switching frequency of the switched-capacitor DC-DC converter has been increased to reduce output voltage ripples. Maximum output voltage ripple is about 21 mV. Power saving in gate driver stage is the method used in this design to improve the power efficiency. Also, a little changes applied in non-overlapping clock signal generator to gain a better power efficiency. During the design procedure, the main power loss sources have been explained and their solutions have been presented.

Keywords DC–DC converter · Switched-capacitor · Power managment · Power efficiency

1 Introduction

During the recent years, technology development have been led to great revolutions in portable electronics industry. The size of the portable electronic devices are getting smaller and smaller and simultaneously their performances are increasing. Portable batteries (such as Li-ion batteries) are the main power source of these devices. The batteries produce a nominal voltage, but different parts of the integrated circuits need other DC voltage levels as their power supply. Therefore, power managment units are imperative for portable electronic devices. A power managment unit takes varying voltage of the battery and converts it to a desired fixed and smooth output voltage. One of the main components of the power managment unit is DC–DC converters. They are also known as switching voltage regulators. A DC–DC converter is a device that receives a DC input voltage and provides a DC output Voltage. In the step-down DC–DC converter, the output voltage level is lower than the input voltage. DC–DC converters have three main types [6]: Linear converters, Magnetic switching converters and Switched-capacitor converters. Switched capacitor converters are prefered because of their smaller size compared to magnetic switching converters. They can reach higher efficiency than linear regulators with large dropout voltage. They also can provide higher or opposite polarity voltages. But switched capacitor converters have some disadvantages too [6]: They have lower output current than magnetic regulators. They are also less efficient than magnetic switching regulators. In this paper we designed a simple 2:1 switched-capacitor step-down DC–DC converter for low power circuits. It is clear that the circuits which use switched-capacitor DC–DC converter as their power supply must have the same technology used in, i.e. 180 nm Standard CMOS as currently considered.

2 Power losses study

The ratio between the output power (P_{OUT}) and the total input power (P_{IN}) is called power efficiency:

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$$\eta_P = \frac{P_{OUT}}{P_{IN}}$$

The difference between the total input power and the output power is called power loss (P_{LOSS}):

$$P_{LOSS} = P_{IN} - P_{OUT} = P_{OUT}\left(\frac{1}{\eta_P} - 1\right)$$

It is notable that the power loss mainly appears as heat. It can affect the other parts of the converter, which will reduce the overall reliability of the system. Practically, power efficiency improvement is the main goal of switched-capacitor converters. Thus, we have to decrease the main power losses arising from switching MOSFETs and gate drivers (buffers). The main power losses in the switching MOSFETs are: conduction loss, switching loss and gate drive loss. In the design process, we should consider an appropriate balance between these losses to gain a optimum result. The conduction loss (P_R) in a MOSFET switch can be given by [10]:

$$P_R = R_{on} \cdot I^2_{on_{(rms)}}$$

where R_{on} is the non-zero on-resistance of a MOSFET switch and $I_{on_{(rms)}}$ is an RMS value of the drain current. It is clear that R_{on} happens in the active region of a MOSFET switch ($V_{DS} < V_{GS} - V_{th}$). The ideal model approximation of R_{on} can be expressed as:

$$R_{on} \approx \frac{V_{DS}}{I_D} = \left[\frac{\mu \cdot C_{ox} \cdot W}{L}(V_{GS} - V_{th})\right]^{-1}$$

In order to achieve a low value of conduction loss, R_{on} has to be low as possible by increasing the $\frac{W}{L}$ ratio of the transitor into a optimum value. But it should be concidered that at the same time, the gate parasitic capacitance is increasing too. The other source of conduction losses (P_E) is because of the capacitors' parasitic equivalent series resistance (R_{ESR}) [2] and can be expressed as:

$$P_E = R_{ESR} \cdot I^2_{OUT}$$

This kind of power loss arises out of metal wiring resistance on the chip and a non-negligible resistsnce in the external capacitors. Thus, the resistance of the essential paths which lead to capacitors should be reduced. In this design, we selected the minimum length paths with suitable big width or paralleled several metals (where needed) to gain the best result.

The second main power loss is switching loss (P_S). It is because of non-zero switching time of the MOSFET switch i.e. a overlap between turning the switch on and off. This kind of power loss can be shown as [11]:

$$P_S = \frac{1}{2} V_{DS} \cdot I_D \cdot (t_{SWon} + t_{SWoff}) \cdot f_{sw}$$

where $(t_{SWon} + t_{SWoff})$ is switching time. As it is obvious, faster rise times and fall times result in lower switching loss. And the last important power loss that should be concidered is gate drive loss. Gate capacitance charging and discharging to ground in a MOSFET switch causes this power loss [1]. The gate drive dissipation can be written as [2]:

$$P_G = Q_G \cdot V_{DD} \cdot f_{sw} = C_G \cdot V^2_{DD} \cdot f_{sw}$$

where f_{sw} is switching frequency and Q_G is the total charge accumulated on a gate capacitance C_G. In this design, the switching frequency is rather high, thus, we set the size of the switches into an optimal value in order to gain a lower C_G.

3 Design steps of the proposed switched-capacitor step-down DC–DC converter

A schematic diagram of the proposed switched-capacitor step-down DC–DC converter optimized for the load current of 50 mA is shown in Fig. 1.

The core of the converter is switched-capacitor array. It is used for producing gain of $\frac{1}{2}$ for the converter [8]. The detailed schematic diagram of the switched-capacitor array [14] is shown in Fig. 2(a). It contains a flying capacitor called C_{Fly} and four series MOSFET switches, shown as S_1, S_2, S_3 and S_4. Smaller size and higher mobility are the reasons of choosing NMOS over PMOS in almost all of the switches of switched-capacitor structure. The switching period is divided into two phases of charging and discharging. During the charging phase which is represented in Fig. 2(b), switches S_1 and S_3 are closed and C_{Fly} is charged from the supply voltage. In the second phase, i.e. discharging phase which is shown in Fig. 2(c), switches S_2 and S_4 are closed causing C_{Fly} to be discharged into the load. The optimization steps of the switched-capacitor topology are [5]:

1. Selecting f_{sw} and C_L respectively,
2. Setting the length of all switches in minimum value (i.e. 180 nm),
3. Finding the proper value of C_{Fly} that satisfies the desired output voltage and output current at the same f_{sw}, the rise time and the fall time of the clock,
4. Setting W for all switches as the width of them at the same f_{sw}, C_{Fly}, the rise time and the fall time of the clock. Then vary W for each switch to gain maximum efficiency,
5. Reoptimizing the value of C_{Fly},
6. Finally optimizing W of each switch again.

S_1 is a p-channel MOSFET and the other three switches; S_2, S_3 and S_4 are n-channel MOSFETs. Their dimensions

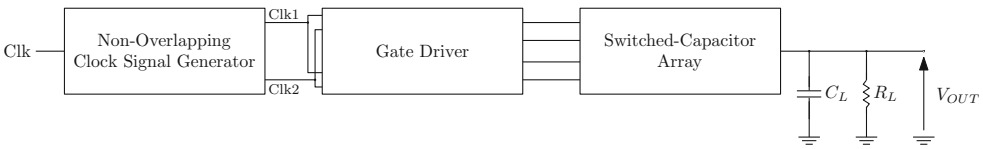


Fig. 1 Schematic diagram of the proposed switched-capacitor step-down DC–DC converter

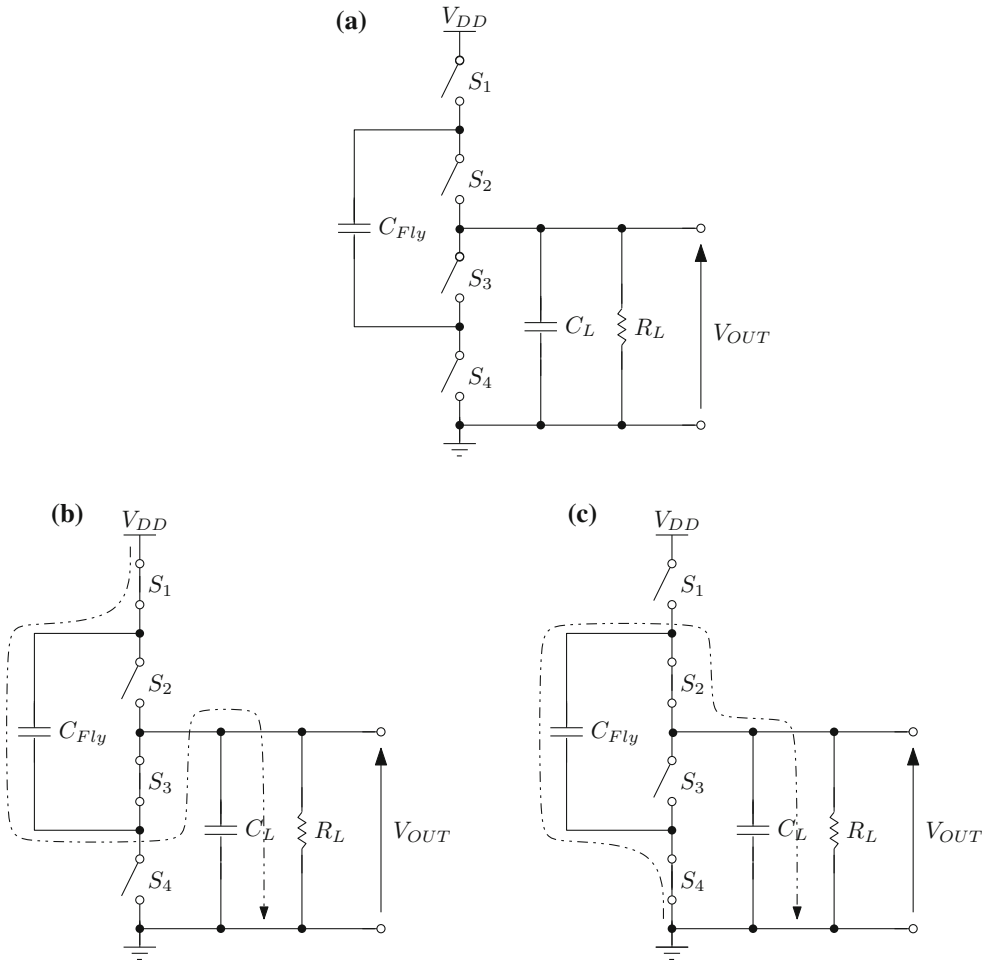


Fig. 2 Detailed schematic diagram of the switched-capacitor array

Table 1 Switch dimensions of switched-capacitor array

$\frac{W_1}{L_1}: \frac{6.43\,\text{mm}}{0.18\,\mu\text{m}}$	$\frac{W_2}{L_2}: \frac{4.1\,\text{mm}}{0.18\,\mu\text{m}}$
$\frac{W_3}{L_3}: \frac{4.1\,\text{mm}}{0.18\,\mu\text{m}}$	$\frac{W_4}{L_4}: \frac{1.37\,\text{mm}}{0.18\,\mu\text{m}}$

are shown in Tabel 1 respectively. These values were extracted from simulations to minimise the power losses.

Large currents need big capacitors. Big capacitors result in bigger chip area and increase the power losses associated with them. With this in mind, the optimum value of 6.13 nF (on-chip) is chosen for the C_{Fly}.

Presense of the load causes voltage ripples at the output of the converter. Voltage ripple is the difference between maximum and minimum output voltage. The output ripples can be reduced by [9]:

- Increasing the load capacitance(C_L) value (the most influential parameter),
- Increasing the switching frequency,
- Increasing the flying capacitance (C_{Fly}) value,
- Reducing the load current,
- Decreasing the R_{ESR} of the capacitors,
- Keeping the clock duty cycle far from 0 and 100 %.

In this design, we Increase the switching frequency into 38 MHz and set the C_L value into 26.2 nF (off-chip) in order to achieve the output ripple of about 21 mV.

Because of wide switching MOSFETs, their gate capacitance is large. Thus, the non-overlapped signals generated directly from the non-overlapping clock signal generator can't drive the large size switching MOSFETs. In

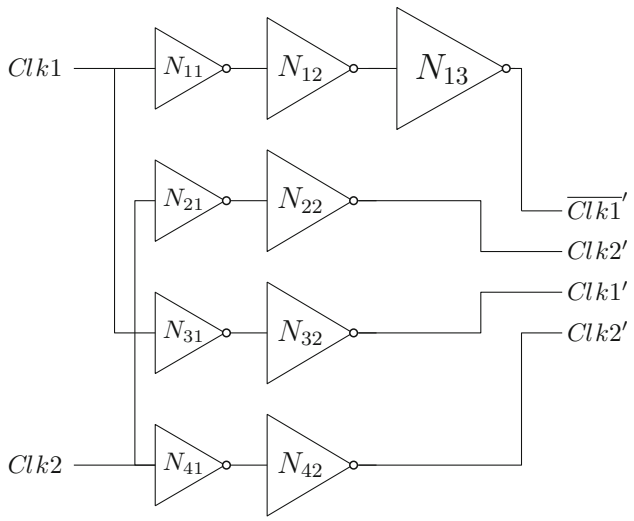


Fig. 3 Schematic diagram of the gate driver stage

order to drive these large capacitive loads, an inverter chain is used between the non-overlapping clock signal generator and the gate of each switching MOSFET. The conventional way in sizing the mentioned inverters is to increase the size of transistors in the inverter chains by a constant factor (for example 2.73). We use another way that results in power saving in the gate driver stage. First, we try to equal the rise time and fall time of the inverters as possible as we can. Second, we set a constant rise time (for example 300 pSec) between the inverters of each branch. Each buffer optimized for a different switching MOSFET. This method decreases the power losses in the gate driver stage without any changes in the output voltage or output current. The total saved power is about 2 mW. The final circuit of the gate driver stage is shown in Fig. 3. The extra inverter in the first buffer is used for driving the PMOS switch.

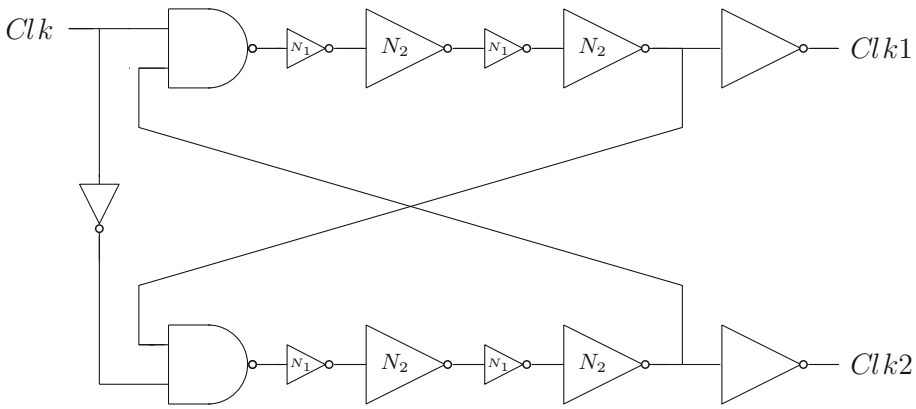


Fig. 4 Schematic diagram of non-overlapping clock signal generator

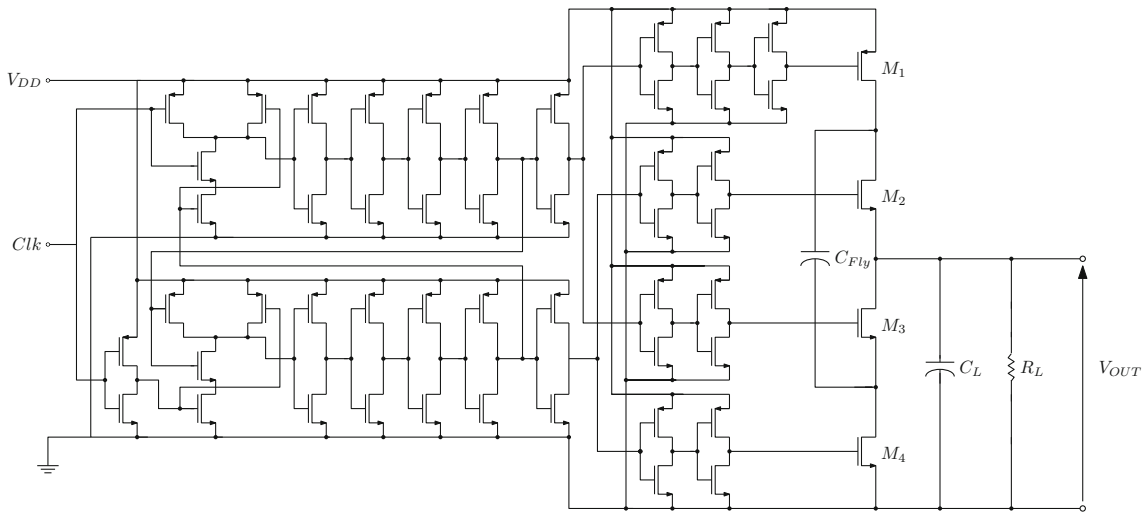


Fig. 5 Final switched-capacitor step-down DC–DC converter

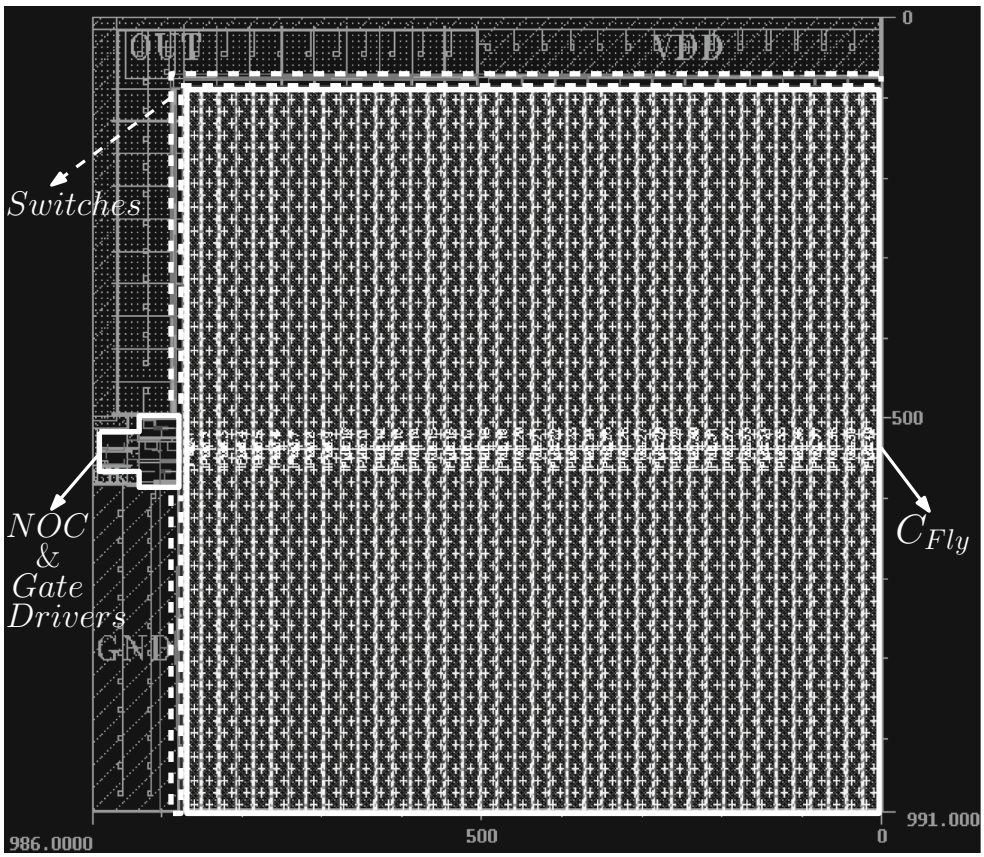
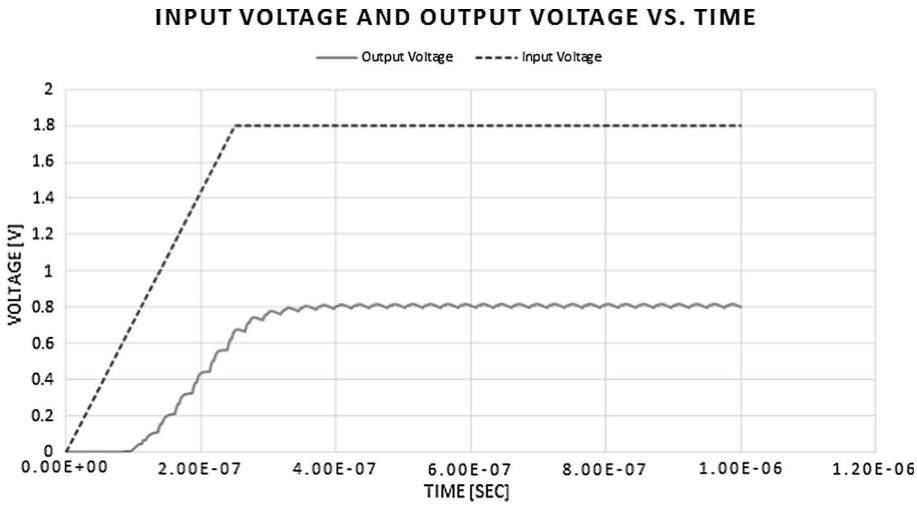


Fig. 6 Layout of the proposed switched-capacitor step-down DC–DC converter

Fig. 7 Time response of the switched-capacitor step-down DC–DC converter



Designing a non-overlapping clock signal generator (NOC) is the last step of our design. If there is no dead time between the two generated clock signals, the switching MOSFETs may be turned on at the same time leading to a large current flowing from the power supply to the ground, thus decreasing the power efficiency will be the result. So, presence of a non-overlapping clock signal generator is necessary. A dead time generator circuit is shown in Fig. 4.

As it's seen, the main clock goes through the non-overlapping clock signal generator and two branches of non-overlapped signal called *Clk*1 and *Clk*2 appear at the two output ports with 180 °C difference. The minimum

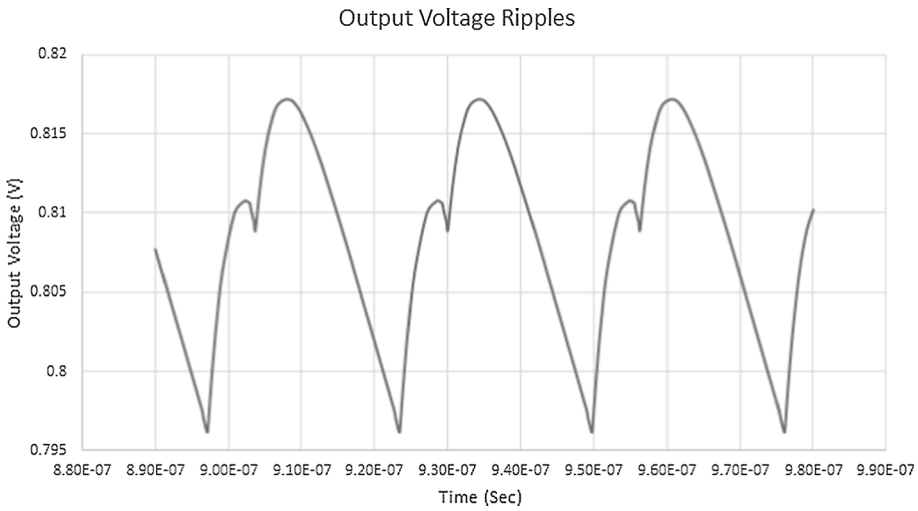


Fig. 8 The switched-capacitor step-down DC–DC converter output voltage ripples

Fig. 9 The relation between efficiency and R_L

value of dead time between the two clocks is set to 500 pSec in order to eliminate possible short circuit currents. This value was achieved by simulations and was a optimal value for the power efficiency point of view. There is also alternative transistor sizes used for the delay part [13]. When smaller size transistors charge the gate capacitance of larger size transistors, the generated RC delay causes the needed time delay in non-overlapping clock signal generator. The overall switched-capacitor step-down DC–DC converter cicuitiry is presented in Fig. 5.

4 Simulation results

The proposed switched-capacitor step-down DC–DC converter is supplied with 1.8 V and loaded with a 16 Ω resistor (R_L) which is paralleled with a 26.2 nF off-chip capacitor (C_L). The produced average output voltage is about 0.8 V and the average output current is about 50 mA. Practically, the output voltage of the switched-capacitor DC–DC converter is not exactly half of its input voltage. This is because of the both switch and capacitors' parasitics [7]. So, for the load current of about 50 mA, only an average output voltage of 0.8 V attained instead of exactly half of 1.8 V supply voltage (i.e. 0.9 V). The layout of the proposed switched-capacitor DC–DC converter is shown in Fig. 6. As it's clear, the distance between the switches and C_{Fly} is set to minimum value in order to gain maximum

Table 2 Comparison with recently published switched-capacitor converters

Design	[2]	[6]	[12]	[3]	[4]	This work
Technology (μm)	0.13	0.045	0.35	0.5	0.35	0.18
Active Area (mm^2)	0.1239	1.3	7.8	10	–	1
Switching Frequency (MHz)	1	60	0.2–1	0.01–1	1–30	35-40
Input Voltage (V)	1.9	3.2–4.2	2.5	2.8	5	1.8
Output Voltage (V)	0.926	0.9–1	0.9–1.5	0.4-2	3.2–3.35	0.8
Power Efficiency (%)	91	71.4 (max)	66.7 (max)	78 (max)	72 (max)	≥ 80
C_{Fly} (nF)	1000 (off-chip)	1.12	6.72 (on-chip)	–	60	6.13 (on-chip)
C_{Load} (nF)	200 (off-chip)	0.19	470 (off-chip)	–	20	26.2 (off-chip)
Load Current (mA)	61.7	16 (max)	5 (max)	0.1 (max)	70 (max)	50
Output Ripple (mV)	22	24	–	–	≤ 37.5	21

efficiency. Figure 7 shows the simulated transient response of the converter. Output voltage ripples is shown in Fig. 8. The peak-to-peak value of the ripples for the mentioned load capacitance is about 21 mV. Increasing the switching frequency and load capacitance value reduced peak-to-peak value of the ripples. The relation between efficiency and R_L is shown in Fig. 9.

Finally, Table 2 presents a comparison between some recent works done at this region of science.

5 Conclusions

Proposed 1.8–0.8 V switched-capacitor step-down DC–DC converter was designed in 180 nm Standard CMOS technology. It delivered about 50 mA load current and achieved the power efficiency of more than 80 %. Improving the power efficiency meantime simply of the converter was the main goal of this design. So, all of the components have been optimized with respect to this matter. During the design, a power saving method proposed on the gate driver circuits. It reduced about 2 mW of total dissipated power and resulted in a higher power efficiency. The converter occupies an area of about 1 mm^2. The maximum peak-to-peak value of output voltage ripple was about 21 mV.

Acknowledgments The authors would like to thank Mr. Saeed Ghiasi, Mrs. Jafarnejad and Mrs. Sheikholeslami for their helpful supports and feedbacks.

References

1. Balogh, L. (2001). *Design and application guide for high speed mosfet gate drive circuits*. Texas Instruments/Unitrode Corporation, Power Supply Design Seminar, SEM.
2. Bochenek, M. (2012). *Development of radiation resistant cmos integrated circuits for the power distribution system un the upgraded atlas semiconductor tracker*. Ph.D. Thesis, AGH University of Science and Technology.
3. Castro, P., Silveira, F., Eirea, G. (2012). Modular architecture for ultra low power switched-capacitor dc–dc converters. In *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)* (pp. 1036–1039).
4. Choi, Y., Jeon, H., Kim, Y.B. (2013). A switched-capacitor dc-dc converter using delta-sigma digital pulse frequency modulation control method. In *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)* (pp. 356–359).
5. Forestiere, G. (2014). *Ultra-low power circuits for power management*. Master's thesis, KTH Information and Communication Technology, Stockholm, Sweden.
6. Haq, F.U. (2011). *Low power switched capacitor dc-dc converters for low power transceiver applications*. Master's thesis, Tampere University of Technology.
7. Jung, I.S., Kim, Y.B., Choi, M. (2011). The novel switched-capacitor dc-dc converter for fast response time and reduced ripple. In *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)* (pp. 1–4).
8. Ma, M. (2003). *Design of high efficiency step-down switched capacitor dc/dc converter*. Master's thesis, Oregon State University.
9. Ngo, K., Webster, R. (1992). Steady-state analysis and design of a switched-capacitor dc–dc converter. In *23rd Annual IEEE Power Electronics Specialists Conference, 1992. PESC'92 Record* (pp. 378–385).
10. Qian, J., & Zhao, L. (2006). *Circuit design and power loss analysis of a synchronous switching charger with integerated mosfets for li-ion batteries*. Technical Report, Texas Instruments.
11. Sclocchi, M. *Switching power supply design: Discontinuous mode flyback converter.* Technical Report, National Semiconductor.
12. Su, L., Ma, D., & Brokaw, A. P. (2010). Design and analysis of monolithic step-down sc power converter with subthreshold dpwm control for self-powered wireless sensors. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *57*(1), 280–290.
13. Wang, L. (2013). Design of integrated voltage-mode controlled dc–dc buck converter.
14. Xu, M., Sun, J., Lee, F.C. (2006). Voltage divider and its application in the two-stage power architecture. In *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC'06.* (p. 7).

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