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MIXED SIGNAL LETTER

SAR ADC architecture with 98.8 % reduction in switching energy over conventional scheme

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Abstract A novel power saving switching scheme for successive approximation register analogue-to-digital converter is proposed in this letter. Adopting the top-plated sampling technology and dummy-capacitor-aided switching technology, the number of capacitors can be reduced by 75 % compared with the conventional scheme. Employing the one-side switching instead technology and higher-bit switching instead technology, the average switching energy can be reduced to 1.2 % compared with the conventional scheme. Employed the proposed switching scheme, a 10-bit 20-kS/s 0.6-V SAR ADC is designed in 0.18-μm CMOS technology. Post-layout simulation results indicate that a SNDR of 60.3 dB can be achieved with the Nyquist input at 20 kS/s. And the figure-of-merit of the proposed ADC is 1.04 fJ/conversion-step.

Keywords SAR · ADC · Dummy-capacitor-aided switching · One-side switching instead · Higher-bit switching instead

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1 Introduction

Due to the advantages of its simple structure, least usage of analog circuit, and energy-efficiency, successive approximation register analogue-to-digital converter (SAR ADC) has been the optimal choice in many special fields nowadays. Of all the components included in SAR ADC, capacitor array contributes a significant part of total power consumption. The switching scheme and the total capacitance of capacitor array are two major factors influencing the power the capacitor array consumed.

With regard to the switching scheme, great efforts have been made to improve it. Compared to the conventional scheme, the set-and-down scheme of [1] and Vcm-based scheme of [2] realize a reduction of 81.2 and 87.5 % separately in switching power. The MCS scheme of [3], tri-level scheme of [4] and Vcm-based monotonic scheme of [5] can reach a reduction of 93.7, 96.9 and 97.7 %, separately. With the scheme proposed in this letter, the power efficiency can be improved further.

2 Principle of energy saving for the capacitor array

2.1 Principle of energy saving during switch transitions

The proposed switching scheme adopts the differential architecture to decrease the impact of common-mode noise and suppress even-order distortion. To realize the one-LSB transition, it changes the voltage, across the dummy capacitor on only one side, by half of the reference voltage. This is named as dummy-capacitor-aided switching (DCAS) technology. Together with the top-plated sampling

technology, the number of capacitors would be cut down by 75 % compared with that of the conventional scheme. That is, the capacitor array for (N−2)-bit resolution with the conventional scheme could realize N-bit resolution with the proposed scheme.

The OSSI technology can be appreciated from Fig. 1. The conventional switching method shown in Fig. 1(a) and the proposed switching method shown in Fig. 1(b) contribute the same effect on the voltage change on common top-plates of capacitors obviously. Nevertheless, since the charge stored on the common top-plates of capacitors satisfies charge conservation law when comparisons are ongoing, the voltage sources just need to charge the bottom-plates of capacitors. Therefore, the energy required can be formulated as:

$$\begin{aligned} E_{change} &= \int_{t1}^{t2} i_{source} V_{source} dt = V_{source} \int_{t1}^{t2} i_{source} dt \\ &= V_{source} Q_{t1 \to t2} \\ &= V_{source}(Q_{t1 \to t2}) = V_{source} \Delta Q = V_{source} C \Delta V \end{aligned} \quad (1)$$

According to (1), the energy consumed in Fig. 1(b) proves to be zero. On condition that the bottom plates of capacitors are initially loaded with the sequence [V_{cm},0,…,0] in sampling periods (V_{cm} represents the common-mode voltage, half of the reference voltage V_{ref}), use of the top-plated sampling technology and OSSI technology could enable the switching energy consumed during the first two comparisons to be zeros.

The HBSI technology is illustrated in Fig. 2. Switching any bit from 0 to Vref and switching the higher bit from 0 to Vcm have the identical effect on the voltage change on common top-plates of the capacitors. However, as Fig. 2(a, b) shown, switching the higher bit instead turns out to be more efficient.

Adopting the OSSI technology and HBSI technology, the proposed switching scheme for a 4-bit SAR ADC is depicted as Fig. 3 shown. When the initial states of the bottom plates are set to be [Vcm,0,…,0], the energy consumed during the third comparison would be zero particularly. That is, the energy consumed in the first three comparison cycles would all be zeros. Since the bulk of switching energy is consumed in the first few comparison cycles, the proposed switching scheme proves to be more energy-efficient than any other existing schemes. As for the following comparison cycles, the HBSI technology would continue to play the role of saving energy.

The average switching energy for an N-bit SAR ADC with this proposed switching scheme can be fit by the following formula.

$$E_{aver} = \sum_{i=1}^{N} (2^{N-i-4}) C V_{ref}^2 \quad (2)$$

On the condition of the same unit capacitor Cu, behavior simulation for 10-bit differential SAR ADC is performed to compare the switching energy between the proposed switching scheme and the other existing schemes. As Fig. 4 shown, the proposed switching scheme proves to be optimal.

Some specific indicators are listed in Table 1. The average switching energy with the latest published scheme, the V_{cm}-based monotonic scheme, is $31.9CV_{ref}^2$, whereas with the proposed scheme, it is only $15.8CV_{ref}^2$. So a reduction of 98.8 % in the switching energy is realized with respect to the conventional scheme.

2.2 Principle of optimization for the total capacitance

The capacitor array for N-bit SAR ADC with this proposed scheme is shown in Fig. 5. Cu represents the unit capacitor, C_0 (namely the dummy capacitor) is equal to Cu, and C_i to $2^{i-1} \times$Cu, where i = [1,2,…,(N−2)]. The number of

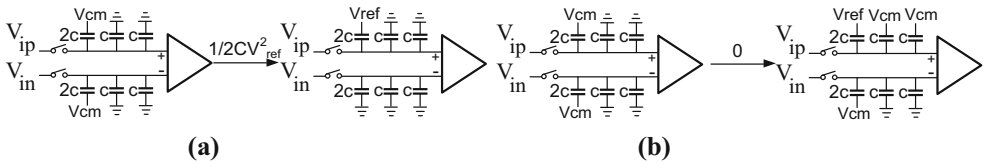


Fig. 1 Illustration of the OSSI technology

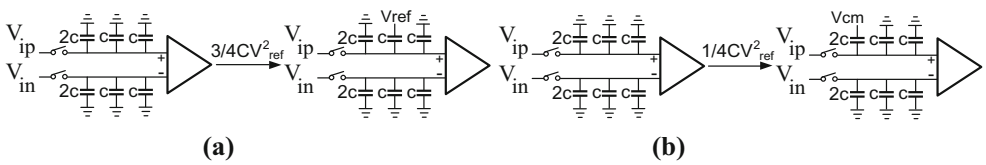


Fig. 2 Illustration of the HBSI technology

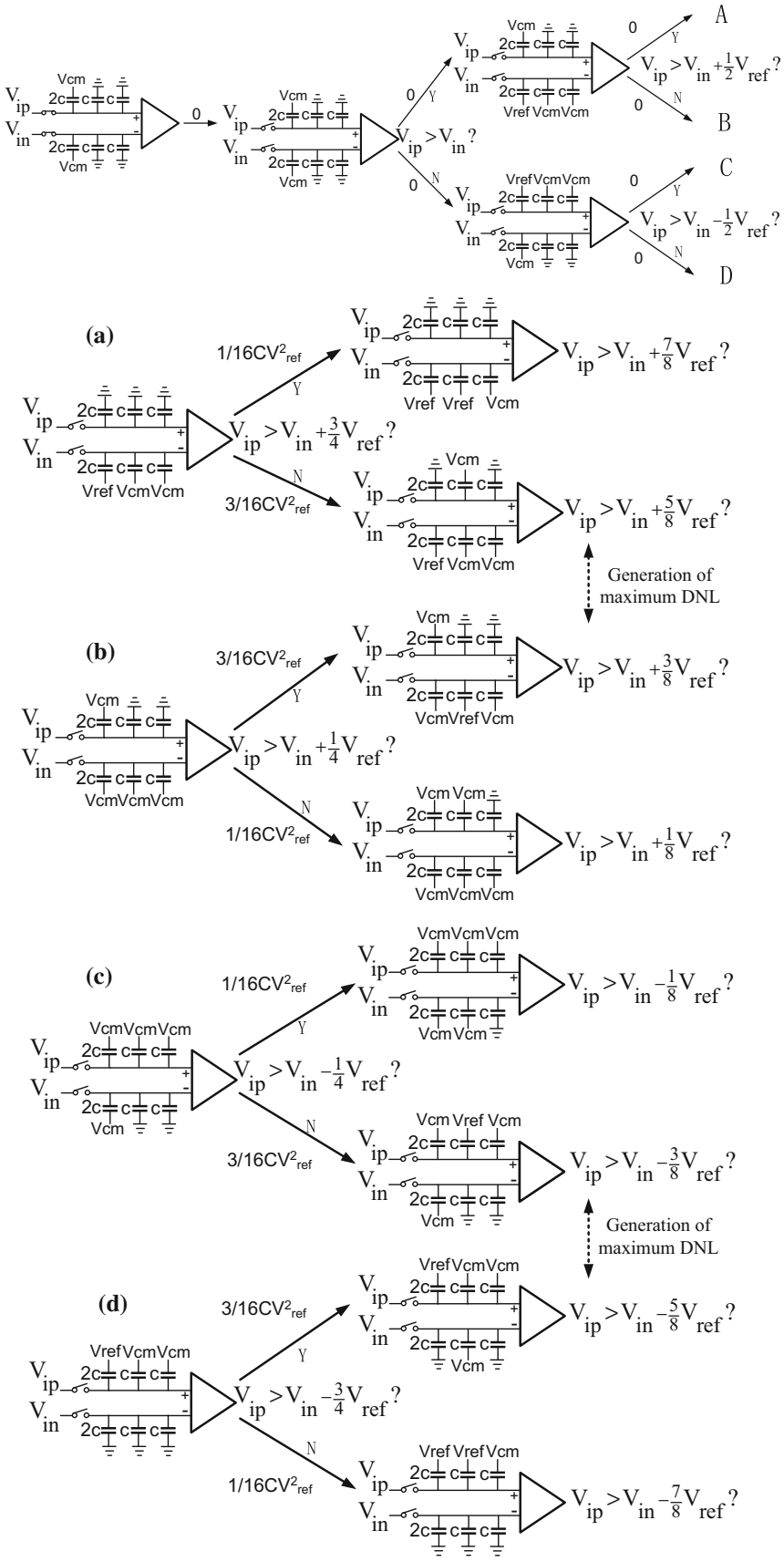


Fig. 3 Illustration of the proposed switching scheme for a 4-bit SAR ADC

capacitors in the capacitor array, on either the positive side or negative side, would be 2^{N-2}. It is a quarter of that with the conventional scheme. Therefore, both chip area and power efficiency can be improved significantly.

For 4-bit resolution shown in Fig. 3, the worst case differential nonlinearity (DNL) would occur during the transition between 1/4 and 3/8 FS, or between 3/4 and 7/8 FS. By this analogy, the similar conclusion would be drawn for the N-bit resolution case. At that time, apart from C_0, all the capacitors, that is, $2 \times (2^{N-2}-1)$ Cu-elements totally, are switched. The capacitance value of Cu follows the normal distribution:

$$\sigma\left(\frac{\Delta C_u}{C_u}\right) = \frac{K_\sigma}{\sqrt{WL}} \quad \text{and} \quad C_u = K_c \cdot WL \tag{3}$$

where Kσ depends on the manufacturing process and capacitor type. Kc is the capacitor density parameter. W and L represent the width and length of the unit capacitor. The standard deviation σ(Cu) can be deduced as:

$$\sigma(C_u) = \frac{C_u}{\sqrt{2}} \cdot \sigma\left(\frac{\Delta C_u}{C_u}\right) = \frac{C_u}{\sqrt{2}} \cdot \frac{K_\sigma}{\sqrt{WL}} \tag{4}$$

If n unit capacitors are connected in parallel, the standard deviation can be obtained in terms of summing n independent random variables.

$$\sigma^2(nC_u) = n \cdot \sigma^2(C_u) \tag{5}$$

So the standard deviation of C_i could be expressed as below:

$$\sigma^2(C_0) = \sigma^2(C_u), \sigma^2(C_i) = \sigma^2(2^{i-1}C_u) = 2^{i-1}\sigma^2(C_u), \quad i = [1, 2, \ldots, (N-2)] \tag{6}$$

In addition, the mismatch of any capacitor is irrelevant to that of the others. If the mismatch property is taken into consideration, the variance of the maximum DNL for the proposed scheme can be depicted as below:

$$\sigma_{DNL,MAX} = \frac{\sqrt{2 \times (2^{N-2}-1)} \times \sigma(C_u)}{C_u} \tag{7}$$

Formula (7) indicates that σ(Cu) with this proposed scheme is by factor $\sqrt{2}$ smaller than that with the conventional scheme. According to (3) and (4), both the area and capacitance of Cu are reduced by half.

To verify the correctness of the above derivation, a behavioral simulation is made and the simulation results are shown in Fig. 6. Figure 6(a) corresponds to the conventional switching scheme, while Fig. 6(b) to the proposed switching scheme. With the conventional switching scheme, the standard deviations of maximum DNL is 0.317LSB, and the standard deviations of maximum INL is 0.446LSB. By contrast, 0.221 and 0.311LSB can be achieved with the proposed switching scheme, respectively. The root-mean-square (RMS) DNL and RMS INL for each digital code are also simulated and shown in Fig. 6. Obviously, with the proposed switching scheme, the maximum RMS DNL and the maximum RMS INL are also improved.

Need of special note is that the proposed switching scheme not only requires an additional Vcm generator, but also leads to comparator common mode variation. Assuming the power consumed by the Vcm generator to be constant, the overall power efficiency could be improved for high-resolution case because the power consumed by the capacitor array increases in an exponential manner,

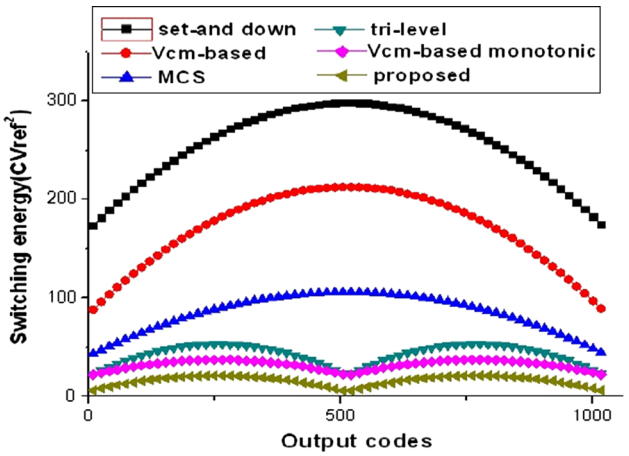


Fig. 4 Switching energy comparison for 10-bit SAR during transitions

Table 1 Comparison of different switching schemes for 10-bit SAR

Switching scheme	Average switching energy (CV^2_{ref})	Energy saving	Area saving
Conventional	1363.33	Reference	Reference
Set-and-down [1]	255.5	81.2 %	50 %
Vcm-based [2]	170.2	87.5 %	50 %
MCS [3]	85.1	93.7 %	75 %
Tri-level [4]	42.4	96.9 %	75 %
Vcm-based monotonic [5]	31.9	97.7 %	75 %
Proposed	15.8	98.8 %	75 %

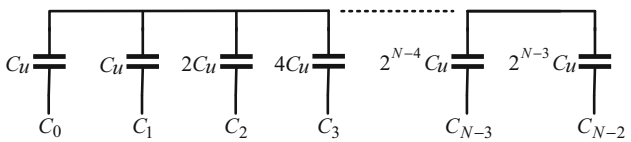


Fig. 5 Capacitor array for N-bit SAR with the proposed scheme

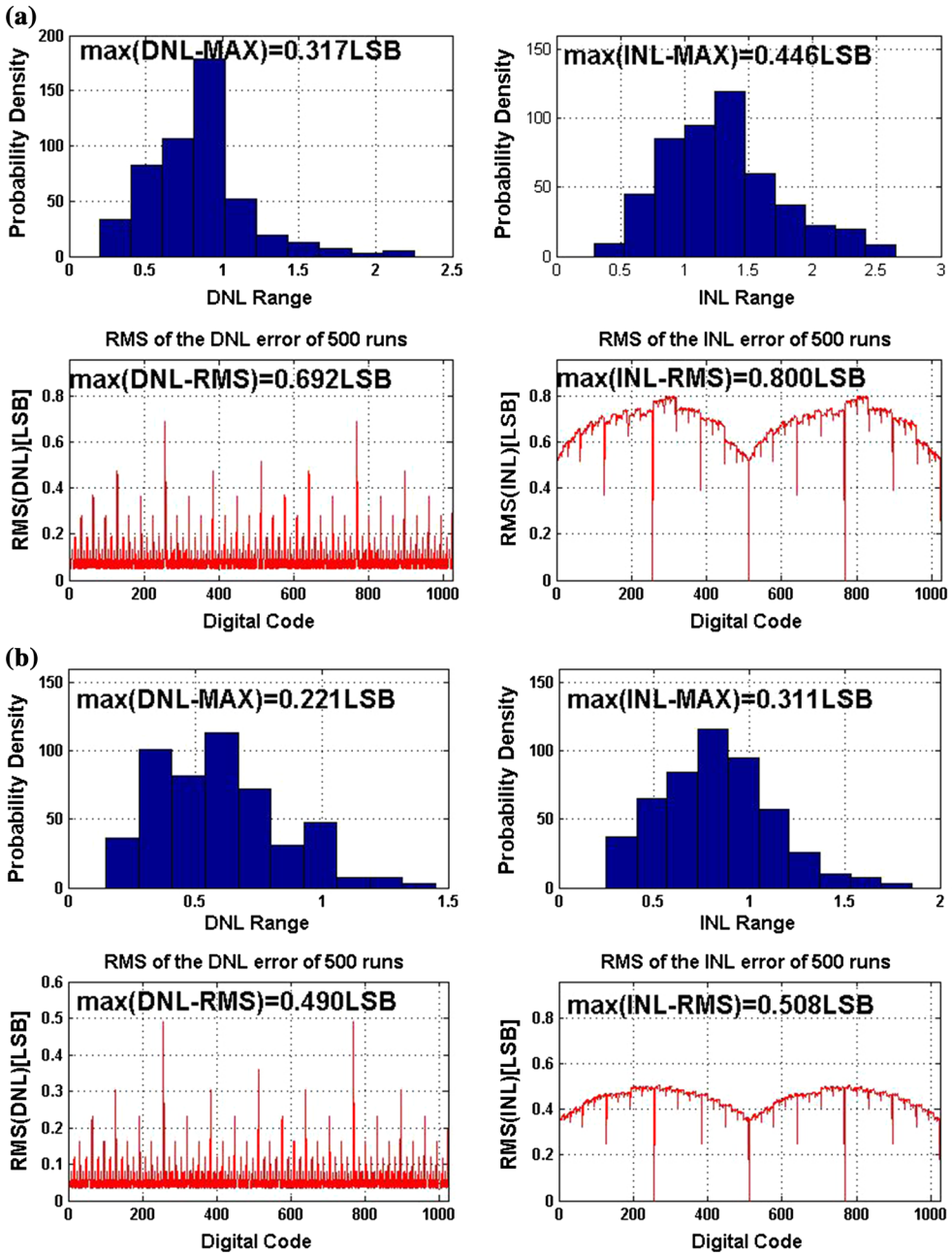


Fig. 6 Comparison of static performance for 10-bit SAR ADC. **a** Simulation result with the conventional switching scheme. **b** Simulation result with the proposed switching scheme

which is depicted in formula (2). The comparator common mode variation can introduce harmonics on account of the voltage-relevant nonlinear of the input parasitic capacitance of the comparator. This can be dealt with by some special handling. For example, simply an additional capacitor connecting between the common top-plates and ground is added to suppress the voltage-relevant nonlinear of the comparator input parasitic capacitance, at the expense of introducing gain error more or less. The comparator common mode variation also makes the dynamic offset change. On one hand, the variation of the dynamic offset can be reduced by increasing the transconductance of input transistors. On the other hand, offset cancelling technology can be adopted to reduce the variation effectively.

3 Simulation results

A 20kS/s 10-bit 0.6 V SAR ADC employed the proposed switching scheme is implemented in 0.18-μm CMOS technology. The designed layout, which occupies an area of 380 × 430 μm^2, is shown in Fig. 7.

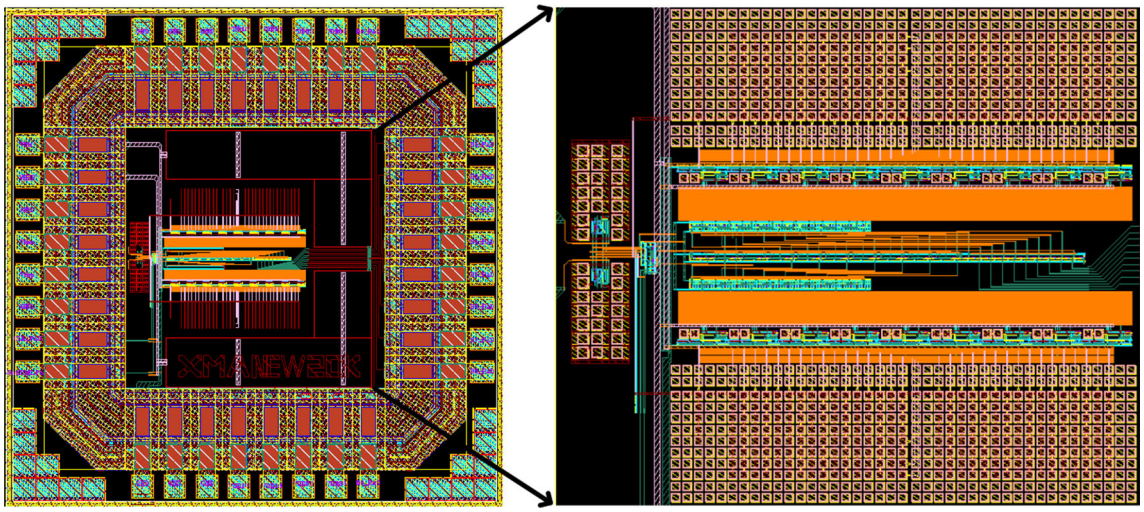


Fig. 7 Layout of the proposed SAR ADC

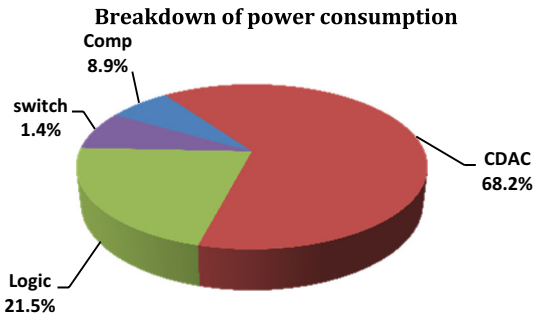


Fig. 8 Breakdown of simulated power consumption for each block

Capacitance of the unit capacitor in this work is designed to 18fF. At the sampling rate of 20kS/s, the proposed SAR ADC consumes 17.6nW from a 0.6-V supply voltage. Based on the post-layout simulation, the breakdown of simulated power consumption for each block is shown in Fig. 8. The capacitive DAC and the control logic consume 68.2 and 21.5 % of the total power, respectively.

The DNL and integral nonlinearity (INL) of the proposed SAR are shown in Fig. 9. It can be seen that the maximum DNL is −0.38/0.2LSB, while the maximum INL is −0.37/0.2LSB.

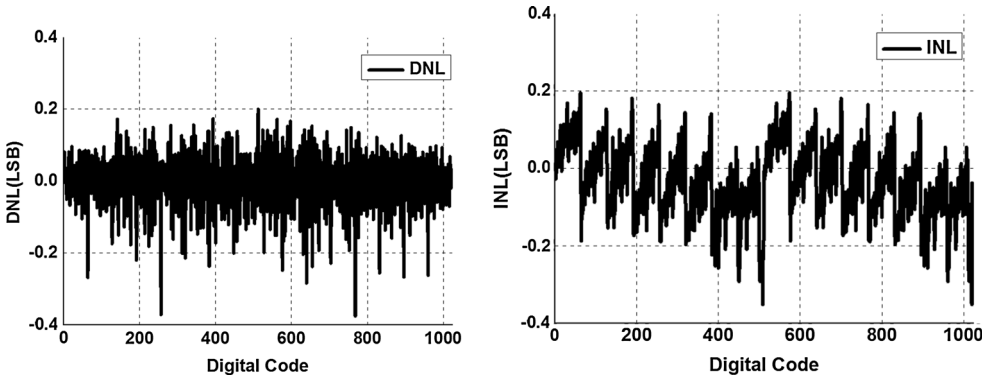
An 8,192-point fast Fourier transform (FFT) of the 20kS/s SAR ADC at near–Nyquist operation is shown in Fig. 10. On condition of the amplitude of the input signal is set to −0.5dBFS, the signal-to-noise and distortion ratio (SNDR) and the spurious free dynamic range (SFDR) can reach 60.3 and 69.6 dB, respectively.

Figure 11 exhibits the dynamic performance as the input frequency is swept at 20kS/s. The ADC achieves a peak SNDR of 61.1 dB.

The Effective Number of Bits (ENOB) of the proposed SAR ADC is 9.73 bits. To estimate power efficiency of ADCs working with different sampling rates and resolutions, the figure-of-merit (FOM) is essential. It is defined as below.

$$\text{FOM} = \frac{\text{Power}}{\min\{2 \times \text{ERBW}, f_s\} \times 2^{\text{ENOB}}} \tag{8}$$

Fig. 9 Simulated DNL and INL



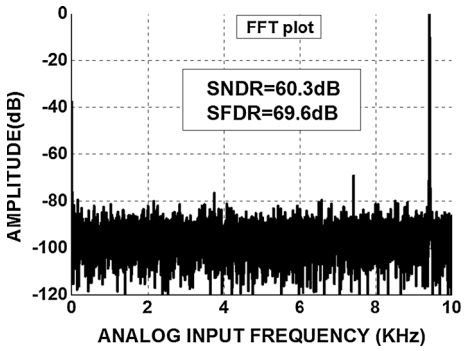


Fig. 10 8,192-point FFT spectrum at 20kS/s with Nyquist input

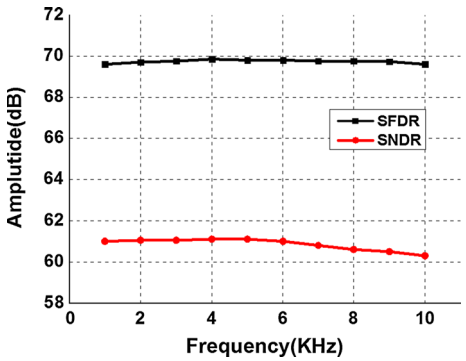


Fig. 11 Dynamic performance of the SAR ADC versus the input frequency

Table 2 Performance summary and comparison

	JSSC' 12[a] [6]	VLSI' 14[a] [7]	JSSC' 14[a] [8]	ISSCC' 14[a] [9]	This work[b]
Technology (nm)	130	90	180	180	180
Resolution (bit)	10	10	10	10	10
Supply (V)	1/0.4	0.4	0.6	0.6	0.6
Sampling rate (kS/s)	1	250	100	16	20
Power (nW)	53	200	390	47	17.6
DNL/INL(LSB)	0.61/0.46	0.43/0.67	0.50/0.89	0.1/0.2	0.38/0.37
ENOB (bits)	9.1	8.63	9.2	9.73	9.73
FOM (fJ/con.-step)	94.5	2.02	6.7	3.5	1.04

[a] Measured results

[b] Simulation results

where ERBW represents the effective resolution bandwidth of the converter. Since only 17.6 nW is consumed under the 0.6-V supply voltage, according to (8), the FOM of the proposed ADC is 1.04 fJ/conversion-step.

Table 2 summaries the simulated performance of the proposed ADC, and compares it with the current state-of-the-art ADCs.

4 Conclusion

A high energy-efficiency strategy on the capacitor array for SAR ADC is proposed. Compared with other existing schemes published so far, the proposed scheme proves to be optimal in both energy saving and chip area saving. Employed the proposed switching scheme, a 10-bit 20-kS/s 0.6-V SAR ADC is designed in 0.18-μm CMOS technology. It occupies a chip area of 380 × 430 μm^2. Post-layout simulation results indicate that, on premise of the 20kS/s sampling rate, the proposed SAR ADC consumes only 17.6 nW, and achieves a SNDR of 60.3 dB with the Nyquist input. Consequently, the FOM is 1.04fJ/conversion-step.

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References

1. Liu, C. C., Chang, S. J., Huang, G. Y., & Lin, Y. Z. (2012). A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. *IEEE Journal of Solid-State Circuits, 45*(4), 731–740.
2. Zhu, Y., Chan, C. H., Chio, U. F., Sin, S. W., Seng-Pan, U., Martins, R. P., & Maloberti, F. (2010). A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS". *IEEE Journal of Solid-State Circuits, 45*(6), 1111–1121.
3. Hariprasath, V., Guerber, J., Lee, S.-H., & Moon, U.-K. (2010). Merged capacitor switching based SAR ADC with highest switching energy-efficiency. *Electronics Letters, 46*, 620–621.
4. Yuan, C., & Lam, Y. (2012). Low-energy and area-efficient tri-level switching scheme for SAR ADC. *Electronics Letters, 48*, 482–483.
5. Zhangming, Zhu, Xiao, Yu., & Xiaoli, Song. (2013). Vcm-based monotonic capacitor switching scheme for SAR ADC. *Electronics Letters, 49*, 327–329.
6. Zhang, Dai, Bhide, Ameya, & Alvandpour, Atila. (2012). A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-μm CMOS for Medical Implant Devices. *IEEE Journal of Solid-State Circuits, 47*(7), 1585–1593.
7. Yan-Jiun Chen, et al.. (2014), A 0.4 V 2.02fJ/conversion-step 10-bit hybrid SAR ADC with time-domain quantizer in 90 nm CMOS, *Symp. VLSIC*, 1–2.
8. Jin, Jiayi, et al. (2014). An Energy-Efficient Time-Domain Asynchronous 2b/Step SAR ADC With a Hybrid R-2R/C-3C DAC Structure. *IEEE Journal of Solid-State Circuits, 49*(6), 1383–1396.
9. Frank M. Yaul, et al.. (2014), A 10b 0.6nW SAR ADC with Data-Dependent Energy Savings Using LSB-First Successive Approximation, *IEEE ISSCC Digest of Technical Papers*, 198–199.

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