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A new SPICE macro model of single electron transistor for efficient simulation of single-electronics circuits

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Abstract To explore single-electron circuits for different applications, a proper simulation platform where circuits consisting of single electron transistors and other devices can be simulated efficiently is needed. A macro model of single electron transistor featuring symmetric tunnel junctions is proposed. In the proposed model, a voltage controlled current source is incorporated in the existing model of SET to get more accurate results. Three scaling factors have been included in the model to improve the versatility of the model. The advantages and disadvantages of different simulation methods are discussed as a justification for choosing the macro model approach. The proposed model can efficiently describe the physical phenomena occurring in coulomb blockade and coulomb oscillation regions. The SPICE environment is used for the simulation and to verify the accuracy, the model is applied to a single electron inverter circuit and the effect of macro model parameters on the noise margin is investigated to estimate the robustness of the inverter cell. A multi peak negative differential resistance circuit based on the proposed macro model is designed and demonstrated. Also, an integrator circuit has been designed to prove the validity of the proposed model in the analog domain. Further, the linearity of the integrator circuit is analyzed through harmonic and intermodulation distortion analysis.

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1 Introduction

Single electronics is nothing but the controlled manipulation of individual electrons through a barrier. Though the journey of single electronics started long ego by Robert Millikan who manipulated single electron onto oil drops in the early 1920s, it took almost 70 years to put its footprint in the solid state technology. Single electron transistor (SET) is the most promising candidate for future VLSI/ULSI solutions [1–4]. Several works have been reported in the literature on SET based circuit designs [5–10]. Some works have also been reported on hybrid SET–MOS circuit design [11–18]. To design and analyze single-electron circuits efficiently, we need a proper simulation environment, which will allow us to study the characteristics and have potential to compete with other existing technologies. As Monte Carlo based simulators take significant time to simulate circuits and don't support the hybrid SET–MOS simulations, researcher have been looking for other modeling approaches [19–24] to efficiently simulate single-electron based circuits. Basically there are three different approaches to the simulation of single electronics circuits: SPICE macro-modeling, Monte Carlo based method and master equation method. The Monte-Carlo method is a probabilistic approach where the result is achieved by stochastic integration [25]. In this method, random tunnel times are computed for all possible events and correlation in these Pseudo random numbers can affect the result drastically [26]. As this method includes stochastic sampling, it takes a long

time to simulate circuit with large no. of nodes. In master equation method, a set of equations which represents the charge transport process in single-electron circuits are solved deterministically to get the simulation results [27]. In this approach one needs to know all relevant states a circuit can occupy which is a tedious job to perform. A macro model is an equivalent circuit of a device designed using conventional microelectronic components such as voltage and current sources, diodes and resistors [28]. In macro modeling, we are not concerned about the probability of tunneling events; rather the focus is on the KCL and KVL equations. So in macro modeling approach, the computation time is lesser compared to the other methods. For small circuits, master equation method is faster than the Monte Carlo approach, but for larger circuits, master equation method becomes infeasible. For very large system, SPICE macro modeling is much faster compared to other approaches.

Several macro models of SETs have been reported in the literature [18–20] which are efficient to be used as a basic circuit element in a single-electron circuit. Yu et al. first proposed a macro model of a single electron transistor for efficient circuit simulation in SPICE [18]. Wu et al. later modified it by incorporating two back to back diodes in the model to make the current flowing from gate to source negligibly small [19]. Karimian et al. further modified it to calculate the timing of electron tunneling through the barrier by employing a switch capacitor circuit in the model which works as a quantizer circuit [20]. In this paper we have improved Yu's model by incorporating a voltage controlled current source to get more accurate results. In Yu's model [18], shown in Fig. 1 the current in the coulomb blockade region is not zero for V_{gs} equal to 0 V, rather it increases linearly. In case of Wu and Lin's model [19], the current in the coulomb blockade region is zero for a fixed value of the gate to source voltage, but it doesn't provide any plots regarding the value of current for other values of gate to source voltage. Yu's model is unable to predict the characteristics in the coulomb blockade region whereas Wu and Lin's model doesn't provide any clear picture of the coulomb blockade characteristics. We have improved Yu's model by replacing R_1 with a voltage controlled current source g_1.

In SPICE simulation, it is assumed that only the terminal characteristics of one device can affect the characteristics of other devices [18]. For circuits consisting of Single electron transistors this assumption may not be valid as the current in a single-electron circuit is calculated considering the charge states of all the coulomb islands together. If we consider the interconnection between adjacent SETs to be very large so that it acts as a reservoir for the adjacent SET, then single-electron circuits can be simulated in SPICE type simulator, but obviously with a bit of sacrifice in accuracy. Therefore, if the interconnection is large enough, SET shows similar characteristics irrespective of whether it is a part of a circuit or an isolated one. It has been observed that SET works well in a circuit if $C_L > 6.25\ C_j$ where C_L and C_j are the values of the load capacitance and typical junction capacitance respectively [18].

2 The macro model

The proposed macro model of SET is shown in Fig. 2 and its code is given in Fig. 3. Here CF1, CI2, CR1, CR2, CR3, CR4, and CVp are macro model parameters, K_1, K_2 and K_3 are the scaling factors. The symmetric features of the characteristics on both side of the coulomb blockade are captured using a combination of resistor, diode and voltage source, denoted by R_1, D_1, V_1 and R_2, D_2, V_2 respectively. The function of R1, D1, V1 and R2, D2, V2 is to control the current in positive and negative direction respectively assuring the flow of current in both directions when the value of V_{ds} is larger than the critical voltage [27] of the device. If the value of the critical voltage is greater than V1 then diode D1 is ON and current flows through the resistor R1 and if it is less than V2 then the diode D2 is ON and current flows through the resistor R2. For coulomb blockade the current contribution comes from the voltage controlled current source g_1.The resistor RG is used in the

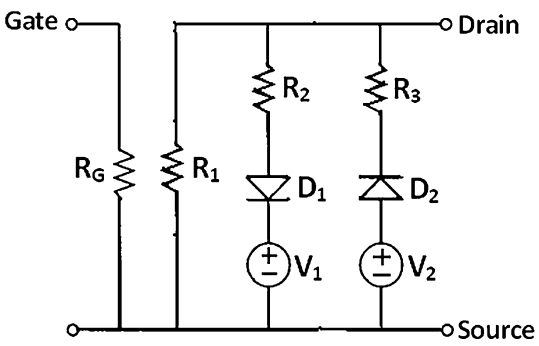

Fig. 1 The macro model of Yu et al.

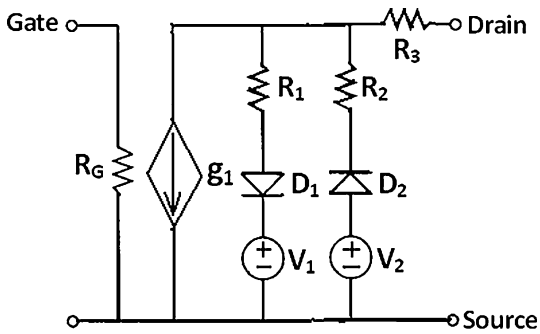

Fig. 2 The proposed macro model, where R_1 of Yu's model is replaced by a voltage controlled current source g_1

```
*D=Drain
*G=Gate
*S=Source

.option
.macro SET D G S
.param
+pi=3.14
+CF1=40
+CI2=0.2e-9
+CR1=300e+6
+CR2=220e+6
+CR3=0.5e-9
+CR4=0.5e-9
+CVp=0.02
V2 5 S DC 0.02
V3 7 S DC -0.02
RG G S 100G
RR1 1 4 R='(CVp/ (CI2-2*CVp/ (2*CR1+CR2*cos (CF1*pi*V (G, GND)))))/K1'
RR2 1 6 R='(CVp/ (CI2-2*CVp/ (2*CR1+CR2*cos (CF1*pi*V (G, GND)))))/K2'
RR3 1 D 1
D1 4 5 DIODE
D2 7 6 DIODE
g1 1 S cur='(CR3*sin (pi*V (G, GND)))/K3'
.MODEL DIODE D (N=0.01)
.eom
```

Fig. 3 SPICE macro model code of the proposed model

circuit to isolate the gate terminal from source terminal by restricting the flow of current through it. The value of RG has been chosen much higher than the values of R_1 and R_2 so that it acts like an open circuit. We have also added R_3 in the model to measure the overall drain current flowing through R_1, R_2 and g_1. The Resistor R_3 contributes nothing to the operation of the macro model but helps in plotting the overall drain current. The main three designed components of our macro model are R_1, R_2 and g_1 which are cosine function of the gate bias. R_1 and R_2 are expressed as [18].

$$R1 = \left(\frac{CVp}{CI2 - \frac{2*CVp}{CR1+CR2*Cos(CF1*\pi*Vgs)}}\right) \Big/ K_1 \quad (1)$$

$$R2 = \left(\frac{CVp}{CI2 - \frac{2*CVp}{CR1+CR2*Cos(CF1*\pi*Vgs)}}\right) \Big/ K_2 \quad (2)$$

From the ideal characteristics of single electron transistor, it is observed that the gate to source voltage mainly have two functions. It acts as a parameter for uplifting the I_d Vs V_{ds} curve for different values of V_{gs} keeping the nature of the curve intake. It also act as a variable for Ids Vs Vgs curve which is oscillatory in nature. Considering these facts, the expression for the novel component g_1 is expressed as

$$g1 = (CR3 * Sin(\pi * Vgs))/K_3 \quad (3)$$

Here the Sine term gives the oscillatory nature of the Ids Vs Vgs curve and the overall value of this expression gives a dc value.

By controlling the values of fitting parameters properly we can control the characteristics of the proposed model in the desired range of operation. It can be observed from (1) and (2) that two scaling factors K_1 and K_2 have been included in the expression of R1 and R2 respectively. K_1 and K_2 have been incorporated in the design to change the range of the drain current without affecting the V–I characteristics of the model. As the values of R_1 and R_2 are dependent on scaling factors, same value of K_1 and K_2 is chosen to maintain the symmetry of the device. The designer has the freedom to select either symmetric or asymmetric SET just by changing the values of K1 and K2. Though there are some advantages of asymmetric SET, we have focused only on analysis of the characteristics of SET with symmetric tunnel junctions in this study. One more scaling factor (K_3) has been included in the design as given in (3) to control the vertical shift of I_{ds}–V_{ds} curve for a specific gate bias.

3 Simulation results

The proposed model of the single electron transistor is simulated in SPICE environment using the following parameter values: the gate capacitance Cg = 3.2aF, the junction capacitace Cj = 1.6aF, and the temperature T = 30 K [18]. The values for the fitting parameters to get the desired result are chosen as CF1 = 40 [18], Cvp = 0.02, CI2 = 0.2×10^{-9}, CR1 = 300×10^6 and CR2 = 220×10^6. It can be observed from Fig. 4 that the coulomb blockade and non coulomb blockade regions are clearly distinguishable in the I_{ds}–V_{ds} characteristics of the model. With increase in V_{gs} the graph shifts upward along vertical axis. Even though this

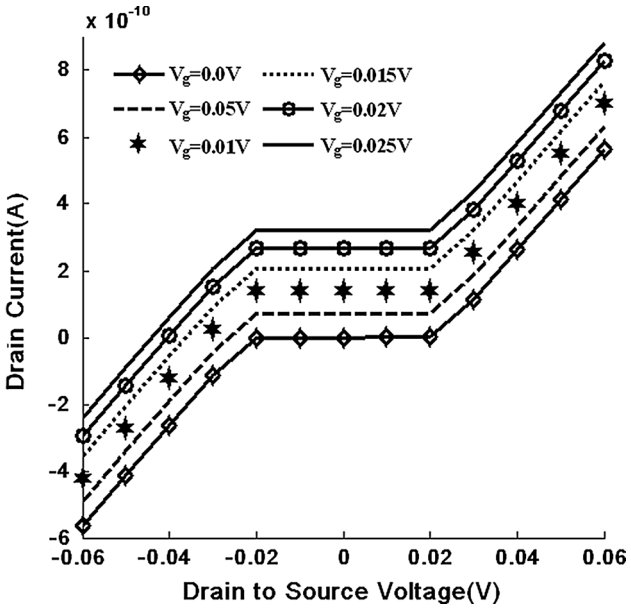

Fig. 4 Current–voltage characteristics of the designed SET where the gate biases is varied from $V_g = 0.0$ V to $V_g = 0.25$ V with an increment of 0.05 V. For simplicity we have assumed $K_1 = K_2$

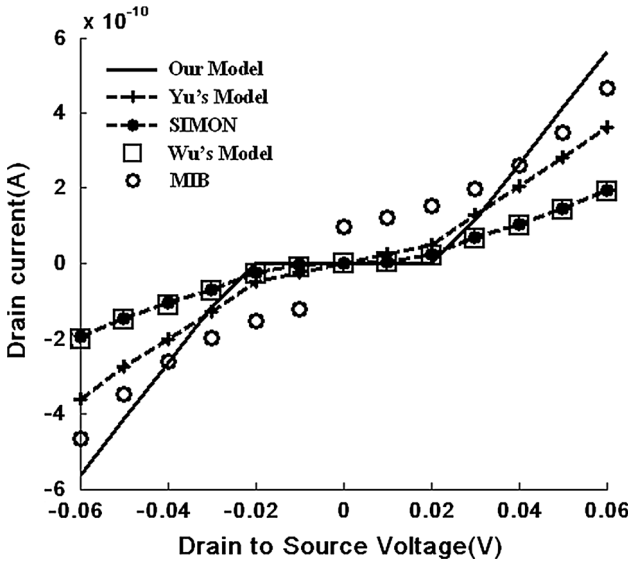

Fig. 5 Comparison of the I_{ds}–V_{ds} characteristics for zero gate to source voltage obtained from Yu's model, Wu and Lin's model, SIMON 2.0 and verilog-A model MIB under the condition $R_D = R_S = 100\ M\Omega$, $C_{TD} = C_{TS} = 1.6$ aF, and T = 30 K. The parameters for our macro model are CF1 = 40, $C_{VP} = 0.02$, $CI2 = 0.2 \times 10^{-9}$, $CR1 = 300 \times 10^{+6}$, $CR2 = 220 \times 10^{+6}$. The value of RG is taken as $50 \times 10^9\ \Omega$

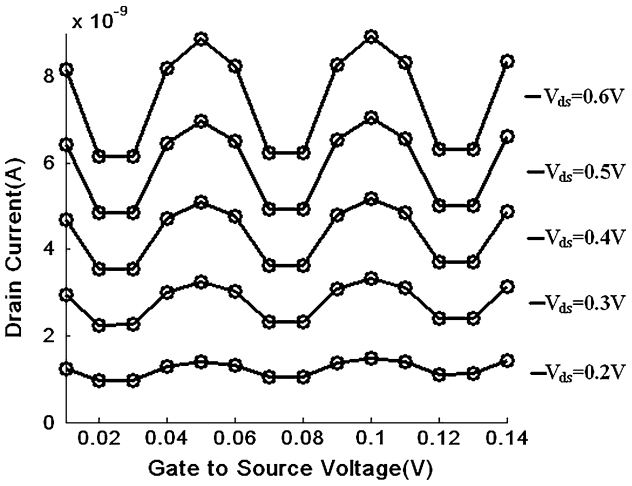

Fig. 6 Coulomb oscillation characteristics of the proposed SET for various drain to source voltage

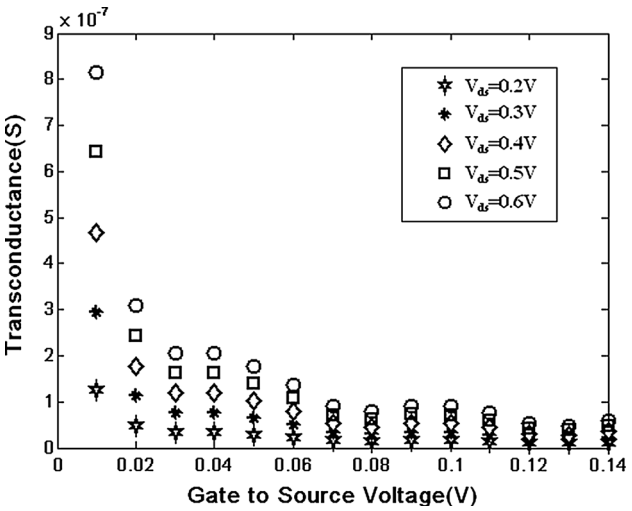

Fig. 7 Transconductance characteristics of the proposed macro model. Here V_{ds} has been chosen as the parameter whose values are varied from 0.2 to 0.6 V, with an increment of 0.1 V

vertical shift is observed in Yu's model, the nature of shift is not fixed. Figure 5 shows the comparison of I_{ds}–V_{ds} characteristics obtained from SIMON [29], MIB model [30], Yu's model, Wu's model and our model for both coulomb blockade and non coulomb blockade regions. It is observed that in the coulomb blockade region of the characteristics, the results obtained using our model closely matches with that of the most popular simulation software SIMON. Among all the models, the drain current of our model covers the maximum range which can be controlled by choosing suitable values of the scaling factors.

The coulomb oscillation characteristics considering V_{ds} as a parameter is shown in Fig. 6. It is observed that with increase in V_{ds} the peak value of the characteristic curve increases and the oscillations look more prominent. Therefore, it can be concluded that SET gives better result for higher values of V_{ds} compared to lower values. The transconductance characteristics of the proposed macro model have been shown in Fig. 7. It is observed that transconductance is a decreasing function of V_{gs} and for values greater than 0.07 V, almost all the transconductance values lie between 0 and 10 μS. Here the positive transconductance part of the characteristics have been shown considering positive values of V_{gs} only, whereas the negative transconductances can also be obtained by taking negative V_{gs} values. A comparison regarding computational overhead for each category (Monte Carlo based, SPICE macro model and master equation based) is given in Table 1. It can be observed that circuits designed with macro model takes lesser time compared to other approaches.

4 Single electron inverter

A single electron inverter is designed using the proposed model as shown in Fig. 8 to verify the validity of the proposed model for single-electron circuits. The voltage transfer characteristic of the single electron inverter along with the results obtained from MIB and SIMON is shown in Fig. 9. The DC input is being varied from −0.02 to 0.02 V. The static characteristic closely matches that of the ideal one. The logic '1' and logic '0' values are clearly

Table 1 Comparison of computational time for different circuits using Monte Carlo based, SPICE macro model and master equation based approach

Logic circuit (simulated in a Intel core i3 processor)	No. of devices	Monte Carlo method (sec)	Master equation based approach (sec)	Macro model approach (sec)
Inverter	2	1.0	3.63	0.9
NAND gate	3	2.0	3.97	1.22
Master–slave JK flipflop	8	3.0	4.3	1.6

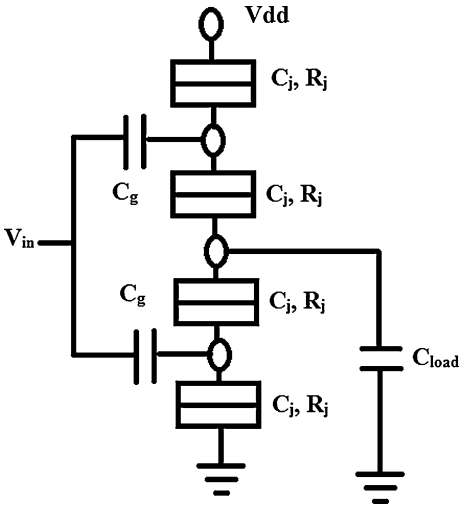

Fig. 8 Single electron transistor based inverter Circuit. C_{load} is the output load capacitance, Cj and Rj are tunnel junction capacitance and resistance respectively

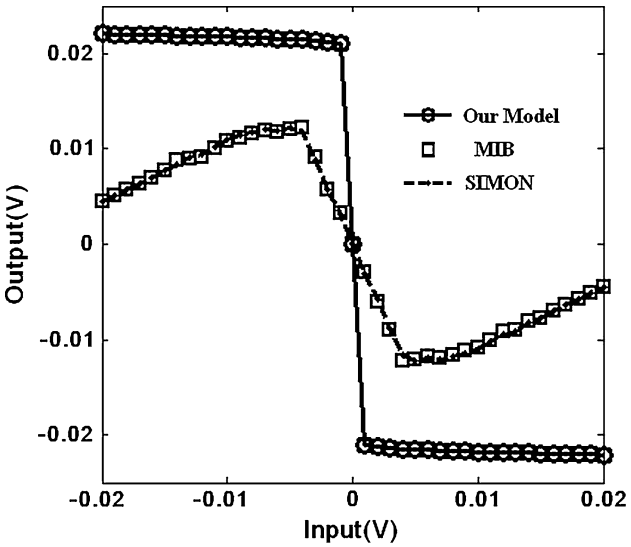

Fig. 9 Static chracteristics of an SET inverter cell, as predicted by MIB, SIMON and our model. The SET parameters for SIMON and MIB are $R_S = R_D = 1$ MΩ, $C_{TD} = C_{TS} = 1$ aF, $C_{G1} = 3$ aF, the output load capacitor is $C_L = 1$ aF, and the parameters for our macro model is CF1 = 40, $C_{VP} = 0.02$, CI2 = 0.2×10^{-9}, CR1 = $300 \times 10^{+6}$, CR2 = $220 \times 10^{+6}$. The value of RG is taken as 50×10^9 Ω

distinguishable for the designed inverter, also the gain of the designed inverter is greater than one. The simulation results obtained from SIMON and MIB model are almost same and the output range is between −0.01 and 0.01 V which is less than that obtained from our model.

It is observed that in all respects, the inverter designed using our model gives better result compared to others. In the inverter circuit, the value of the load capacitor is considered to be large enough to ensure that each SET in the inverter can work independently. The transient characteristic of the designed inverter circuit is shown in Fig. 10. The output pulse is an exact opposite replica of the input pulse which proves that our model performed well for the test input. The simulation results obtained from the popular simulation software SIMON and well accepted verilog-A MIB model have also been plotted in the same graph so that a comparison can be drawn.

The comparison with Monte Carlo simulation (SIMON) and MIB model demonstrates the accuracy of the proposed macro model in both static and dynamic regimes. We have further investigated the effect of parameters on the noise margin of the inverter circuit. We observed that R_G affects the SET logic robustness significantly compared to the other parameters. The effect of R_G on the static characteristics of the inverter cell is demonstrated in Fig. 11. As the value of R_G increases, the characteristics curve moves towards the ideal characteristics and hence the noise margin is improved. With the value of R_G equal to 50 GΩ, the designed inverter shows the best result and further increase in its value does not affect the characteristics curve. The values of noise margin for different values of R_G are depicted in the inset of Fig. 11. It is observed that for all the values of RG, $NM_L = NM_H$, so instead of representing it in ratio form, we have represented the noise margin in absolute form. Starting from RG = 10 GΩ to RG = 20 GΩ, the noise margin increases rapidly after which the slope decreases. The minimum value of absolute noise margin ($NM_H = NM_L = 0.25$ V) is obtained for RG = 10 GΩ, whereas the maximum value is obtained ($NM_H = NM_L = 0.286$ V) for RG = 50 GΩ.

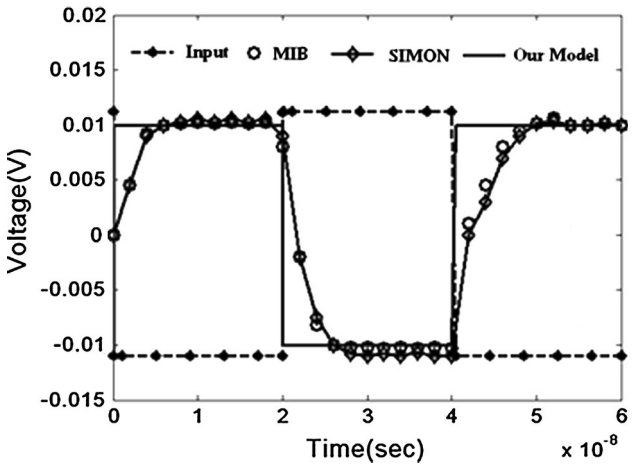

Fig. 10 Transient characteristics of an SET inverter cell, as predicted by MIB, SIMON and our model. The SET parameters for SIMON and MIB are $R_S = R_D = 1$ MΩ, $C_{TD} = C_{TS} = 1$ aF, $C_{G1} = 3$ aF, the output load capacitor is $C_L = 1$ aF, and the parameters for our macro model is CF1 = 40, $C_{VP} = 0.02$, CI2 = 0.2×10^{-9}, CR1 = $300 \times 10^{+6}$, CR2 = $220 \times 10^{+6}$. The value of RG is taken as 50×10^9 Ω

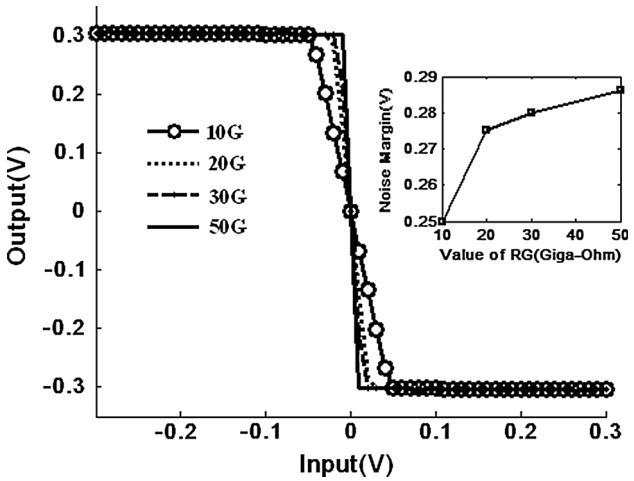

Fig. 11 Effect of RG on the static characteristics of the inverter circuit

5 Multiple peak NDR circuit

The negative differential resistance circuit has a wide variety of applications such as in memory circuit, analog-to-digital converter, oscillators, logic circuit, delta sigma modulator, cellular neural network [31, 32]. Heji et al. [33] first proposed SET based NDR circuit. Later Mahapatra et al. [30] proposed a more versatile architecture with an improved dynamic range of the NDR region. Due to its potential to reach ultra high speed and to reduce circuit complexity, multiple peak NDR circuit has been employed in multiple valued logic circuits, frequency multiplier and

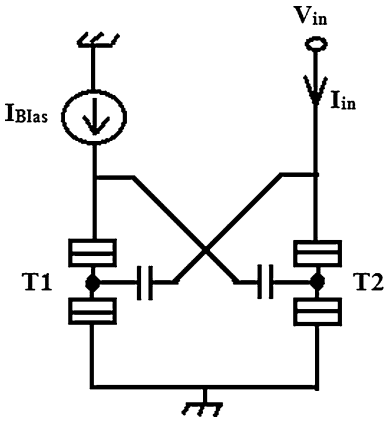

Fig. 12 Schematic diagram of the multi peak NDR circuit with two cross coupled single electron transistors and one current source used for biasing the transistor T1. The parameter values used are CF1 = 40, $C_{VP} = 0.02$, CI2 = 0.2×10^{-9}, CR1 = $300 \times 10^{+6}$, CR2 = $220 \times 10^{+6}$ (for T1) and CR1 = $300 \times 10^{+6}$, CR2 = $220 \times 10^{+6}$ (for T2). The value of RG is taken as 10×10^6 Ω

in multiple valued memory circuits [34–36]. A multiple peak NDR circuit based on single electron transistor and MOS transistor is proposed by Inokawa et al., but nothing has been reported based on single electron transistors only. We have presented a multiple peak NDR circuit based on single electron transistor [30]. The designed circuit consists of two cross connected SETs as depicted in Fig. 12. Here a feedback loop is created by the current biased transistor T1, which controls the current I_{in}, flowing through the transistor T2. I–V characteristics of the designed multi peak NDR cell for different bias current has been shown in Fig. 13. We investigated the effect of different parameters on the characteristics of the multi peak NDR circuit. The parameter CR1 increases the NDR region where as CR2 helps to get a proper peak for different NDR regions. The parameter R_G has the maximum effect on the characteristics plot as it controls the number of NDR regions for a fixed range of input voltage. As the value of RG decreases, the number of NDR region increases as depicted in Fig. 14.

6 Integrator

We have designed an integrator circuit based on single electron transistors [37] as shown in Fig. 15. Here the transistor T1 is biased using Vdd and transistor T2 is biased using Vgs. The input Vin is connected to the gate of transistor T1 and to the drain of transistor T2. So transistor T2 works in a pass transistor format. Finally the output is received across the capacitor C_L. The input and output waveform of the designed circuit is shown in Fig. 16. It can be observed that the input is a sine wave where as the output is a cosine wave which proves that the designed

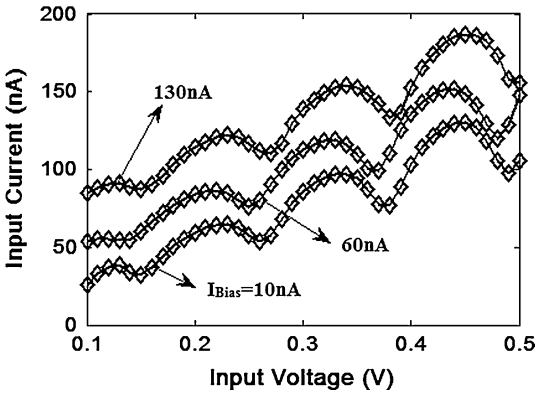

Fig. 13 Characteristics of the designed multi peak NDR circuit for different bias current simulated in SPICE environment. The parameter values used are CF1 = 40, $C_{VP} = 0.02$, CI2 = 0.2×10^{-9}, CR1 = $420 \times 10^{+6}$, CR2 = $5 \times 10^{+6}$ (for T1) and CR1 = $330 \times 10^{+6}$, CR2 = $330 \times 10^{+6}$ (for T2), the value of RG is taken as 10×10^{6} Ω

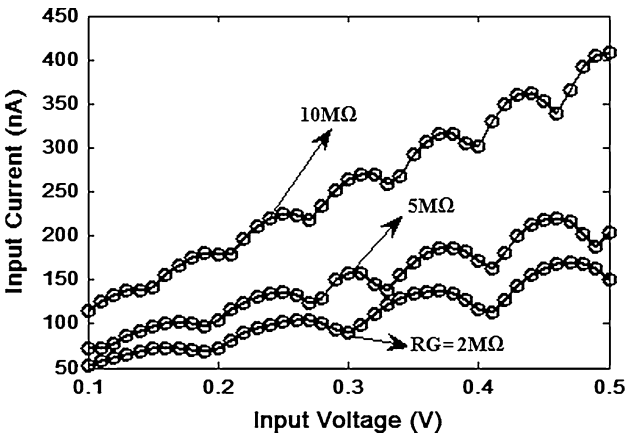

Fig. 14 Effect of Rg on the characteristics of the multi peak NDR circuit. The parameter values used are CF1 = 40, $C_{VP} = 0.02$, CI2 = 0.2×10^{-9}, CR1 = $420 \times 10^{+6}$, CR2 = $5 \times 10^{+6}$ (for T1) and CR1 = $330 \times 10^{+6}$, CR2 = $330 \times 10^{+6}$ (for T2). The value of the bias current is 60 nA

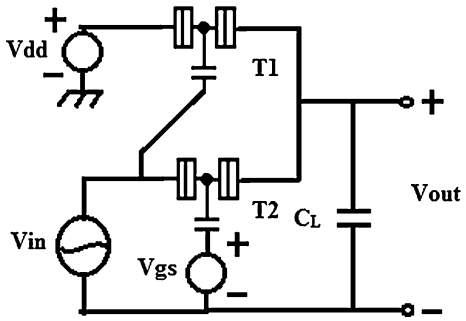

Fig. 15 Schematic diagram of the integrator circuit. The parameter values used are CF1 = 40, $C_{VP} = 0.02$, CI2 = 0.25×10^{-9}, CR1 = $420 \times 10^{+6}$, CR2 = $5 \times 10^{+6}$, CR3 = $0.29e^{-5}$ (for T1) and CI2 = 0.15×10^{-9}, CR1 = $330 \times 10^{+6}$, CR2 = $3 \times 10^{+6}$, CR3 = $0.7e^{-7}$ (for T2), the value of RG is taken as 2×10^{6}Ω

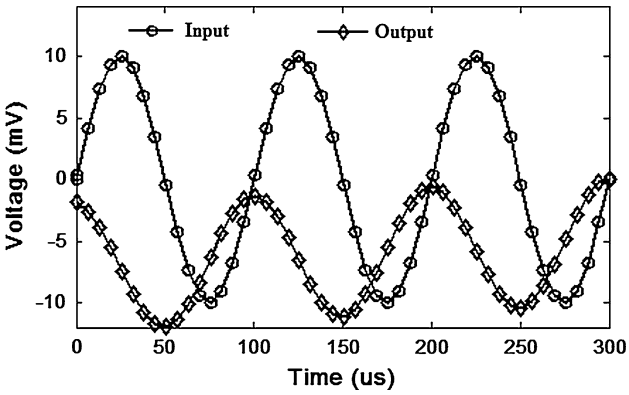

Fig. 16 Transient characteristics of the designed integrator circuit

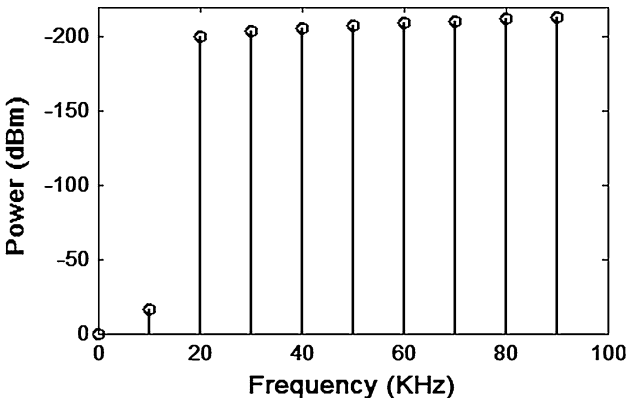

Fig. 17 Plot of the harmonic distortion of the designed circuit

circuit is working satisfactorily. The linearity of the designed circuit is analyzed with the harmonic and intermodulation distortion analysis [38]. In SPICE environment the harmonic distortion analysis is done using four command which instructs the simulator to perform a harmonic decomposition by calculating the fourier coefficients of the input waveform and finally calculates the total harmonic distortion (THD) [39]. We perform the harmonic distortion analysis of the circuit where the fundamental frequency is considered as 10 kHz and the number of harmonics is nine. The result of the analysis is plotted after normalizing the power of the harmonics in dBm and shown in Fig. 17. It is observed that the maximum power of −15.95 dBm is observed for the fundamental frequency 10 kHz and for other frequencies the power is around −200 dBm which is very much lower compared to the power of the input waveform. Finally the THD is obtained as 2.94 % which proves that the designed circuit is highly immune to the harmonic distortion. Intermodulation distortion is another quantity that signifies the linearity of the designed circuit. The problem is SPICE does not provide any command to analyze the intermodulation distortion. So the

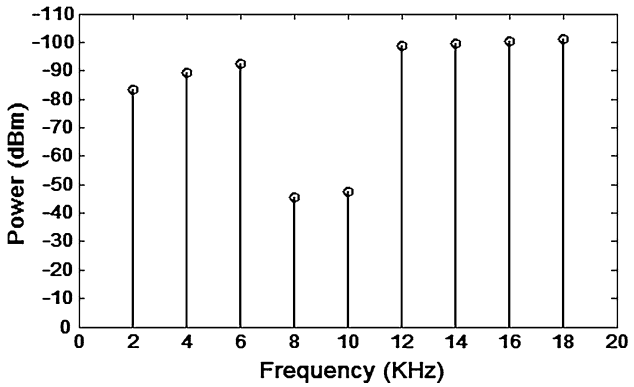

Fig. 18 Plot of the intermodulation distortion of the designed circuit

intermodulation distortion of the circuit is analyzed using total difference frequency distortion (TDFD) test [40]. Actually the TDFD test uses the same four command keeping in mind the fact that all frequencies of interest have to be the multiple of the fundamental so the fundamental frequency is chosen as the submultiple of the stimulating frequencies [41]. In TDFD analysis a two tone test is performed where the stimulating frequencies are 8 kHz, 10 kHz and the fundamental frequency is 2 kHz. The result of the intermodulation distortion analysis is shown in Fig. 18. It is observed from the figure that the power of the stimulating frequencies are much higher compared to the second order intermodulation frequency (2 kHz) and third order intermodulation frequency (12 kHz). Finally the intermodulation distortion is calculated as 1 %.

7 Conclusion

In this paper an improved macro model of SET is reported for efficient simulation of single-electron circuits in SPICE simulation environment. A voltage control current source is incorporated in the existing model to predict the characteristic of the model in the coulomb blockade region. Some scaling factors are included which can be selected by the designer to switch between symmetric SET and asymmetric SET and also to scale the drain current. By comparison with other types of simulation methods, it is shown that our model closely matches the results obtained from the popular simulation software SIMON. Simulation results of the single electron inverter designed using the proposed model are promising enough to justify the use of the model for designing single electronics logic circuits. It was found that among all the parameters, R_G shows maximum effect on the noise margin of the designed inverter cell. It is observed that with increase in R_G, the noise margin is improved and the maximum value of absolute noise margin is obtained for R_G equal to 50 GΩ. The designed multi peak NDR circuit is found to work satisfactorily. Among all the parameters, CR1, CR2 and RG have significant effects on the characteristics of the multi peak NDR cell. CR1 and CR2 affects the shape of the NDR region where as R_G controls the number of NDR regions for a fixed range of the input voltage. The integrator circuit is found to work satisfactorily. The harmonic and Intermodulation distortion is calculated as 2.94 % and 1 % respectively, which proves that the designed circuit is highly immune to the harmonic and intermodulation components of the designed integrator circuit.

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References

1. Chen, R. H., Korotkov, A. N., & Likharev, K. K. (1996). Single-electron transistor logic. *Applied Physics Letters, 68*(14), 1954–1956.
2. Likharev, K. K. (1999). Single-electron devices and their application. *Proceedings of the IEEE, 87*(4), 606–632.
3. Ionescu, A. M. & Michel J. (2002) Few electron devices: towards hybrid CMOS-SET integrated circuits. *Design Automation Conference,* 88–93.
4. Jain, A., & Sarkar, S. K. (2012). Design and reliability analysis of a 4:1 MUX using single electron tunneling technology based threshold logic gate. *Journal of Electron Devices, 15*, 1241–1248.
5. Zardalidis, G., & Karafyllidis, I. (2006). Design and simulation of a nanoelectronic single-electron control—not gate. *Microelectronics Journal, 37*(2), 94–97.
6. Uchida, K., Koga, J., Ohba, R., & Toriumi, A. (2003). Programmable single-electron transistor logic for future low-power intelligent LSI: proposal and room-temperature operation. *IEEE Transaction on Electron Devices, 50*(7), 1623–1630.
7. Chaohong, H., Cotofana, S. D., Jianfei, J., & Qiyu, C. (2004). Analog-to-digital converter based on single-electron tunneling transistors. *IEEE Transaction on VLSI Systems, 12*(11), 1209–1213.
8. Gerousis, C., & Grepiotis, A. (2013). Reconfigurable gate array architecture for logic functions in tunneling transistor technology. *Microelectronics Journal, 44*(8), 706–711.
9. Agarwal, P. B., & Kumar, A. (2011). Design and simulation of octal-to-binary encoder using capacitive single-electron transistors (C-SETs). *Microelectronics Journal, 42*(1), 96–100.
10. Chen, Y. C., Wang, C. Y., & Huang, C. Y. (2013). Verification of reconfigurable binary decision diagram-based single-electron transistor arrays. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 32*(10), 1473–1483.
11. Samanta, D., Ghosh, A., Sarkar, S., & Sarkar, S. K. (2010). Design and simulation of a sequence generator using single electron devices and hybrid architecture. *Journal of Nanoelectronics and Optoelectronics, 5*(1), 323–331.
12. Sui, B., Fang, L., Chi, Y., & Zhang, C. (2010). Nano-reconfigurable cells with hybrid circuits of single-electron transistors and MOSFETs. *IEEE Transactions on Electron Devices, 57*(9), 2251–2257.
13. Deng, G., & Chen, C. (2011). Hybrid CMOS-SET arithmetic circuit design using Coulomb blockade oscillation characteristic. *Journal of Computational and Theoritical Nanoscience, 8*(8), 1520–1526.

14. Jana, A., Singh, N. B., Sing, J. K., & Sarkar, S. K. (2013). Design and simulation of hybrid CMOS-SET circuits. *Microelectronics Reliability, 53*(4), 592–599.
15. Wei, W., Han, J., & Lombardi, F. (2013). Design and evaluation of a hybrid memory cell by single-electron transfer. IEEE Transactiosn on Nanotechnology, *12*(1), 57–70.
16. Jain, A., Singh, N. B., Ghosh, A., & Sarkar, S. K. (2014). Stability and reliability analysis of Hybrid CMOS-SET Circuits—a new approach. *Journal of Computational and Theoritical Nanoscience, 11*(12), 2519–2524.
17. Zhang, W., & Wu, N. J. (2007). A novel hybrid phase-locked-loop frequency synthesizer using single-electron devices and CMOS transistors. *IEEE Transaction on Circuits and System, 54*(11), 2516–2527.
18. Koppimen, P. J., Stewart, M. D., & Zimmerman, M. J. (2013). Fabrication and electrical characterization of fully CMOS-compatible Si single-electron devices. *IEEE Transactions on Electron Devices, 60*(1), 78–83.
19. Yu, Y. S., Hwang, S. W., & Ahn, D. (1999). Macromodeling of single-electron transistors for efficient circuit simulation. *IEEE transaction on Electron Devices., 46*(8), 1667–1671.
20. Wu, Y. L. & Lin, S. T. (2003) An improved single electron transistor model for SPICE application. *Nanotech 3*.
21. Karimian, M. R., & Dousti, M. (2010). A new SPICE macromodel for the simulation of single electron circuits. *Journal of the Korean Physical Society, 56*(4), 1202–1207.
22. Yu, Y. S., Hwang, S. W., & Ahn, D. (2005). Transient modelling of single-electron transistors for efficient circuit simulation by SPICE. *IEE Proceedings on Circuits, Devices and Systems*, *152*(6), 691–696.
23. Abuelma'atti, M. A. (2009). Improved analysis of the single-electron transistor mixer. *Analog Integrated Circuits and Signal Processing, 61*, 223–229.
24. Wei, W., Han, J., & Lombardi, F. (2014). Robust HSPICE modeling of a single electron turnstile. *Microelectronics Journal*, *45*(4), 394–407.
25. Wasshuber, C. (2002). Single –electronics –how it works. How it's used. How it's simulated. In *Proceedings of the International Sympposium On Quality Electronic Design*.
26. Ferrenberg, A. M., Landau, D. P., & Wong, Y. J. (1992). Monte Carlo simulations: hidden errors from 'good' random number generators. *Physics Review Letters, 69*(23), 3382–3384.
27. Wasshuber, C. (2001). *Computational single-electronics*. New York: Springer.
28. Mahapatra, S. (2006). *Hybrid CMOS single-electron-transistor device and circuit design.* London: Artech House Publication.
29. Wasshuber, C., Kosina, H., & Selberherr, S. (1997). SIMON–a simulator for single-electron tunnel devices and circuits. *IEEE Transaction on Computer aided design of integrated circuits and systems, 16*(9), 937–944.
30. Mahapatra, S., Banerjee, K., Pegeon, F., & Inoescu, A. M. (2003). A CAD framework for co-design and analysis of CMOS-SET hybrid integrated circuits. In *Proceedings of the ICCAD.*
31. Mahapatra, S., Vaish, V., Wasshuber, C., Banerjee, K., & Ionescu, A. M. (2004). Analytical modeling of single electron transistor for hybrid CMOS-SET analog IC design. *IEEE Transactions on Electron Devices, 51*(11), 1772–1782.
32. Gan, K. J., Tsai, C. S., & Liang, D. S. (2009). Novel multiple-selected and multiple-valued memory design using negative differential resistance circuits suitable for standard SiGe-based BiCMOS process. *Analog Integrated Circuits and Signal Processing, 59*(2), 161–167.
33. Heij, C. P., Dixon, D. C., Hadley, P., & Mooij, J. E. (1999). Negative differential resistance due to single-electron switching. *Applied Physics Letters, 74*(7), 1042–1044.
34. Gan, K. J. (2000). Novel four-peak or five-peak current-voltage characteristics for three negative differential resistance devices in series. *Solid-State Electronics, 44*(9), 1597–1602.
35. Gan, K. J. (2001). The low-high-low IV characteristics of five to seven peaks based on four NDR devices. *IEEE Transactions on Electron Devices, 48*(8), 1683–1687.
36. Shin, S., & Kim, K. R. (2013). Novel design of multiple negative-differential resistance (NDR) device in a 32 nm CMOS technology using TCAD. In *Proceeding of International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)* (pp. 316–319).
37. Cai L., Kang Q., & Shi D. Y. (2013). Study of a second order low pass filter based on hybrid SETMOS. In: *Proceedings of the SPIE8762, PIAGENG 2013: Intelligent Information, Control and Communication Technology for Agricultural Engineering*.
38. Abulem'atti, M. T. (2011). Harmonic and intermodulation performance of carbon nanotube field-effect transistor-based and single-electron tunnelling transistor-based inverting amplifiers. *International Journal of Electronics, 98*(7), 847–861.
39. Tuinenga, P. W. (1988). *A guide to circuit simulation and analysis using PSPICE*. Upper Saddle River: Prentice Hall, New Jersey.
40. Rathmell J., Scott J. & Parker A. TDFD-based measurement of analog-to-digital converter nonlinearity. *Journal of Audio Engineering Society, 45*(4), 832–840.
41. Scott, J., & Parker, A. (1995). Distortion analysis using SPICE. *The Journal of the Audio Engineering Society, 43*(12), 1029–1040.

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