Analog Integr Circ Sig Process (2015) 82:181–187
DOI 10.1007/s10470-014-0450-6

Low insertion loss, high power handling and good performance 90° phase shifter for X-band radar application

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Received: 5 March 2014 / Accepted: 19 August 2014 / Published online: 19 November 2014

Abstract In this paper, a monolithic microwave integrated circuit 90° phase shifter circuit for X band radar application is designed and fabricated using 0.1 μm pseudomorphic high electron mobility transistor technology based on GaAs with $f_t = 85$ GHz. This block is used in passive phase shifters. The structure of 90° used double single port double throw (SPDT) in both input/output. The SPDT used a high yield and good performance switch. The switches have low insertion loss and phase variation. The measurement results of 90° block with −6 V control voltage indicate that the insertion loss is less than −1.6 dB and phase shift is 87 ± 3.5° over 8–12 GHz. The 1 dB compression point (P_1dB) is more than 25 dBm. The die size is 1 mm^2. The measurements show good correlation between simulation and measurement results. So, the result demonstrates the great potential of the proposed block for high performance phased array radar systems.

Keywords Phase shifter · pHEMT · SPDT · MMIC

1 Introduction

Today's PPS are important elements in phase array radars, antenna switch and positioning systems. The phase shifters have two kinds of structures, passive and active. The PPS is a bilateral network, but the active-type is an unilateral network. The advantage of PPS is that it can be used to both transmit and receive path at the same time. The structure of PPS is a combination of low/high pass filters. For radio frequency (RF)/microwave switch design, PIN diode [1], Micro Electro Mechanical System (MEMS) [2], Low Temperature Co-fire Ceramic (LTCC) [3] and Field Effect Transistor (FET) (in both GaAs and CMOS processes) are the four commonly used technologies. However, considering the cost, integration, switching speed, power consumption, and linearity, FET switches based on III–V compounds (e.g., GaAs), especially pHEMTs, are the most attractive choice on the wireless communication market [4].

Many different passive and active MMICs PS have been reported in literature [5–7]. A switched high-pass/low-pass phase shifter for the X band with 6-bit resolution has been reported in [6]. The technology can be implemented in MMICs. So, the designer can be able to use lumped elements such as inductors, capacitors, resistors and transistors together. Here the dimension of the chip is much smaller than other methods [8]. All connections between elements (microstrip lines) are simulated using advanced design system (ADS) Momentum for planar electromagnetic simulations to take into account the coupling between adjacent microstrip lines.

In Sect. 2, the optimization of switch will explain how to use phase shifter designing. In Sect. 3, the configuration of SPDT is introduced and in the last Sect. 4, the structure of 90° phase shifter block indicated optimized switch and SPDT are presented.

2 Optimized switch

In this section, an original method is used to describe the investigation on the improvement of the insertion loss and

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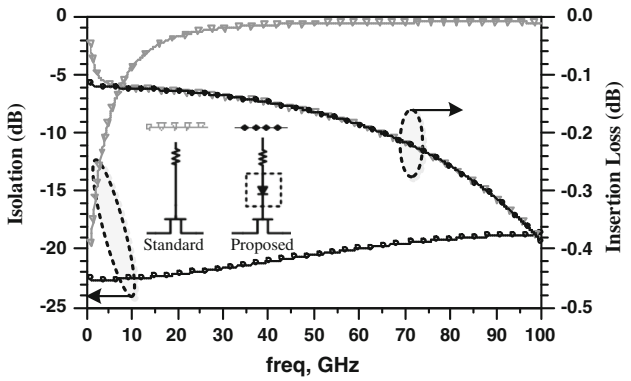

Fig. 1 Simulated insertion loss and isolation for the switch in standard and proposed form

isolation of the pHEMT switch. Fundamentally, the role of the switch is very important in PPS designing. In PPSs, some undesired effects occur due to parasitic elements of transistors. These affects are found in the phase and insertion loss variation of the PPS. The Fig. 1 illustrates GaAs pHEMT switch in standard and proposed form. In this method, the undesired effects of transistors are reduced.

As shown in Fig. 1, a diode is added on a gate of transistor. Usually, a diode is modeled by a dynamic resistor (R_d) and a capacitor (C_d). The C_d is the junction capacitor between the anode and cathode of diode in the depletion region. The C_d and gate capacitor (C_g) are series together as shown in Fig. 2. Also, the C_d is significantly less than C_g.

$$\frac{C_{g\times}C_d}{C_g + C_d} \cong C_d \quad if \quad C_g \gg C_d \tag{1}$$

The Eq. (1) shows that C_g of the proposed switch is smaller than the standard form. The Fig. 2 shows the equivalent circuit of the proposed switch. The parameters of the proposed switch in Fig. 1 can be modeled with parasitic elements like as $a\ C_d$, C_{gs}, C_{ds}, C_{gd}, g_{ds} and $g_m.v_{gs}$ as shown in Fig. 2. The next equation is extracted from the solving of polynomial function for the Z-parameters matrix where the Z_{in} is the input impedance of the proposed switch.

The input impedance of the proposed switch is given by:

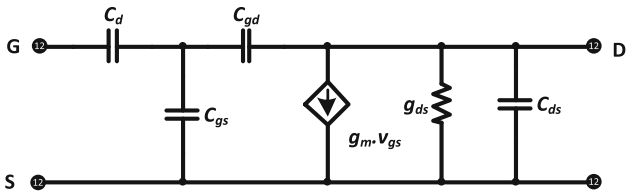

Fig. 2 Equivalent circuit of the proposed switch

If we assume that the transistor is unilateral, then C_{gd} is omitted.

$$Z_{in} = \frac{\left[g_{ds}.R_L.C_d + C_d + G_{ds}.R_L.C_{gs} + C_{gs}\right] + \left[C_d.C_{ds}.R_L\right]s}{\left[g_{ds}.C_{gs}.C_d.R_L + C_{gs}.C_d\right]s + \left[C_{gs}.C_{ds}.C_d.R_L\right]s^2} = \frac{(C_d + C_{gs})}{s(C_{gs}.C_d)} \tag{3}$$

The behaviors of the switches are illustrated in Fig. 3 [4]. Figure 3 shows the study of the characteristics of the standard and proposed switches. The Fig. 3(a) shows that the gate capacitor (C_g) of the transistor changes significantly in 20 GHz bandwidth. If the input power increases, the non-linear effect of the transistor will be found through the large signal phenomenon of pHEMT transistor. But in Fig. 3(b), the C_g of the proposed switch is decreased, hence, the large signal and nonlinear effects of the new method are declined. Table 1 shows the value of C_g as a function of frequency from Fig. 3.

As it is evident in the Fig. 4 and Table 1, the proposed switch is suitable for the phase shifter designing. Because in PPS application, the behavioral switch have an undesirable effect in PPS specification, so, it has been tried to design a good switch with minimum undesirable effect. The Fig. 4 shows that the phase variation is decreased in proposed switch, whereas in standard switch the phase variation is too much in on–off mode. In standard switch, the phase variation is more than 15 degrees, but in the proposed, phase variation is maximum 2 degrees in on–off mode@ 10 GHz. Some parameters such as phase uniformity, the best insertion loss and maximum input power handling are very important in PPSs [9].

$$Z_{in} = \frac{\left[g_{ds}.R_L.C_d + C_d + g_{ds}.R_L.C_{gd} + g_m.R_L.C_{gd} + C_{gd} + g_{ds}.R_L.C_{gs} + C_{gs}\right] + \left[C_{ds}.C_d.R_L + C_{gd}.C_d.R_L + C_{gd}.C_{ds}.R_L + C_{gs}.C_{gd}.R_L\right]s}{C_d.\left[g_{ds}.R_L.C_{gd} + g_m.R_L.C_{gd} + C_{gd} + g_{ds}.R_L.C_{gs} + C_{gs}\right]s + C_d.\left[C_{ds}.C_d.R_L + C_{gd}.C_d.R_L + C_{gd}.C_{ds}.R_L + C_{gs}.C_{gd}.R_L\right]s^2} \tag{2}$$

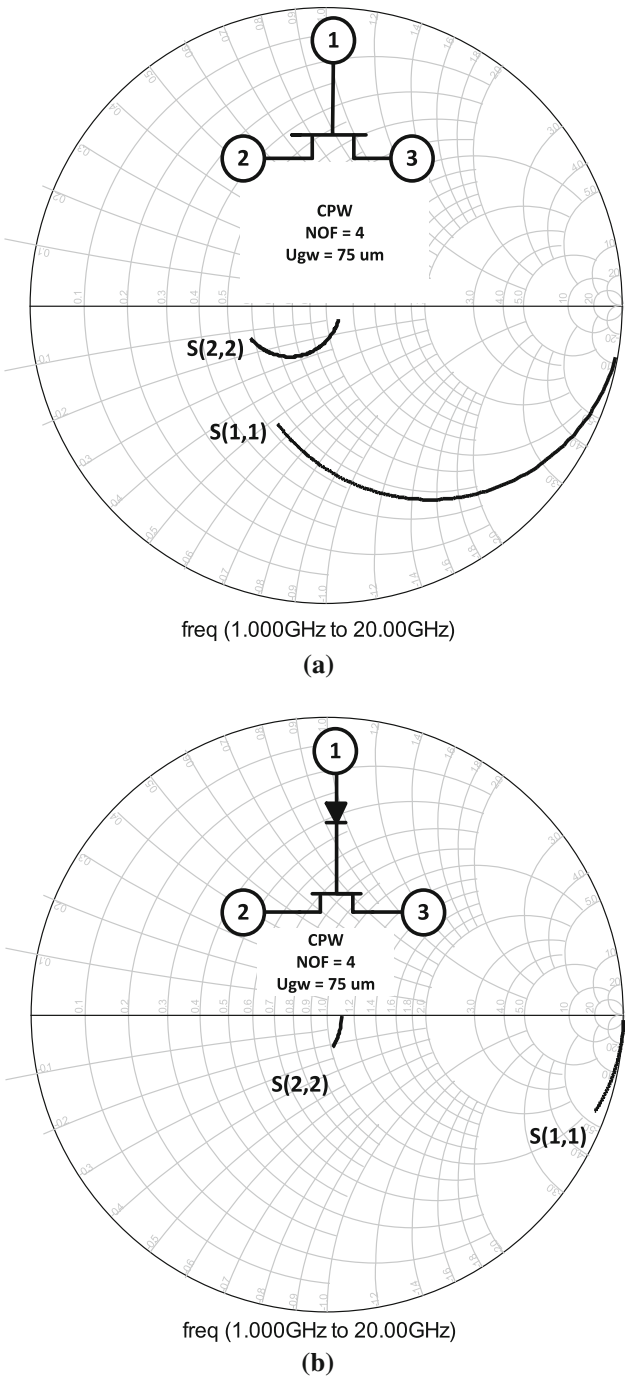

Fig. 3 The smith chart of (**a**) Standard switch structure. (**b**) Proposed method structure

Table 1 The C_g values in standard and the proposed method

	1 GHz	10 GHz	20 GHz
($C_g$of Standard mode) pF	0.0286	0.293	0.638
($C_g$of Proposed mode) pF	0.0032	0.0311	0.0627

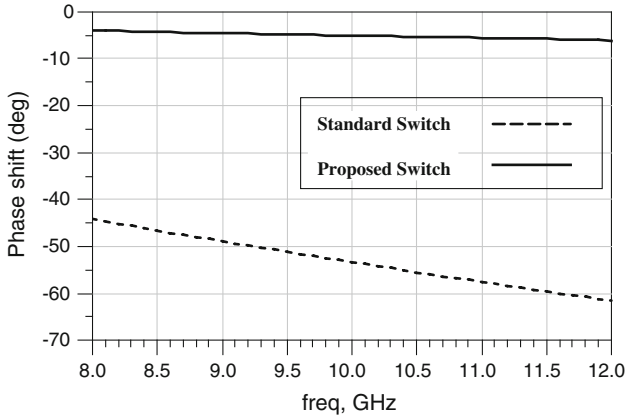

Fig. 4 The phase shift of standard and proposed switch

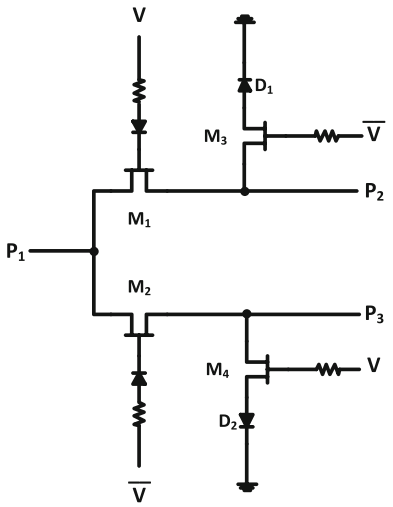

Fig. 5 Schematic of SPDT

3 SPDT structure

In this section, we describe how by using the proposed method, the performance of the GaAs switch can be improved. The schematic circuit diagram of the implemented SPDT switching circuit is shown in Fig. 5. The size of the transistors has been selected for high power handling. Since the breakdown voltage in a GaAs HEMT is larger than the pinch off voltage, power handling of the switch is set by the open channel current limit of a transistor. Therefore, in order to have a design with acceptable power handling, total gate width of the series pHEMTs has to be selected in a fitting manner [10].

In Fig. 5, the series transistors M_1 and M_2 perform the main switching functions, and the shunt transistor M_3 and M_4 increase the isolation of the switch. Under these conditions, one of the RF inputs (P_2 or P_3) is connected to the common

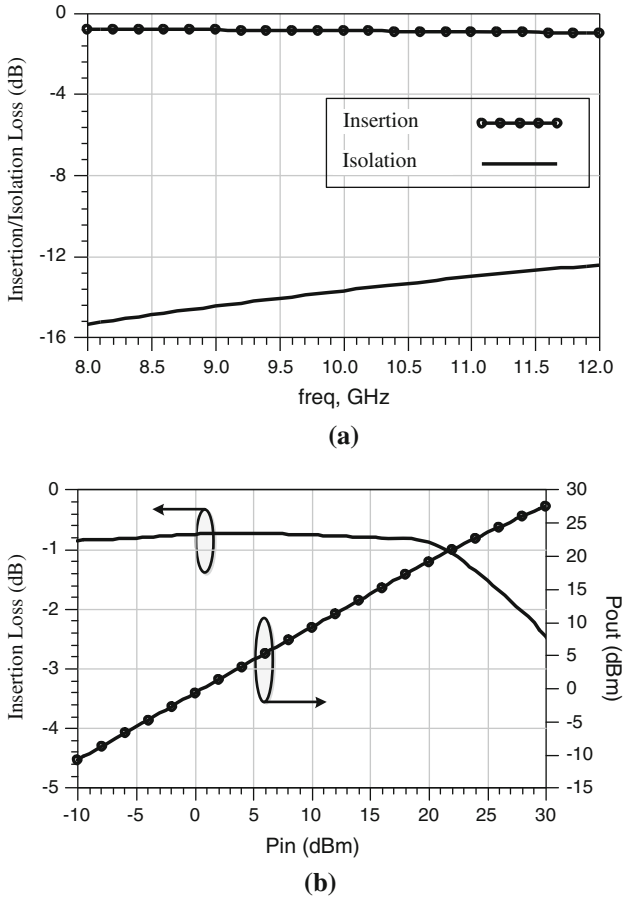

Fig. 6 (**a**) Simulation result of Insertion loss and Isolation (**b**) Simulation result of 1 dB compression point and pout versus pin

port (P_1) through a low value of the complementary HEMT's on—resistance, while another one is isolated from the common port by the large value of the drain—source resistance in the "off" mode. The D_1 and D_2 are increased the power handling of SPDT switches. The Fig. 6 shows the simulation results of the proposed SPDT switch. As shown in Fig. 6(a), the insertion loss is 0.7 dB with variation of ±0.1 dB and its isolation is better than 28 dB. Also, Fig. 6(b) shows that the P_1dB of the circuit is 28 dBm [10].

4 90° phase shifter Block structure

The Fig. 7 illustrates the proposed 90° block structure. This configuration has two SPDT switches in input and output of block. The proposed block includes a high pass and a band pass filter.

The Fig. 8(a) shows the structure of high pass filter through which the SPDT switch leads signal to high pass section of the proposed block. Then, the signal finds a path to the ground via L_1 and C_1.

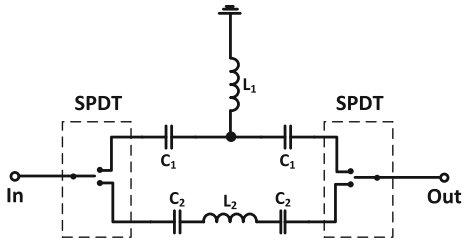

Fig. 7 Proposed 90° block

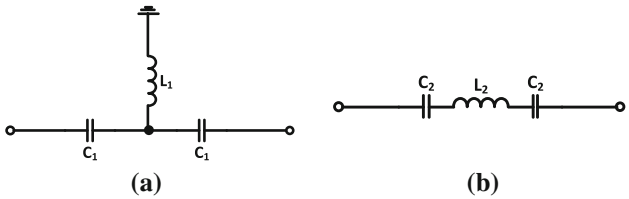

Fig. 8 (**a**) High pass filter (**b**) Band pass filter

The Fig. 8(b) illustrates the band pass filter at the second state. The signal finds the ground via L_2, C_2 to 50 Ω impedance matching.

The Eqs. (4) and (5) are the transfer function of high pass and band pass filter respectively.

$$H_{H.P}(s) = \frac{\left(C_1^2 L_1 Z_0\right)s^3}{1 + (C_1 Z_0)s + (2C_1 L_1)s^2 + \left(C_1^2 L_1 Z_0\right)s^3} \tag{4}$$

$$H_{B.P}(s) = \frac{\left(C_2^2 Z_0\right)s^2}{(2C_2)s + \left(C_2^2 Z_0\right)s^2 + \left(C_2^2 L_2\right)s^3} \tag{5}$$

The S-parameters of the high pass filter are given by:

$$S_{H.P11} = \frac{j(2C_1\omega - C_1^2 L_1\omega^3 - Z_0^2 L_1\omega)}{2Z_0 - 2Z_0 L_1 C_1\omega^2 + j\left(Z_0^2 L_1\omega + 2C_1\omega - C_1^2 L_1\omega^3\right)} \tag{6}$$

$$S_{H.P12} = \frac{2Z_0}{2Z_0 - 2Z_0 L_1 C_1\omega^2 + j\left(Z_0^2 L_1\omega + 2C_1\omega - C_1^2 L_1\omega^3\right)} \tag{7}$$

By using the above equations, the best values of L_1 and C_1 are calculated. To achieve the best impedance matching in input and output circuit of central angular frequency (ω_0), $S_{11} = 0$ should be considered, so the relationships between L_1 and C_1 are:

$$L_1 = \frac{2C_1\omega_0}{C_1^2\omega_0 + Z_0^2\omega_0} \tag{8}$$

From S_{21}, the values of phase shift, L_1 and C_1 in central angular frequency (ω_0) are obtained as follows:

$$\Delta\varphi = -\tan^{-1}\left(\frac{Z_0^2 L_1\omega_0 + 2C_1\omega_0 - C_1^2 L_1\omega_0^3}{2Z_0 - 2Z_0 L_1 C_1\omega_0^2}\right) \quad (9)$$

$$C_1 = \frac{Z_0\tan(\Delta\ \varphi\ /2)}{\omega_0}; L_1 = \frac{\sin(\Delta\varphi)}{Z_0\omega_0} \quad (10)$$

Also,the S-parameters of the band pass filter are given by:

$$S_{B.P11} = \frac{j(C_2L_2\omega^2 - 2)}{2Z_0C_2\omega + j(C_2L_2\omega^2 - 2)} \quad (11)$$

$$S_{B.P12} = \frac{2Z_0C_2\omega}{2Z_0C_2\omega + j(C_2L_2\omega^2 - 2)} \quad (12)$$

By using above equations, the best value of L_2 and C_2 are calculated. To give the best impedance matching of circuit in ω_0, S_{11} should be equal to zero. So L_2 and C_2 are:

$$\frac{d}{d\omega}\left(-\tan^{-1}\left(\frac{L_2C_2\omega^2 - 2}{2Z_0C_2\omega}\right)\right)\Big|_{\omega=\omega_0} = \frac{-1}{Z_0C_2\omega_0^2} \quad (13)$$

By evaluating Eqs. (9) and (13), the best value of C_2 and L_2 are achieved.

$$L_2 = \frac{2Z_0\tan(\Delta\varphi/2)}{\omega_0}; C_2 = \frac{1}{2Z_0\omega_0\tan(\Delta\varphi/2)} \quad (14)$$

The values of C_1, C_2, L_1 and L_2 are shown in Table 2.

Table 2 Components values

Elements	C_1	C_2	L_1	L_2
Values	0.83*pF*	29*pF*	0.9*nH*	0.6*nH*

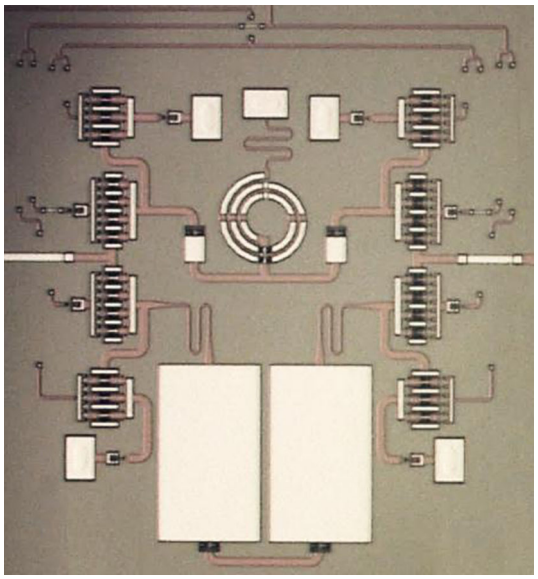

Fig. 9 Photograph of 90° block

The Fig. 9 shows the photograph of 90° block in pHEMT GaAs technology.

The Fig. 10 shows the simulation and the measurement results of 90° phase shifter block. The measured phase shift is 87° ± 3.5° over 8–12 GHz.

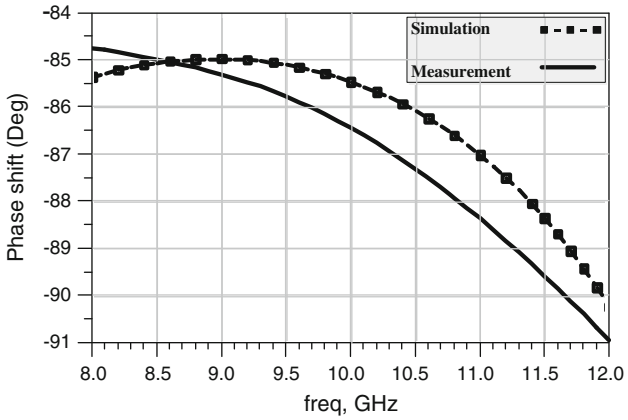

Fig. 10 The measurement and the simulation results of 90° phase shifter

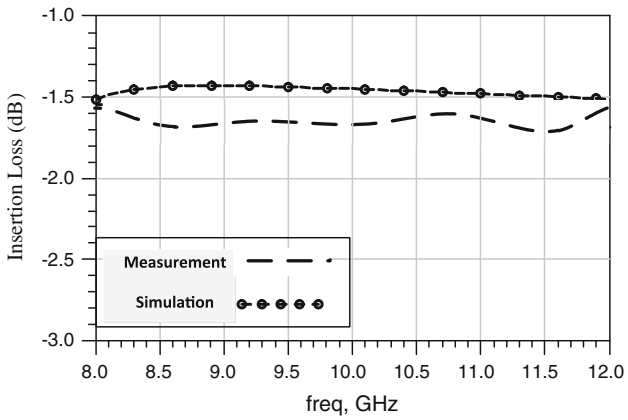

Fig. 11 The measurement and the simulation results of insertion loss

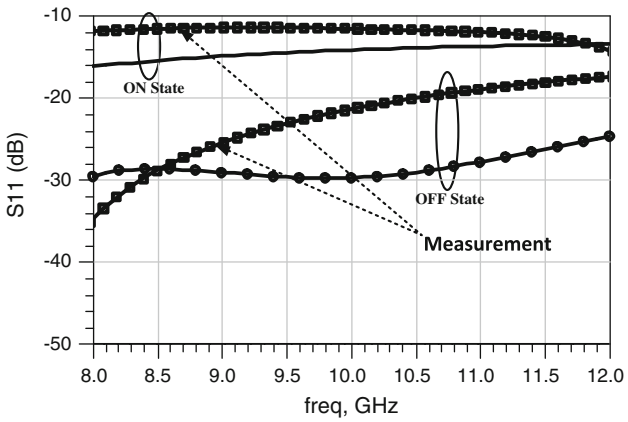

Fig. 12 The measurement and the simulation results of S_{11}

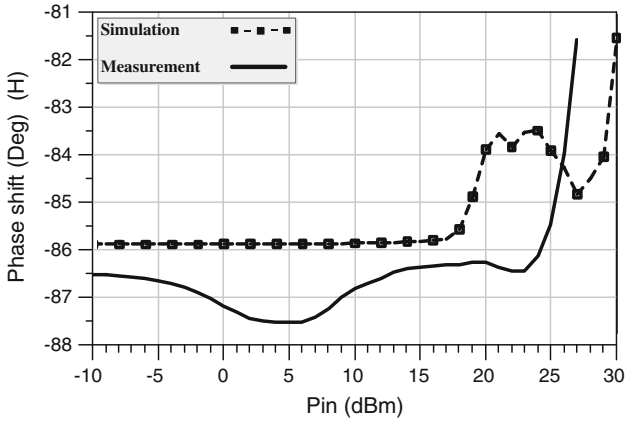

Fig. 13 The measurement and the simulation results of phase variation versus input power

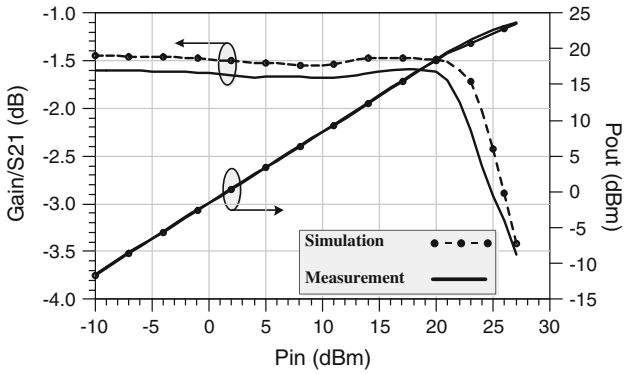

Fig. 14 The measurement and the simulation results of 1 dB compression point and output power versus input power

Table 3 Comparison of 90° phase shifter blocks

Process	Freq (GHz)	Phase range	IL (dB)	Ref
0.18 μm RF CMOS	9–15	90° + 4°	−16 ± 1.3*	[4]
0.5 μm pHEMT GaAs	4–12	93° ± 7°	− 1.95 ± 0.7	[11]
0.6 μm MESFET GaAs	4–6	90°	−1.2 ± 0.5	[12]
0.3 μm pHEMT GaAs	40–60	90°	−4 ± 0.4	[13]
0.25 μm pHEMT GaAs	3.6–4.2	90°	<6.4*	[14]
0.15 μm pHEMT GaAs	8–12	87° ± 3.5°	−1.6 ± 0.1	This work

* All states of phase shifter

The Fig. 11 shows the simulation and the measurement of the insertion loss of the proposed block. The measured insertion loss is −1.6 ± 0.1 dB over 8–12 GHz.

The Fig. 12 shows the simulation and the measurement of the S_{11} of 90° block in "ON" and "OFF" state.

The Fig. 13 illustrates phase shift of the block versus input power. This diagram shows that the output phase shift has less phase variation in 25 dBm input power.

In the Fig. 14, 1 dB compression point of the proposed block is determined. The result shows that P_1dB is 25 dBm.

The Table 3 presents a detailed comparison between some of the same studies.

5 Conclusions

In this study, by using 0.15 μm pHEMT technology, a MMIC 90° block is fabricated and measured in X-band. In this work, a transistor switch is optimized by using the proposed method, and then utilized in the SPDT switch. The SPDT switch is used in the proposed block. The measurement results of the proposed block show that the insertion loss is −1.6 dB, the phase shift is 87° ± 3.5° over 8–12 GHz. The phase linearity and P_1dB are more than 25 dBm. The die size is 1 mm^2. The measurements hence show a good correlation between simulation and the measurement results. So, the results demonstrate the great potential of the proposed block for high performance phased array radar systems.

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