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A new current mode implementation of a balanced-output-signal generator

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Abstract This paper presents a new current mode implementation of a balanced-output-signal generator that utilizes an operational floating current conveyor (OFCC) as a basic building block. The OFCC, as a current-mode device, shows flexible properties with respect to other current or voltage-mode circuits. The advantages of the proposed current mode balanced-output-signal generator (CMBG) are threefold. Firstly, it offers an accurate phase and amplitude performance over a wide bandwidth without requiring matched resistors. Secondly, it has a differential input and it can provide either current or voltage outputs. Finally, the proposed CMBG circuit offers a significant improvement in accuracy compared to other CMBGs based on the current conveyor. The proposed CMBG has been analyzed, simulated and experimentally tested. The experimental results verify that the proposed CMBG outperforms existing CMBGs in terms of the number of basic building blocks used and accuracy.

Keywords Current mode circuits · Operational floating current conveyor · Current conveyor · Instrumentation · Operational amplifier · Balanced amplifiers

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1 Introduction

Generating a balanced-output-signal from a sinusoidal input over a large frequency range is used in many application areas, such as synchronous detection [1] and lock-in-based systems [2]. Also, signals which are both amplitude matched and phase balanced are very important in the transmission of analog signals over long lines in order to reject unwanted common mode signals [3]. Nowadays, lab-on-a-chip which requires the integration of the actuation and sensing parts, as well as the read-out circuitry in a single chip, needs also a wide bandwidth balanced-output-signal generator to generate two 180° out-of-phase signals from a sinusoidal input [4].

The voltage-mode balanced-output-signal generators (VMBG) based on an operational amplifier, as shown in Figs. 1 and 2, require the matching of amplifier poles [5, 6]. Also, due to the fixed gain bandwidth product of the operational amplifier, the system cannot simultaneously provide both a minimum phase-difference error between the outputs and minimum amplitude difference without compromising the bandwidth performance of the system. Additionally, VMBGs require precise resistor matching to achieve high common-mode rejection ratio (CMRR) [5, 6].

A current-mode balanced output signal generator (CMBG) is used as shown in Fig. 3 [7]. It uses two op-amps working in conjunction with two second-generation

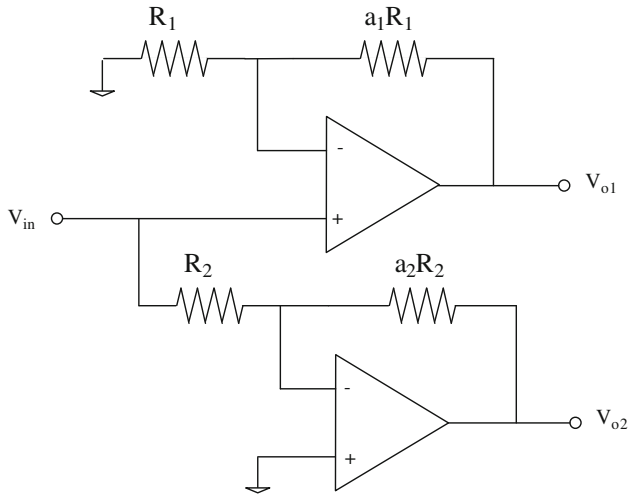

Fig. 1 Circuit proposed in Ref. [5] for 180° out-of-phase signals

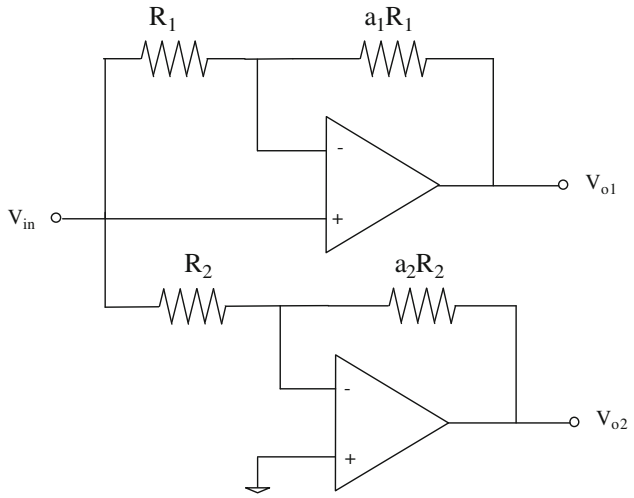

Fig. 2 Circuit proposed in Ref. [6] for 180° out-of-phase signals

current conveyors (CCII). Unlike the circuits in Ref. [5] and [6], this circuit does not require precise matching of amplifier poles. However, when this circuit, see Fig. 3, works in a single ended input mode, i.e., v_{in1} is active and v_{in2} is grounded, the phase difference and the amplitude between v_{o1} and v_{o2} are: [7]

$$\Delta\phi = \tan^{-1}(\omega C_1 R_G) + 180^{o} \quad (1)$$

$$|\Delta V|_{dB} = 10\log(1 + \omega^2 C_1^2 R_G^2) \quad (2)$$

Equation (1) shows that there is a phase error [$\tan^{-1}(\omega C_1 R_G)$] which increases with both the frequency and R_G. Thus in order to minimize the phase error, R_G should be as small as possible. Equation (2) also indicates an increase of the output-signal amplitude difference (error) with frequency and with R_G. Additionally, this approach suffers from higher power consumption and a more complicated circuit topology when compared with the topologies shown in Figs. 1 and 2. Recently, a CMBG based on four CCIIs is presented [8] and is shown in Fig. 4, where the two Op-amps (OP1 and OP2) in Fig. 3, are replaced by two CCIIs. Figure 4 is taking into consideration the equivalent input resistance at X terminal (R_X) of the CCIIs. This circuit used only CCII as a building block. However, this circuit has the same issue associated with the circuit shown in Fig. 3, i.e., when works in a single ended input mode, v_{in1} is active and v_{in2} is grounded, the phase difference and the amplitude between v_{o1} and v_{o2} are exactly the same ones given in Eqs. (1) and (2). Thus, it suffers from increasing the output-signal amplitude difference (error) with frequency and with R_G. In this paper, the new proposed CMBG circuit has the following advantages: (1) it is simple and has symmetric circuit topology, (2) it has much improved amplitude and phase difference compared with the other voltage or current-mode balanced output signal generators, and (3) it has a differential input and it can provide either a balanced output current or voltage. The proposed CMBG circuit is based on the Operational Floating Current Conveyor (OFCC), which exhibits flexible characteristics with respect to other current-mode or voltage-mode devices [9–13]. The remainder of this paper is organized as follows:

Section 2 introduces and reviews the basic concept of the OFCC and its characteristics. Also, a simple model of the OFCC, as well as, the effect of feedback on the OFCCs performance are presented and discussed. A detailed analysis of the proposed CMBG is presented in Sect. 3. Section 4 presents the simulation and experimental results. Section 5 discusses the performance of the proposed CMBG and compares it to the performance of currently used CMBGs. Section 6 concludes the paper and discusses the merits of the proposed CMBG based on the experimental findings.

2 The operational floating current conveyor (OFCC)

The OFCC is a five-port network, comprised of two inputs and three output ports, as shown in Fig. 5 [9–13]. In this diagram, the port labeled X represents a low impedance current input, port Y is a high impedance input voltage, W is a low impedance output voltage, and Z+, and Z− are the high impedance current outputs with opposite polarities. The OFCC operates where the input current at port X is multiplied by the open loop transimpedance gain Z_t to produce an output voltage at port W. The input voltage at port Y appears at port X and thus a voltage tracking property exists at the input port. Output current flowing at

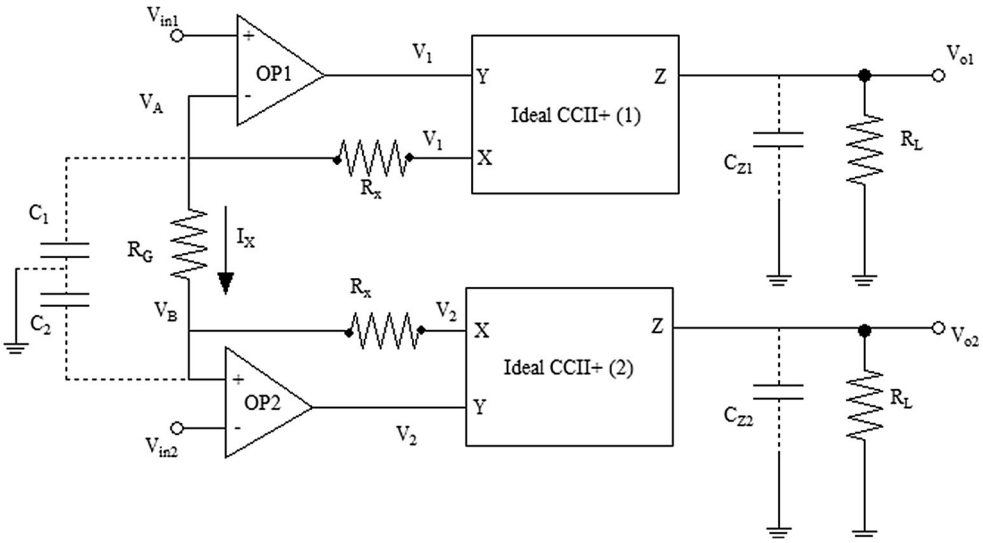

Fig. 3 Two CCII+ used in conjunction with two Op-amps CMBG, Ref. [7]

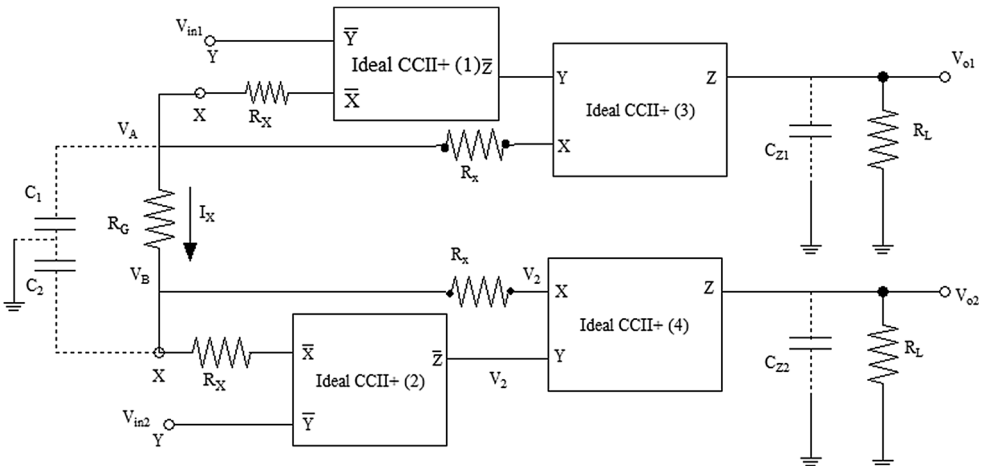

Fig. 4 Four CCII+ based CMBG, Ref. [8]

port W is conveyed in phase to port Z+ and out of phase with that flowing into port Z−, so in this case a current tracking action exists at the output port. Thus, the transmission properties of the ideal OFCC can be conveniently described as:

$$\begin{bmatrix} i_y \\ v_x \\ v_w \\ i_{z+} \\ i_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ i_W \\ v_{z+} \\ v_{z-} \end{bmatrix} \quad (3)$$

where i_y and v_y are the inward current and voltage at the Y port, respectively, as shown in Fig. 5. i_x and v_x are the input current and voltage at the X port, respectively. i_w and v_w are the output current and voltage at W port, respectively. i_{z+} and v_{z+} are the output current and voltage at Z + port, respectively. Similarly, i_{z-} and v_{z-} are the output current and voltage at the Z− port, respectively. Z_t represents the impedance between X and W ports.

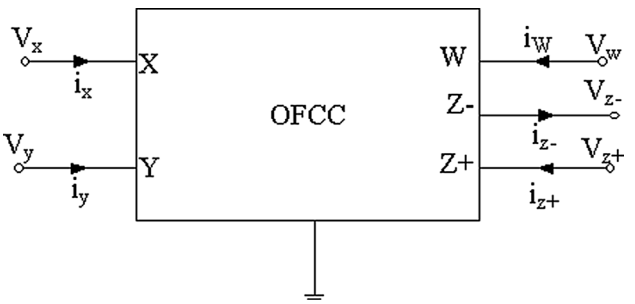

Fig. 5 Block diagram representation of the operational floating current conveyor

The OFCC can be implemented by applying the principle of supply current sensing to a current feedback (CFB) op-amp [14] such as illustrated in Fig. 6. The current mirrors CM1 and CM2 establish the output current at port Z+. Also, CM1 and CM2 and their cross-coupling with the current mirrors CM3 and CM4 through the current steering

transistors CS1 and CS2 generate a complementary output current at port Z−. The OFCC is basically designed to be used in a closed loop configuration, with current being fed back from port W to port X [9].

2.1 A simple model

A simple model of the OFCC based on the circuit topology shown in Fig. 6 is illustrated in Fig. 7. In this figure, R_x and R_y are the resistances of the CFB op-amp at negative (−) and positive (+) ports, respectively. C_x and C_y are the input capacitances of CFB op-amp (−) and (+) ports, respectively. R_T and C_T are the small signal resistance and internal compensation capacitance of the CFB op-amp. R_{Z+} and R_{Z-} are the small signal output resistances of the respective current mirrors at node Z+ and Z−, respectively

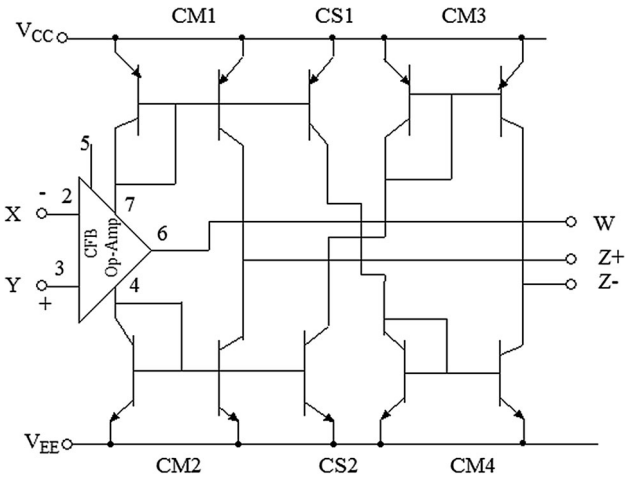

Fig. 6 Circuit scheme of the OFCC

at the d.c. operating point. C_{Z+} and C_{Z-} represent the output capacitances of the respective current mirrors at nodes Z+ and Z−, respectively.

2.2 OFCC with feedback

The OFCC, unlike the CCII, is designed with a feedback resistor between W and X, i.e. negative feedback between W and X. This feedback resistor allows the OFCC to operate at a positive or negative current-conveyor while simultaneously reducing the input resistance at X port [11]. Also, the negative feedback improves the dc stability as well as the transfer function accuracy [7, 9, 10].

To understand why the input resistance at the X terminal is reduced by negative feedback, consider the OFCC with feedback resistor R_W, as shown in Fig. 8. The capacitive reactance to ground due to C_x is quite high and can therefore be ignored in the frequency range of interest. In this case, the input current i_{in} is defined as:

$$i_{in} = i_1 + i_e \tag{4}$$

and,

$$i_1 = \frac{v_{in} - v_w}{R_W} \tag{5}$$

where v_{in} is the input voltage at port X, v_w is the output voltage at port W, R_w is the feedback resistance, i_1 is the feedback current, and $i_{.e.}$ is the error current.Using Eq. (3), the output signal voltage v_w is given as,

$$v_w = -i_e Z_t \tag{6}$$

where $Z_t = R_T//(1/j\omega C_T)$. For low frequencies ($\omega << 1/R_T C_T$) the reactance due to C_T is very high and can be ignored. Thus $Z_t \approx R_T$ and

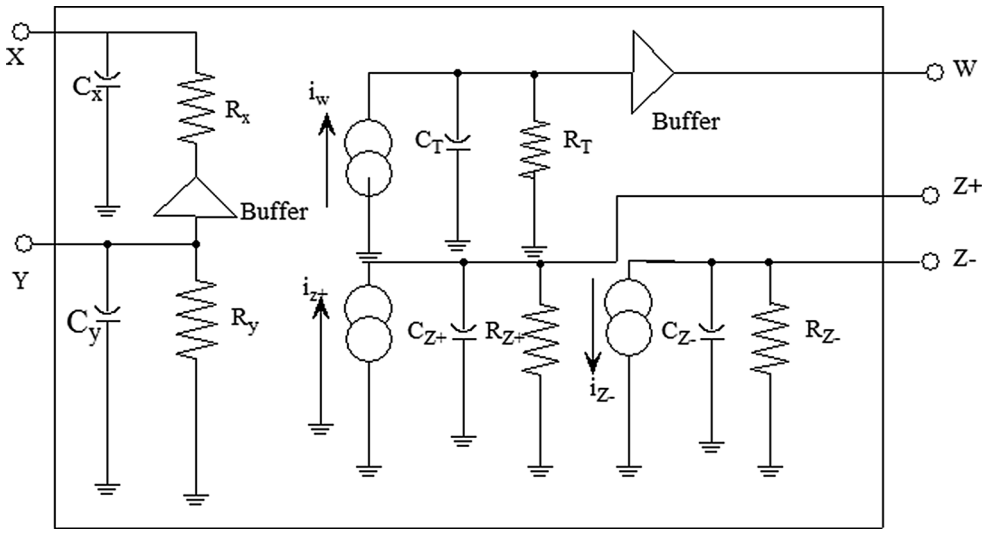

Fig. 7 The OFCC's model, Ref. [10]

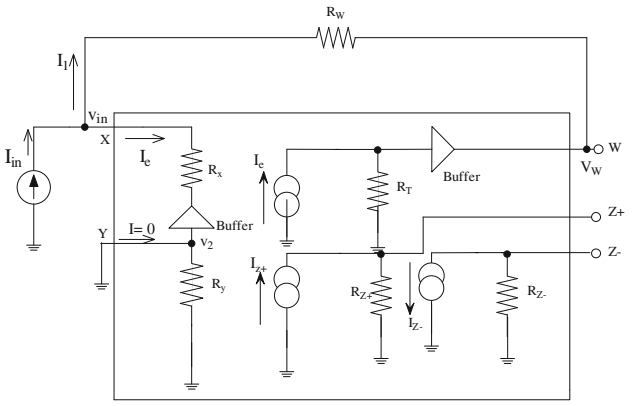

Fig. 8 Circuit to measure OFCC's R_X, Ref. [10]

$$v_w = -i_e R_T \tag{7}$$

Now since the Y port is connected to ground, $v_2 = 0$, and therefore the error current is defined as:

$$i_e = \frac{v_{in} - 0}{R_X}. \tag{8}$$

By substituting Eqs. (5), (7), and (8) in (4), i_{in} can be expressed as

$$i_{in} = \frac{v_{in}(R_X + R_T + R_W)}{R_X R_W} \tag{9}$$

The low frequency input resistance at X port can therefore be expressed as,

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{R_X R_W}{R_X + R_T + R_W}. \tag{10}$$

With typical resistor values of: $R_x = 50\ \Omega$, $R_w = 1\ K\Omega$, and $R_T = 200\ M\Omega$. Equation (10) yields $R_{in} = 0.0025\ \Omega$. Therefore, the input resistance at X is greatly reduced, thus minimizing the voltage tracking error between X and Y, and therefore can be neglected at low frequencies.

3 The proposed CMBG

The proposed CMBG consists of two operational floating current conveyors (OFCC), two feedback resistors (R_{W1} and R_{W2}), a gain determined resistor (R_G) and a ground loads (R_{L1} and R_{L2}), as shown in Fig. 9. The two OFCC are arranged such that the output current into the load resistor R_{L1} is equal and 180° out of phase of the current into R_{L2}. C_1 and C_2 are the parasitic capacitances at the inverting input (X) of OFCC1 and OFCC2, respectively, while C_{Z1}, and C_{Z2} are that parasitic capacitances at the outputs.

Taking into consideration both the voltage and current tracking errors of the OFCC, the current tracking error between ports X, Z + and Z− is:

$$\alpha = 1 - \varepsilon_+ \tag{11}$$

and

$$\gamma = 1 - \varepsilon_- \tag{12}$$

where: ε_+ and ε_- denotes the finite current tracking error at the high impedance output Z+ and Z−, respectively. Thus, the port currents may then be expressed as $i_{z+} = \alpha i_x$ and $i_{z-} = \gamma i_x$.The voltage tracking error between ports X and Y is defined as:

$$\beta = 1 - \varepsilon_V \tag{13}$$

where εV denotes the finite voltage tracking error at the low impedance X from the high input impedance node Y.The voltage at nodes vA and vB, as shown in Fig. 9, can be expressed as:

$$v_A = \beta_1 v_{in1} \text{ and } v_B = \beta_2 v_{in2} \tag{14}$$

where β_1 and β_2 are the voltage tracking error of OFCC (1) and OFCC (2), respectively. Because of the effect of the OFCC, the voltage transfer error is zero, i.e., $\beta_1 = \beta_2 = 1$ [9–12]Thus,

$$v_A = v_{in1} \text{ and } v_B = v_{in2} \tag{15}$$

The current i_x can be expressed as:

$$i_X = i_1 + i_3 \tag{16}$$

$$i_1 = v_{in1}(sC_1) \tag{17}$$

$$i_3 = \frac{v_{in1} - v_{in2}}{R_G} \tag{18}$$

From (17) and (18) into (16),

$$i_x = v_{in1}\left(sC_1 + \frac{1}{R_G}\right) - v_{in2}\left(\frac{1}{R_G}\right) \tag{19}$$

3.1 Differential input mode

For the differential Input mode, $v_{in1} = -v_{in2} = \frac{v_d}{2}$. The resulting current i_x and i_4 can be calculated as:

$$i_x = \frac{v_d}{R_G}\left(\frac{sC_1R_G}{2} + 1\right) \tag{20}$$

Similarly,

$$i_4 = \frac{v_d}{R_G}\left(\frac{sC_2R_G}{2} + 1\right) \tag{21}$$

The output currents i_5 and i_6 are calculated as follows:

$$i_5 = \alpha_1 i_x = \frac{\alpha_1 v_d}{R_G}\left(\frac{sC_1R_G}{2} + 1\right) \tag{22}$$

$$i_6 = \gamma_1 i_x = \frac{\gamma_1 V_d}{R_G}\left(\frac{sC_1R_G}{2} + 1\right) \tag{23}$$

The output voltages v_{o1}, and v_{o2} are:

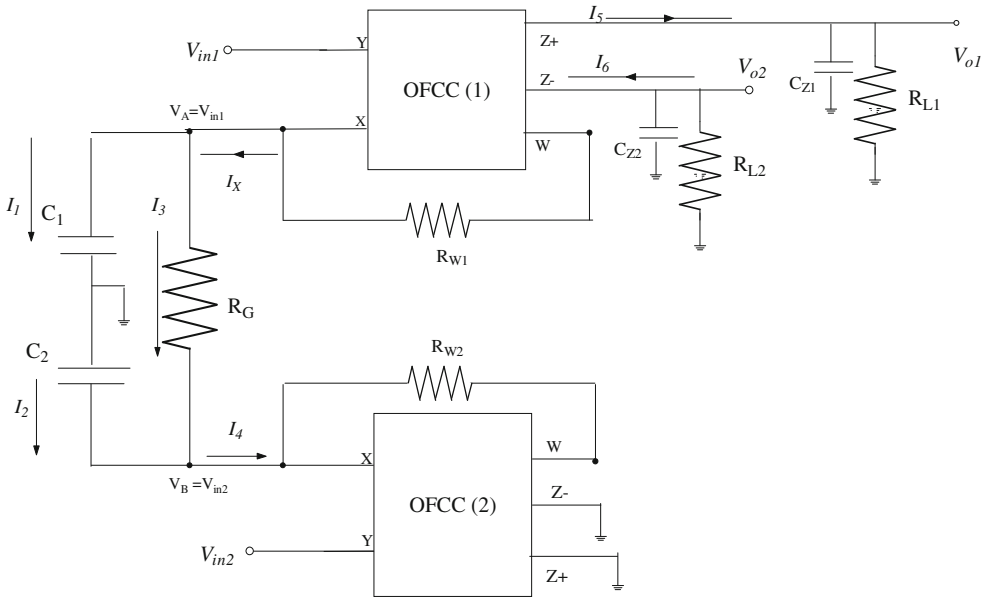

Fig. 9 The Proposed CMBG circuit

$$v_{o1} = (i_5)\left(R_{L1} // \frac{1}{sC_{Z1}}\right) \tag{24}$$

$$v_{o2} = -(i_6)\left(R_{L2} // \frac{1}{sC_{Z2}}\right) \tag{25}$$

where C_{Z1} and C_{Z2} are the output node capacitance at Z +, Z− terminals which are in parallel with R_{L1} and R_{L2}.

Using i_5 and i_6 from Eqs. (22) and (23), respectively, v_{o1} and v_{o2} can now be computed,

$$\frac{v_{o1}}{v_d} = \frac{\alpha_1 R_{L1}(1 + sC_1R_G/2)}{R_G(1 + sC_{Z1}R_{L1})} \tag{26}$$

$$\frac{v_{o2}}{v_d} = -\frac{\gamma_1 R_{L2}(1 + sC_2R_G/2)}{R_G(1 + sC_{Z2}R_{L2})} \tag{27}$$

The phase differences Φ_1, and Φ_2 of v_{o1} and v_{o2} are given by:

$$\phi_1 = \tan^{-1}\left(\frac{\omega C_1 R_G}{2}\right) - \tan^{-1}(\omega C_{Z1}R_{L1}) \tag{28}$$

$$\phi_2 = \tan^{-1}\left(\frac{\omega C_1 R_G}{2}\right) - \tan^{-1}(\omega C_{Z2}R_{L2}) - 180^o \tag{29}$$

The output phase difference $\Delta\Phi_{12}$ is given by:

$$\begin{aligned}\Delta\phi_{12} &= \phi_1 - \phi_2 \\ &= \tan^{-1}(\omega C_{Z2}R_{L2}) - \tan^{-1}(\omega C_{Z1}R_{L1}) + 180^o\end{aligned} \tag{30}$$

The output signal amplitude difference Δv_{12} can be calculated from (26) and (27)

$$\Delta v_{12} = \frac{v_{o1}}{v_{o2}} = \frac{\alpha_1 R_{L1}}{\gamma_1 R_{L2}} \cdot \frac{(1 + sC_{Z2}R_{L2})}{(1 + sC_{Z1}R_{L1})} \tag{31}$$

For ideal OFCCs, $\alpha_1 = \gamma_1 = 1$, thus the output voltage is:

$$\Delta v_{12} = \frac{R_{L1}}{R_{L2}} \cdot \frac{(1 + sC_{Z2}R_{L2})}{(1 + sC_{Z1}R_{L1})} \tag{32}$$

Assuming matched resistors and capacitors, i.e., $R_{L1} = R_{L2}$ and $C_{z1} = C_{z2}$. $\Delta\varphi_{12} = 180°$ and $\Delta v_{12} = 0$ dB, i.e., the phase and amplitude errors disappear. v_{o1} and v_{o2} therefore become balanced amplitude-matched signals. The mismatching impacts of R_{L1}, R_{L2} and C_{z1} and C_{z2} will be discussed and investigated in details in part 4.

3.2 Single ended input mode

For a single ended input, $v_{in1} = v_1$ and $v_{in2} = 0$, then i_x and i_4 can be expressed as:

$$i_x = v_1\left(sC_1 + \frac{1}{R_G}\right) \tag{33}$$

and

$$i_4 = v_1\left(\frac{1}{R_G}\right) \tag{34}$$

Using a routine circuit analysis we can prove that:

$$\frac{v_{o1}}{v_1} = \frac{\alpha_1 R_{L1}(1 + sC_1R_G)}{R_G(1 + sC_{Z1}R_{L1})} \tag{35}$$

$$\frac{v_{o2}}{v_1} = \frac{-\gamma_1 R_{L2}(1 + sC_1R_G)}{R_G(1 + sC_{Z2}R_{L2})} \tag{36}$$

The phase differences Φ_1 and Φ_2 of v_{o1} and v_{o2} are given by:

$$\phi_1 = \tan^{-1}(\omega C_1 R_G) - \tan^{-1}(\omega C_{Z1}R_{L1}) \tag{37}$$

$$\phi_2 = \tan^{-1}(\omega C_1 R_G) - \tan^{-1}(\omega C_{Z2}R_{L2}) - 180^o \tag{38}$$

The output phase differences $\Delta\Phi_{12}$ is given by:

$$\Delta\phi_{12} = \phi_1 - \phi_2 = \tan^{-1}(\omega C_{Z2} R_{L2}) - \tan^{-1}(\omega C_{Z1} R_{L1}) + 180^{o} \quad (39)$$

The output signal amplitude difference Δv_{12} is:

$$\Delta v_{12} = \frac{\alpha_1 R_{L1}}{\gamma_1 R_{L2}} \cdot \frac{(1 + sC_{Z2}R_{L2})}{(1 + sC_{Z1}R_{L1})} \quad (40)$$

For ideal OFCCs, $\alpha_1 = \gamma_1 = 1$, thus the output voltage is:

$$\Delta v_{12} = \frac{R_{L1}}{R_{L2}} \cdot \frac{(1 + sC_{Z2}R_{L2})}{(1 + sC_{Z1}R_{L1})} \quad (41)$$

From (40) and (41), and assuming matched resistors and capacitors (i.e., $R_{L1} = R_{L2}$ and $C_{z1} = C_{z2}$). Then $\Delta\varphi_{12} = 180°$ and $\Delta v_{12} = 0$ dB, i.e., the phase and amplitude errors disappear. v_{o1} and v_{o2} therefore become balanced amplitude-matched signals. The mismatching impacts of R_{L1}, R_{L2} and C_{z1} and C_{z2} will be discussed and investigated in details in part 4.

4 Impact of mismatch variations on the proposed CMBG performance

In this section, the ideal assumption made in Eqs. (31) and (41) where $R_{L1} = R_{L2}$ and $C_{z1} = C_{z2}$, is investigated. It is assumed that resistances R_{L1} and R_{L2} have a mismatch ΔR. Capacitances C_{z1} and C_{z2} are assumed to have a mismatch ΔC. Ten thousands Monte Carlo simulation points are calculated for different values of $\Delta R/R$ and also for different values of $\Delta C/C$. Following that, the resulting magnitude variations around the nominal value of 1.0 and the phase variations around the nominal value of 180° is determined.

4.1 Resistor mismatch

The resistance mismatch variation (i.e., $\Delta R/R$) is assumed to be 2, 5, 10, and 20 %. Monte Carlo simulations are performed to get the corresponding mean and standard deviation of the magnitude and the phase. Figure 10 shows the relative variations of the magnitude and phase (i.e., the standard deviation divided by the nominal mean value) resulting from different resistance mismatch values (i.e., 2, 5, 10, and 20 %) when the operating frequency is 1 MHz.

From Fig. 10, it is obvious that the relative phase variations are higher than the relative magnitude variations, especially at higher resistance mismatch values. In addition, as the resistance mismatch variations increase, the relative magnitude variations increase at a lower rate than that of the relative phase variations.

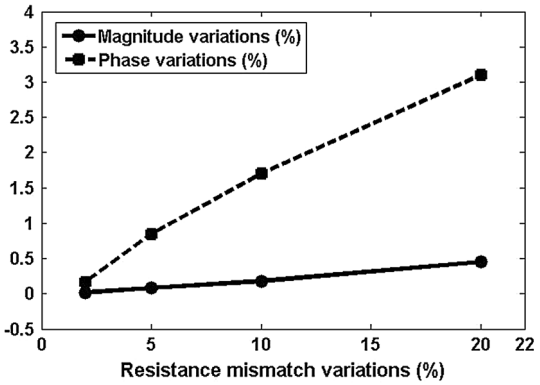

Fig. 10 The relative variations of the magnitude and phase for different resistance mismatch variations

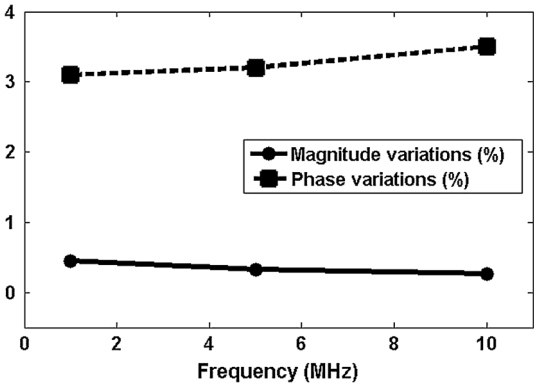

Fig. 11 The relative variations of the magnitude and phase at different frequencies (the resistance mismatch variations are fixed at 20 %)

Also, the relative magnitude variations and the relative phase variations are calculated for different operating frequency values (1, 5 and 10 MHz) when the resistance mismatch variations are fixed at 20 % and are shown in Fig. 11. In Fig. 11, it can be noted that the effect of the operating frequency on the relative magnitude and phase variations is not significant.

4.2 Capacitor mismatch

Similarly, the relative variations of the magnitude and phase are calculated for different values of the capacitance mismatch (i.e., 2, 5, 10, and 20 %) at 1 MHz operating frequency and plotted in Fig. 12.

As shown in Fig. 12, the relative phase variations are higher than the relative magnitude variations and also increasing at a higher rate. Moreover, the relative variations in magnitude and phase due to the capacitance mismatch are smaller than that due to the resistance mismatch by a factor of

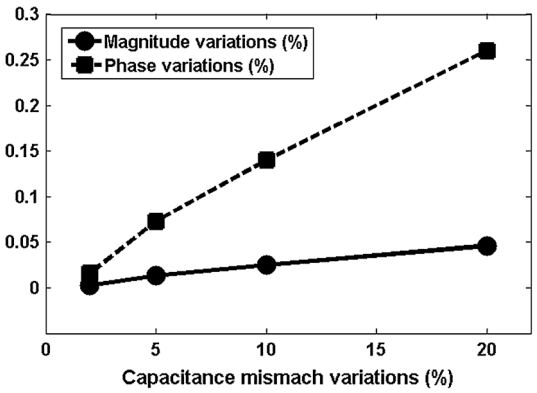

Fig. 12 The relative variations of the magnitude and phase for different capacitance mismatch variations

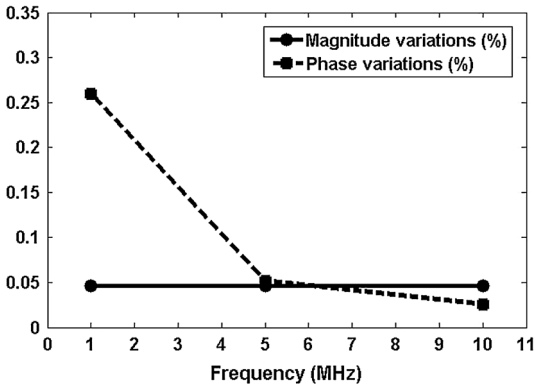

Fig. 13 The relative variations of the magnitude and phase at different frequencies (the capacitance mismatch variations are fixed at 20 %)

10. This shows that the selection of the resistances should be done very carefully as the resistance mismatch has an impact on the proposed circuit performance. However, this impact is still not significant as it is less than 4 % when the resistance mismatch variations are 20 %.

Figure 13 displays the relative magnitude and phase variations for different frequency values at 20 % capacitance mismatch. It is shown that increasing the operating frequency helps in reducing the relative phase variations significantly (i.e., when the frequency changed from 1 to 10 MHz, the relative phase variations dropped by a factor of 5).

5 Experimental and simulation results of the proposed CMBG

To verify the operational characteristics of the proposed CMBG, the circuit of Fig. 9 was simulated using PSPICE version 9.1. The proposed CMBG was also prototyped, tested

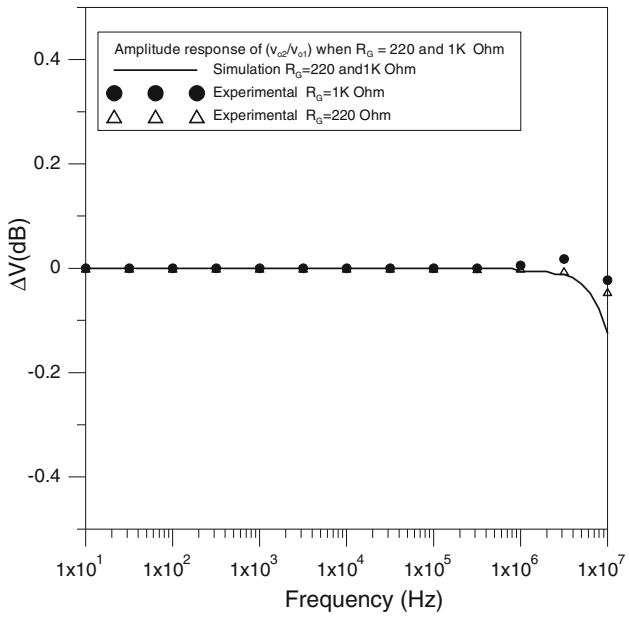

Fig. 14 The amplitude response with R_G = 220 and 1 K Ohm

in the single-ended input mode and the simulation results verified. Each OFCC was constructed using an Analog Devices *AD846AQ* current feedback op amp [15] and current-mirrors composed of Harris transistor array *CA3096CE* [16]. The *AD846AQ* has a bandwidth of 80 MHz at unity gain, and slew rate 450 V/μs. We connected the input voltage to v_{in1} and connected v_{in2} to the ground. Resistors R_{w1} and R_{w2} were set at 1 KΩ, while R_{L1} and R_{L2} were set at 1.5 KΩ and R_G was tested at values of 220Ω and 1 KΩ. All resistors have 1 % tolerance. For these resistors values, the low frequency gains were 6.8 (16.7 dB) and 1.5 (3.5 dB), respectively. The output-signal phase and amplitude differences were measured with respect to frequency. The amplitude error $|\Delta V|$ in dB for the two values of R_G is shown in Fig. 14. This error is 0 dB for R_G = 220 and 1 KΩ for frequencies up to 1 MHz. The phase-difference error $\Delta\Phi$ for the two values of R_G is shown in Fig. 15, the system phase error remained less than about 1 for frequencies up to 1 MHz for $R_G = 1$ kΩ and $R_G = 220$ Ω. This performance up to 1 MHz is superior to the circuit performances in Ref [5–8]. Figures 14 and 15 confirm the independence of both the phase and amplitude responses with changing of R_G. Also, from these figures, we can observe that the experimental results validate the simulated results and the analytical results of Eqs. (40) and (41), except at frequencies approaching the bandwidth of the OFCC. The difference between the experimental and simulation results can be interpreted as a result of tracking errors and the presence of additional stray capacitances at the various nodes in the circuit. The oscilloscope output taken at 1 MHz is shown in Fig. 16 with R_G = 1 KΩ.

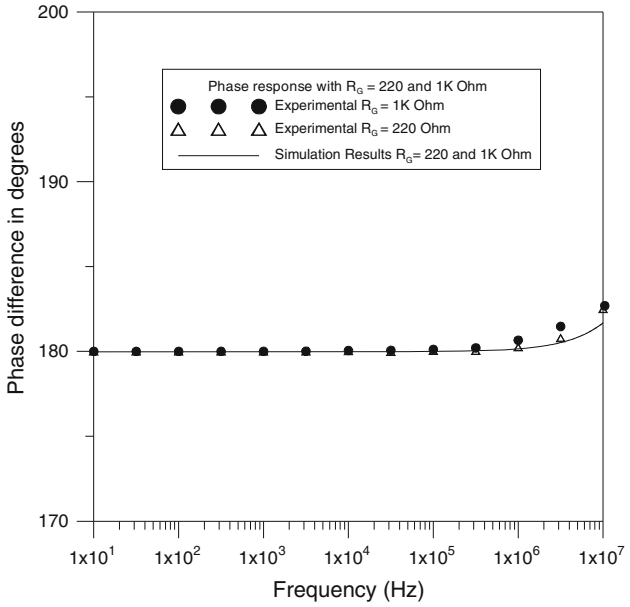

Fig. 15 The phase response with R_G = 220 and 1 K Ohm

6 Discussion

Table 1 shows a performance comparison between the proposed current-mode balanced generator circuits and the other circuitry that used to provide the same functions [5–7]. Balanced generator circuits proposed in Ref. [5, 6] which utilized the operational amplifiers, these circuits require the amplifier-pole matching and gain restrictions. Inversely, the current-mode balanced generator, which uses two CCII+ and two Op-amps, or four CCII+ , Ref. [7, 8], respectively, have better amplitude and phase performance at low frequencies. However at high frequencies, the amplitude and phase errors increase and depend on the gain dependent resistor (R_G), see Eqs. (1) and (2). Also, these topologies use 2 CCII+ in conjunction with 2 op-amps or 4 CCII+, which means more power consumption. The power consumptions and the expected fabrication area of the circuits proposed in Refs. [5–8] are as shown in Table 2 [15–18]. From Table 2, the expected fabrication die area of the proposed circuit is outperforming the circuits provided in Refs [7, 8]. For example, the expected die area of the circuit proposed in Refs [5, 6] is calculated as follows: the die area of a single LF351 Op-Amp is 2.286×2.286 mm^2 = 5.2258 mm^2 [17], there are two Op-amps used to implement the circuit proposed in Refs [5, 6], thus the total expected die area is 2×5.2258 mm^2 = 10.4516 mm^2. The expected die area of the proposed circuit is calculated as follows: The OFCC consists of 1 × AD846 current feedback amplifier and 2 × CA3069 transistor array [15, 16]. The die area of AD846 current feedback amplifier is 2.2×2.64 mm^2 = 5.808 mm^2 [15]. The die area of the CA3096 is 0.74×0.74 mm^2 = 0.5476 mm^2 [1]. Thus, the total die area of a single OFCC is 5.808 + (2 × 0.5476) = 6.9032 mm^2 and the total die area of the proposed CMBG which includes 2 × OFCC is 2 × 6.9032 = 13.8064 mm^2. Similarly, the expected die areas of the circuits proposed in Ref. [7, 8] are calculated and shown in Table 2. The power consumption of the proposed circuit is better than Refs [5–7]. However, Ref [8] shows better power consumption compared to the proposed circuit. On the other hand, the proposed topology uses only two OFCCs. It has a phase and amplitude errors 1 and 0 dB, respectively, up to frequency 1 MHz. This performance up to 1 MHz is superior to the circuit performances of Ref. [7, 8]. The proposed circuit's output phase and amplitude are independent of R_G, see Eqs. (39) and (41). In other words, in the proposed

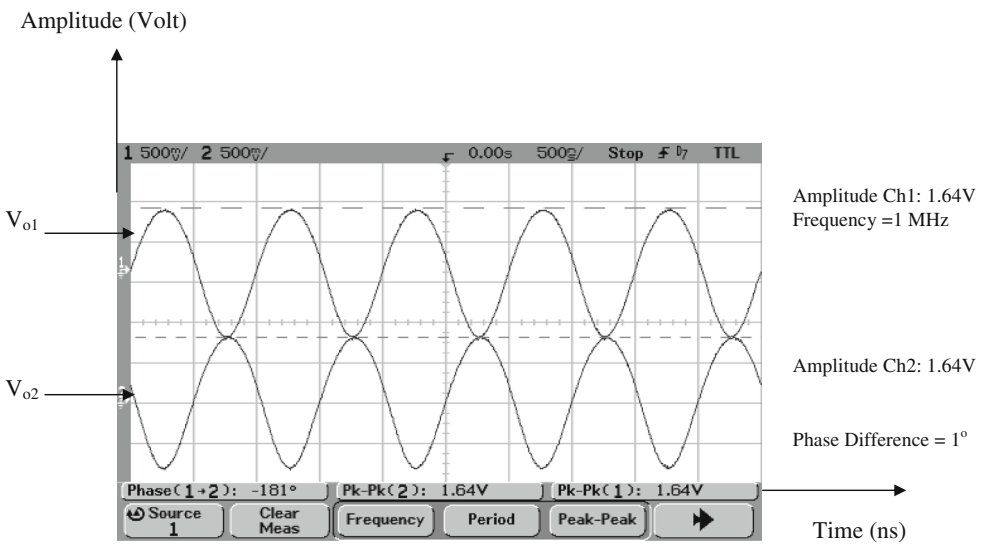

Fig. 16 Sample of the results with R_G = 1 K Ohm and frequency = 1 MHz

Table 1 Comparison between the proposed and other CMBG circuits

Balanced generator reference	Phase error in degrees at frequency = 1 M Hz	Amplitude error in dB at frequency = 1 M Hz	Power consumption (normalized to the proposed circuit)	Expected fabricated area (normalized to the proposed circuit)	Number of building blocks used
[5]	8°	0.08	7.58	0.76	2 Op-Amps
[6]	6°	0.08	7.58	0.76	2 Op-Amps
[7]	3°	0.2	8.06	1.42	2CCII 2 Op-amps
[8]	3°	0.2	0.977	1.32	4CCII
Proposed circuit	1°	0	1	1	2 OFCC

Table 2 Power consumption and expected die area of the proposed and other CMBG circuits

Balanced generator reference	Power consumption (mW)	Expected fabricated area (mm^2)	Number of building blocks used
[5]	1,360	10.4516 [5, 17]	2 Op-Amps
[6]	1,360	10.4516 [6, 17]	2 Op-Amps
[7]	1,447.6	19.5716 [7, 17, 18]	2CCII 2 Op-amps
[8]	175.5	18.24 [8, 18]	4CCII
Proposed circuit	179.5	13.8064 [11, 15, 16]	2 OFCC

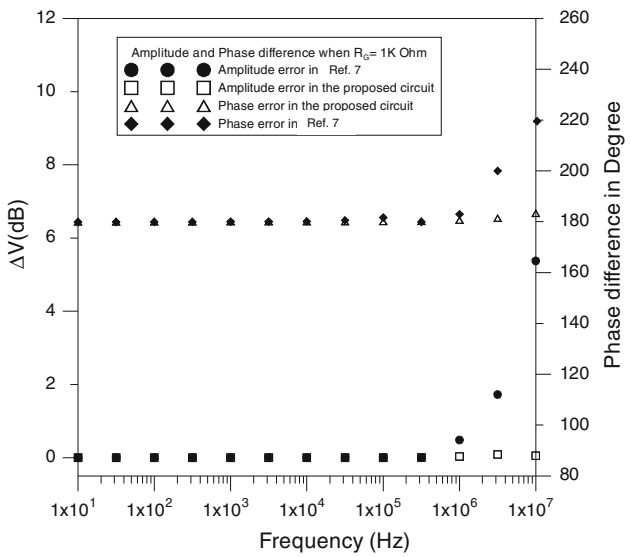

Fig. 17 The amplitude and phase responses of the circuit in Ref. [7] and the proposed circuit when $R_G = 1$ K Ohm

circuit R_G controls only the gain of v_{o1} and v_{o2}, as shown in Eqs. (35) and (36) and it does not control the phase or amplitude difference, as proven in Eqs. (39) and (41). Figure 17 shows the amplitude and phase performance of the proposed circuit and the circuit in Ref. [7], when $R_G = 1$ KΩ. This figure shows that the proposed circuit provides accurate amplitude and phase-matched balanced signals for frequencies up to 1 MHz compared with circuit in Ref. [7]. The power consumption and expected fabrication area of the proposed circuit are 179.5 mW and 13.8064 mm^2, respectively.

7 Conclusion

A new CMBG circuit based on an OFCC has been proposed, simulated and prototyped. The experimental results show that the new CMBG configuration has the following advantages: it produces accurate amplitude-matched balanced signals for frequencies up to 1 MHz without using matched devices. The voltage gain, as well as the bandwidth, of the proposed CMBG is independent of R_x of the current feedback op-amp used and dependent only on the external resistors (i.e., R_G and R_L). The mismatching impacts on the proposed CMBG are presented and discussed. The proposed CMBG is not complicated and offers advantages over and above currently used CMBG. On the other hand, it would be suitable candidate for integration in an IC process. Thus, it can be used in many applications, such as biomedical and lab-on-a-chip.

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References

1. Rzeszewski, T. (1976). A system approach to synchronous detection. *IEEE Transactions On Consumer Electronics, CE-22*(2), 186–193.
2. Nakanishi, M., & Sakamoto, Y. (1996). Analysis of first-order feedback loop with lock-in amplifier. *IEEE Transaction on Circuit and System II, 43*(8), 570–576.
3. Duque-Carrillo, J. F. (1993). Control of the common-mode component in CMOS continuous-time fully differential signal processing. *Analog Integrated Circuit and Signal Processing, 4*, 131–140.

4. Ghallab, Y. H., & Badawy, W. (2010). *Lab-on-a-chip: Techniques, circuits and biomedical applications*. Boston: Artech House Publisher.
5. Golnabi, H., & Ashrafi, A. (1996). Producing 180° out-of-phase signals from a sinusoidal waveform input. *IEEE Transactions on Instrumentation and Measurement, 45*(1), 312–314.
6. Baert, D. H. J. (1999). Circuit for the generation of balanced output signals. *IEEE Transactions on Instrumentation and Measurement, 48*(6), 1108–1110.
7. Gift, S. J. G., & Maundy, B. J. (2006). Balanced-output-signal generator. *IEEE Transactions on Instrumentation and Measurement, 55*(3), 835–838.
8. Abuelma'atti, M. T.(2013) Balanced output signal generator, US Patent 8,368,464 B2.
9. Ghallab, Y. H., Badawy, W., Kaler, K. V. I. S., & Maundy, B. J. (2005). A novel current-mode instrumentation amplifier based on operational floating current conveyor. *IEEE Transaction on Instrumentation and Measurement, 54*(5), 1941–1994.
10. Ghallab, Y. H., & Badawy, W. (2006). A new topology for a current-mode wheatstone bridge. *IEEE Transaction on Circuit and System II, 53*(1), 18–22.
11. Ghallab, Y. H., Badawy, W., Abou El-Ela, M., & El-Said, M. H. (2006). The operational floating current conveyor and its applications. *Journal of Circuits, Systems and Computers, 15*(3), 352–371.
12. Ghallab, Y. H. & Badawy, W. (2006). *A New Design of the Current-mode Wheatstone Bridge Using Operational Floating Current Conveyor, International Conference on MEMS, NANO, and Smart Systems* 2006 *(ICMENS 2006)*, Dec. 27–29th (pp. 41–44) Cairo, Egypt.
13. Ghallab,Y. H., Badawy, W. & Kaler, K. V.I.S. (2003). *A novel differential ISFET current mode read–out circuit using operational floating current conveyor, ICMENS* 2003(pp. 255–258). Banff, Alberta, Canada.
14. Soclof, S. (1991). Design and applications of analog integrated circuits, Chap.9 (pp. 443–460). New York: Prentice Hall Inc.
15. Analog Devices Manual "450 V/μs, precision, current-feedback OpAmp (AD846)" (pp. 2-307–2-317).
16. Harris semiconductor "CA3096, CA3096A, CA3096C, NPN transistor arrays" File Number 595.4, December 1997.
17. National Semiconductor LF351 Wide Bandwidth JFET Input Operational Amplifier Data Sheet.
18. Analog Devices Manual " 60 MHz 2000 V/μs, monolithic Op Amp (AD844)".

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