

# A low power multiple output switch-mode power supply with wide input range

Indrit Myderrizi · Emre Ozbey

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**Abstract** In this paper, a wide input range multiple output flyback switch-mode power supply (SMPS) with its design aspects is presented. The implemented SMPS is intended to be used in various applications in industry requiring low power and operating under wide input voltage fluctuations. The SMPS is designed using TOPSwitch off-line switched integrated circuit and includes line protection, input filter, rectifier, switching control, output rectification and feedback circuitries. A 5 Watt prototype has been manufactured and is validated through measurements. Experimental results obtained from evaluation tests demonstrate distinct features like wide input range, multiple regulated output voltages, isolation and high efficiency. Technology challenges for the full integration of the presented SMPS are briefly discussed.

**Keywords** Switch-mode power supply (SMPS) · Flyback converter · Voltage regulation · Isolated output · Transformer · Snubber circuit

## 1 Introduction

The switch-mode power supplies (SMPSs) are widely used in various applications in industry. They have distinct advantages over linear power supplies such as higher power efficiency, more compact size, better output voltage

regulation, lower cost, etc. Design of high efficiency SMPSs plays an important role in power management providing an effective source of power for most of electronic systems. SMPSs are designed in two different topologies with respect to application's function that are non-isolated and isolated topologies. In applications which are safe and have low input voltages, use of isolation between input and output is not required. However, in unsafe applications where the input voltage is higher than 60 V, switching operation is realized by using a transformer for isolation between input and output sections. In low power electronics, various transformer isolated converters are widely used. The two fundamental topologies are flyback and forward converters [1].

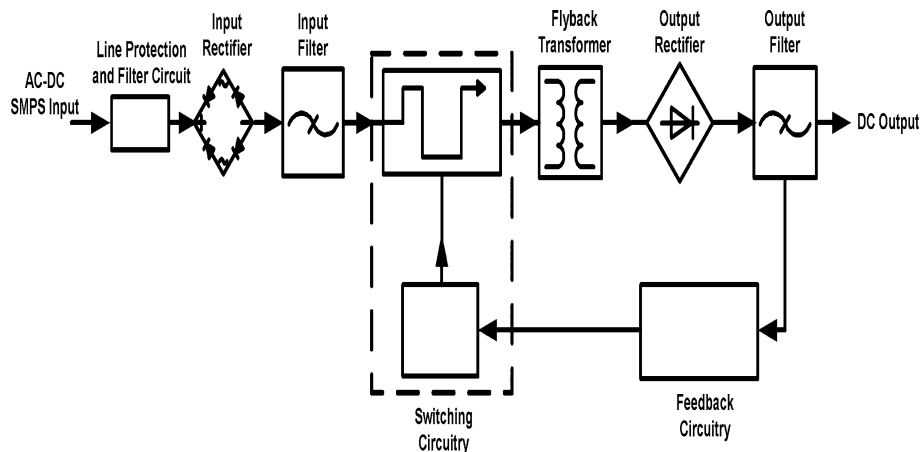
Generally, most of the SMPSs which are produced by reputable manufacturers from all around the world have 85–265 V AC–DC input range. However, there is a need for ultra-wide input range in several applications and in places where unpredictable and large AC mains voltage fluctuations occurs [2]. Many topologies have been presented recently with the aim of supplying different applications operating with specific input voltage ranges and power ratings. A high power two-stage isolated SMPS with high efficiency consisting of an interleaved boost designed for a 220 V AC input voltage and a full-bridge converter designed for a 400 V DC input voltage is proposed in [3]. A boost converter based SMPS with AC mains voltage between 100 and 230 V designed for medical applications is analyzed in [4]. A flyback converter adopting an isolated output-feedback scheme with DC–DC stage supplied by 120–380 V DC input is fabricated in [5]. Several research papers introduce integrated SMPSs to improve power density and reliability at low voltages, such as integrated dual active bridge (DAB) converter designed for 3 V input in [6], integrated DC–DC boost converter in [7], and

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I. Myderrizi (✉) · E. Ozbey  
Department of Electronics and Communications Engineering,  
Dogus University, Acibadem Campus E-Blok, Zeamet Sok. 21,  
Kadikoy, 34722 Istanbul, Turkey  
e-mail: imyderrizi@dogus.edu.tr

E. Ozbey  
e-mail: emreozbey@gmail.com

**Fig. 1** Typical block diagram of an isolated flyback SMPS



100 MHz buck converter integrated with a high power amplifier (HPA) optimized for operation at input voltages of 17 V and 20 V in [8]. In [2] considering some practical design aspects for switch-mode transformer, a flyback topology SMPS expected to operate with AC input voltages swinging between 90 and 264 V, is developed. Using commercially available integrated monolithic ICs, SMPS circuits containing flyback type converters and operated at 85–265 V AC input voltages are designed [9, 10].

Apart from wide input range, a multiple output SMPS is required to supply various electronic devices where diverse isolated and regulated outputs are needed. Multiple output SMPSs supplying the most common output voltages useful in appliances such as personal computers and medical devices can be found in [4, 9] and [11].

In this paper, a low power SMPS based on TOPSwitch power management IC available from Power Integrations Inc. [12, 13] is presented. The objective of this SMPS is to supply different applications with regulated/unregulated multiple output voltages under a wide AC–DC voltage input range.

The paper is organized as follows. Sect. 2 describes typical architecture of an isolated flyback SMPS. Sect. 3 presents design considerations and discrete devices implementation of the SMPS. Some discussions on the potential full integration of the presented SMPS are addressed in Sect. 4. Experimental results obtained through measurements are summarized in Sect. 5, and finally, conclusions are drawn in Sect. 6.

## 2 Isolated flyback SMPS

A SMPS is a device that converts the output taken from an AC power line to a steady DC output or regulated/unregulated multiple outputs. The AC voltage is rectified to provide a pulsating DC signal, and then is filtered to produce a smooth voltage free from ripples. Ultimately, the voltage is regulated to generate a constant output flat

voltage albeit variations in the AC line voltage or fluctuations occurring on account of circuit loading.

A typical block diagram of an isolated flyback SMPS is shown in Fig. 1. It consists of a line protection and filter circuit, an input rectification and filtering block, a transformer, an output rectification and filtering block, and a feedback circuitry connected to a switching block. In line protection and filter circuit block, the line protection is used to block the effects caused by very high current levels or hazardous input voltages, while the filter circuit also known as electromagnetic interference (EMI) filter [5, 14] is used to attenuate conducted differential or common-mode EMI noise. Input/output rectification and filtering blocks are used to convert AC input signals to DC output signals. The output voltage regulation is achieved by a feedback control circuit, which controls the duty cycle of the switch, to keep the output voltage at a constant value.

## 3 Design considerations and discrete devices implementation

The circuit schematic of the designed multiple output SMPS based on the typical block diagram of isolated flyback converter is shown in Fig. 2. Off-line SMPS providing regulated and unregulated output voltage is optimized for low power applications such as digital cameras, power adaptors, battery chargers, communication converters, analyzers, electricity meters, etc. An overview of the specifications of the designed SMPS is given in Table 1. Multiple output feature is realized by modifying secondary side of the flyback transformer.

### 3.1 Transformer design

The primary winding turns  $N_p$  is best calculated using a volt–second approach. From Faraday’s law, the voltage across the primary winding terminals can be written as

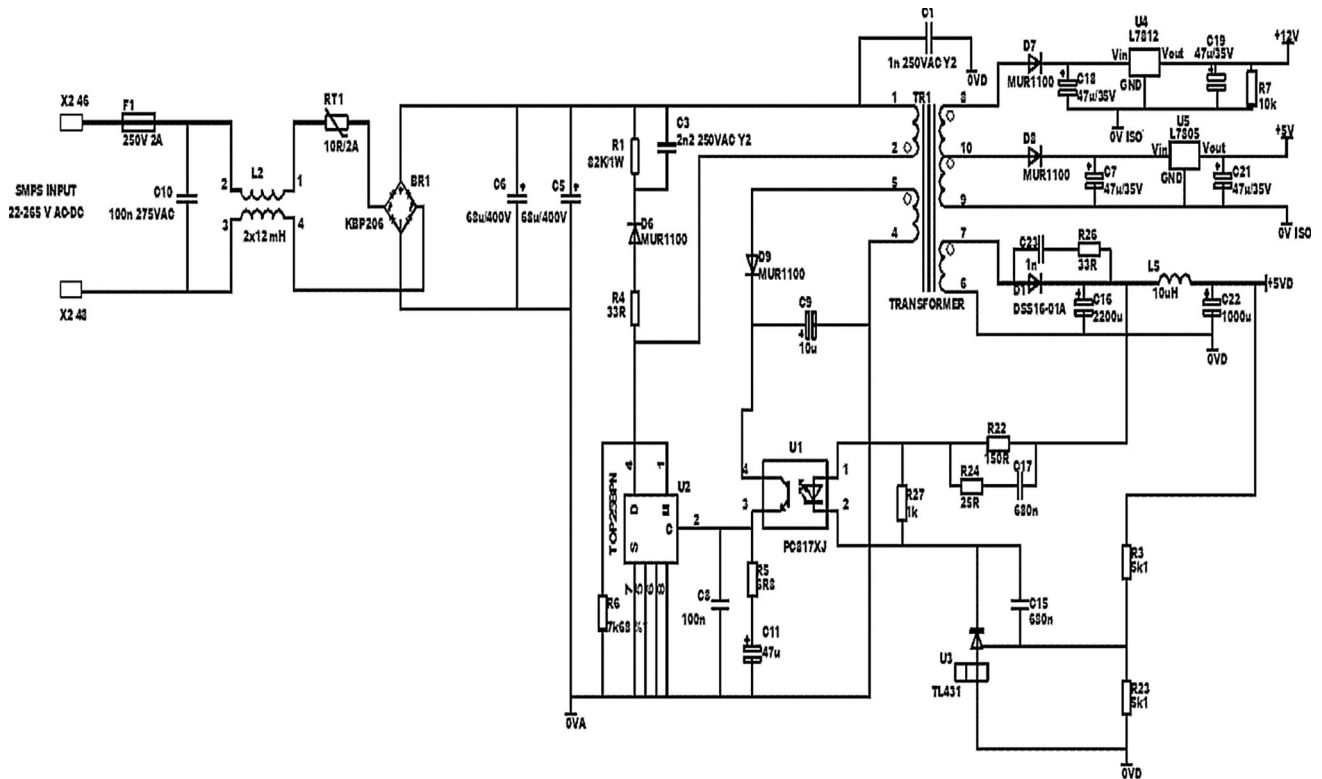


Fig. 2 Circuit schematic of the designed multiple output SMPS

Table 1 Design specifications for SMPS

Symbol	Parameter	Value	Units
$V_i$	AC/DC input voltage	22–265	V
$V_o$	DC regulated output voltage	5	V
	DC regulated output voltage	5	
	DC regulated output voltage	12	
	DC unregulated output voltage	9	
	DC unregulated output voltage	18	
$P_o$	Output power	5	W
$F$	Switching frequency	30–66	KHz

$$v_p = N_p \cdot \frac{d\Phi_p}{dt} \tag{1}$$

where  $\Phi$  is magnetic flux that maximum value can be expressed as the product of maximum flux density in the core  $B_m$  and cross-sectional area of the core  $A$  i.e.  $\Phi_m = B_m \times A$ .

Practically, considering the design specs and information from the transformer core material datasheet, for a desired input voltage range and operating frequency, the number of turns for the primary side can be calculated as

$$N_p = \frac{v_{i(\min)} \cdot [T \cdot (1 - D)]}{B_m \cdot A} \tag{2}$$

where  $T = 1/f$  is the period of the switching signal related to the switching block,  $D$  is the duty cycle, and  $v_{i(\min)}$  is the minimum input voltage.

Once the turns of the primary side are determined for the switch-mode transformer, the turns of the secondary sides are to be determined using input and output power calculations. The input power  $P_{in}$  is

$$P_{in} = \frac{\frac{1}{2} L_p I_p^2}{T} = \frac{(V_i \cdot t_{on})^2}{2TL_p} \tag{3}$$

where  $I_p$  and  $L_p$  are primary current and inductance, respectively.  $V_i$  is input voltage and  $t_{on}$  is on time of one complete switching cycle. Note that  $V_i$  is DC voltage obtained after input rectification and filtering block. Output power may be written as  $P_o = \eta P_{in}$ , where  $\eta$  is the efficiency of the transformer.

All significant design specs (input/output voltages and powers) and transformer design parameters (transformer’s primary and secondary turns) can be arranged to obtain the ratio of  $t_{on}$  on time and  $t_{off}$  off time as [2],

$$\frac{t_{on}}{t_{off}} = \frac{N_p}{N_s} \cdot \frac{V_o}{V_i} \cdot \sqrt{\frac{P_{in}}{P_o}} \tag{4}$$

The transformer primary turns are determined by substituting  $v_{i(\min)} = 22$  V, duty cycle  $D = 0.5$ ,

switching's signal period, and temperature dependent material parameters  $B_m = 125$  mT for Siemens N27 and  $A_e = 52.5$  mm<sup>2</sup> for E25/13/7 core [15] into (2). The value of primary turns is selected as  $N_p = 54$ . The turns for the multiple secondary windings are selected as  $N_{s1} = 16 + 16$  and  $N_{s2} = 9$  for the low power output secondary and high output secondary, respectively.

### 3.2 Input block

Input block consists of protection fuse  $F_1$ , EMI filter (filtering capacitor  $C_{10}$  and common mode choke  $L_2$ ), negative temperature coefficient (NTC) resistor  $RT_1$ , full wave bridge rectifier  $BR_1$ , and bulk storage capacitors  $C_5$ ,  $C_6$ .

Filtering capacitor  $C_{10}$  is used to filter undesired high frequency signals from input to output or vice versa. At high frequency levels the impedance of this capacitor is very small and can be calculated as

$$X_{C10} = \frac{1}{2\pi f_{sw} \cdot C_{10}} \quad (5)$$

where  $f_{sw}$  is switching frequency and is in the order of several 10 kHzs. Note that at 50/60 Hz the impedance value of  $C_{10}$  is very high.

The purpose of NTC resistor  $RT_1$  is blocking inrush current. Initially,  $RT_1$  has a high resistance, and then resistance value decreases after warming up.

Bulk storage capacitors  $C_5$  and  $C_6$  are used to increase the quality of the DC signal achieved from rectifier  $BR_1$  and ensure low ripple DC input to the flyback converter stage [12, 13].

$$C_{bulk} \geq \frac{P_o}{2\pi f \cdot V_{ripple} \cdot V_{i(min)}} \quad (6)$$

where  $f$  is mains frequency,  $V_{ripple}$  is peak-to-peak ripple voltage and  $V_{i(min)}$  is the rms value of the minimum input voltage.

The voltage rating and rated current of the protection fuse  $F_1$  are selected as 300 VAC/VDC and 2 A.  $C_{10}$  filter capacitor is selected as 100 nF 275 VAC to exhibit low impedance at switching frequency and high impedance at mains frequency. Common mode choke filter is selected as  $2 \times 10$  mH. As in protection fuse the current limit is determined as 2 A. A standard KBP206 with 50–1,000 V voltage range and 2 A maximum forward current silicone bridge rectifier is used for implementation of  $BR_1$ .  $RT_1$  value is determined as 10  $\Omega/2$  A. A value of 136  $\mu$ F is selected for the bulk capacitor. Since this capacitor physically is a huge one, two equal capacitors in parallel  $C_5$  and  $C_6$  with value 68  $\mu$ F 400 V each are used in implementation. Last high frequency signal filter capacitor  $C_1$  at primary side is selected as 1 nF 275 VAC.

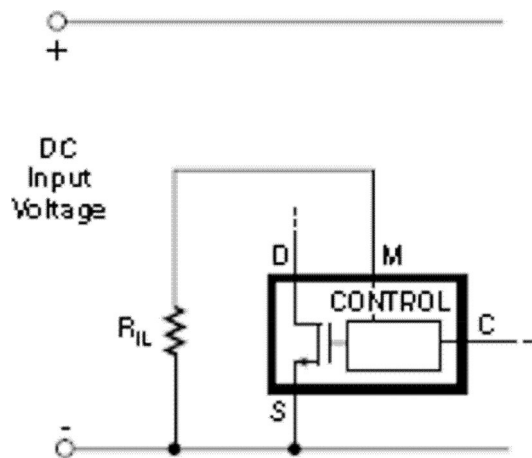


Fig. 3 TOP258PN with externally set current limit [13]

### 3.3 Feedback and switching block

The feedback circuit's selection adopted in this design relies on controlling the output voltage using a programmable shunt regulator reference IC in series with an optocoupler's diode. Programmable shunt regulator is used to set the output voltage and is programmed via voltage divider consisting of  $R_3$  and  $R_{23}$  resistors. Resistors  $R_{27}$  and  $R_{22}$  set the minimum operating current and DC gain for the regulator, respectively. AC feedback is provided directly through an optocoupler with good transfer efficiency. Additionally, RC circuit consisting of  $R_{24}$  and  $C_{17}$  is used to further improve control loop bandwidth by providing additional phase boost [12].

The switching block comprises TOPSwitch monolithic device offered by Power Integrations Inc.. The device incorporates a power MOSFET, high voltage switched current source, pulse-width modulation (PWM) control, oscillator, thermal shutdown circuit, fault protection and some other control circuitry [13]. The selected product part for the design, TOP258PN is a four pin configuration package and in this application is configured as shown in Fig. 3.

A conventional RCD snubber clamp network consisting of diode  $D_6$  and capacitor  $C_3$ , together with resistors  $R_1$  and  $R_4$  is used to dissipate energy stored in primary leakage inductance of the transformer and to filter high frequency unwanted signals occurring because of the switching action.

In case to provide maximum output current, external current limit resistor  $R_6$  is selected as 7.68 k $\Omega$  [13]. Components of the primary clamp block are selected as; diode protection resistor  $R_4 = 33$   $\Omega$ , discharging resistor  $R_1 = 82$  k $\Omega$ , and capacitor  $C_3 = 2.2$  nF 250 VAC.

Output feedback circuitry employs a TL 431 programmable shunt regulator biased by  $R_{27} = 1 \text{ k}\Omega$  with a bias current of approximately 0.5 mA. Other components completing the feedback loop are selected as  $R_3 = R_{23} = 5.1 \text{ k}\Omega$ ,  $R_{22} = 150 \text{ }\Omega$ ,  $R_{24} = 25 \text{ }\Omega$ , and  $C_{15} = C_{17} = 680 \text{ nF}$ .

### 3.4 Output block

Output block consists of three different voltage/power output rectification and regulation stages. Multiple secondary windings configuration is preferred to obtain electrical isolation between low and high power output circuits. The high power output secondary is rectified and filtered by  $D_1$  and  $C_{16}$ . Inductor  $L_5$  and capacitor  $C_{22}$  provide noise filtering. Capacitor  $C_{23}$  and resistor  $R_{26}$  are used to protect diode from high frequency signals and overheating.  $C_{16}$  is used to increase the quality of DC signal achieved from rectification and is selected dependent on the output line voltage and power levels, as shown below

$$C_{16} \geq \frac{P_{o1}}{2\pi f_{sw} \cdot V_{ripple} \cdot V_{o1}} \tag{7}$$

Filter inductor  $L_5$  is selected to exhibit an impedance value  $X_L$ , very small at AC and negligible at DC, calculated as

$$X_{L5} = 2\pi f_{sw} \cdot L_5 \tag{8}$$

The low power output secondary is realized using two windings connected in series to provide two different output voltages. The lower voltage output including only one winding and the higher voltage output including both windings are rectified and filtered by  $D_3$  and  $C_7$ , and  $D_7$  and  $C_{18}$ , respectively. Additionally, the outputs of these stages are supplemented with fixed positive linear voltage regulator ICs to obtain regulated outputs at desired voltage levels.  $C_{19}$  and  $C_{21}$  capacitors connected to the outputs of the regulator ICs are used to filter the high frequency noise that may appear at the output.  $R_7$  resistor is used to discharge capacitor  $C_{19}$  capacitor when the output is not used.

Although not mandatory, 5 V/4 W isolated output comprises a DSS16-01A Schottky diode to withstand the power level which is higher in this output compared to other outputs.  $C_{23}$  and  $R_{26}$  that protect the diode from high frequency signals and overheating are selected as 1 nF 100 V and 33  $\Omega$ , respectively. The minimum values of filter capacitors for an output power of 5 W are selected as  $C_{16} = 2,200 \text{ }\mu\text{F}$  10 V and  $C_{22} = 1,000 \text{ }\mu\text{F}$  10 V. Considering a very low value for the impedance in (8) the inductance value of  $L_5$  is selected equal to 10  $\mu\text{H}$ . 12 V/0.4 W and 5 V/0.4 W isolated outputs comprise standard MUR1100 diodes prominent for their high switching speed and low equivalent series resistance (ESR). The minimum

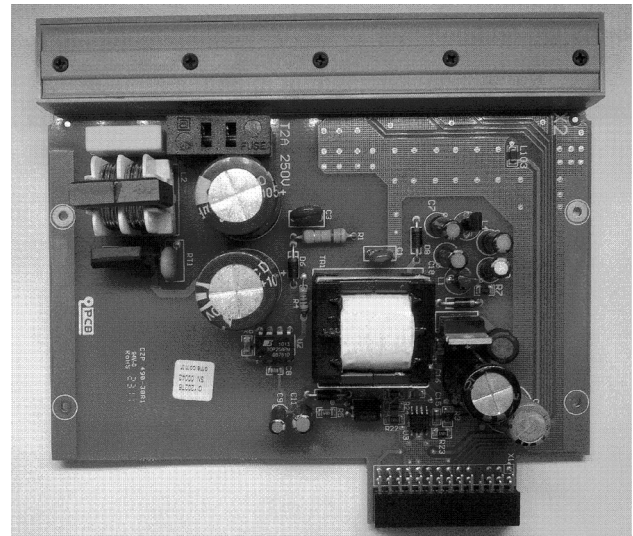


Fig. 4 Assembled PCB of the SMPS

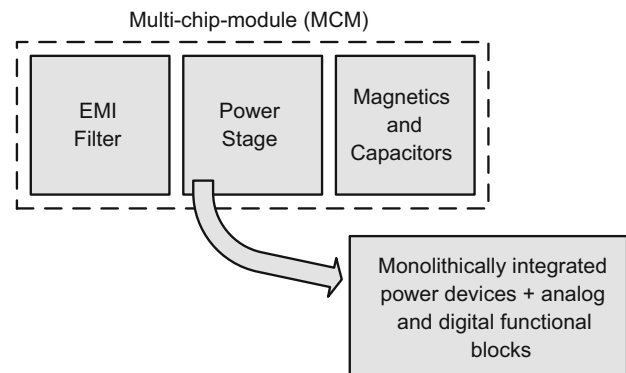


Fig. 5 Block diagram of a fully integrated SMPS

values of  $C_7$ ,  $C_{21}$ ,  $C_{18}$  and  $C_{19}$  filter capacitors for an output power of 1 W are selected as 47  $\mu\text{F}$  35 V. Discharging resistor  $R_7$  used at 12 V output stage is determined as 10 k $\Omega$ .

The implemented PCB, designed to provide high isolation between the primary and secondary sides of the transformer, is shown in Fig. 4.

## 4 Full integration issues

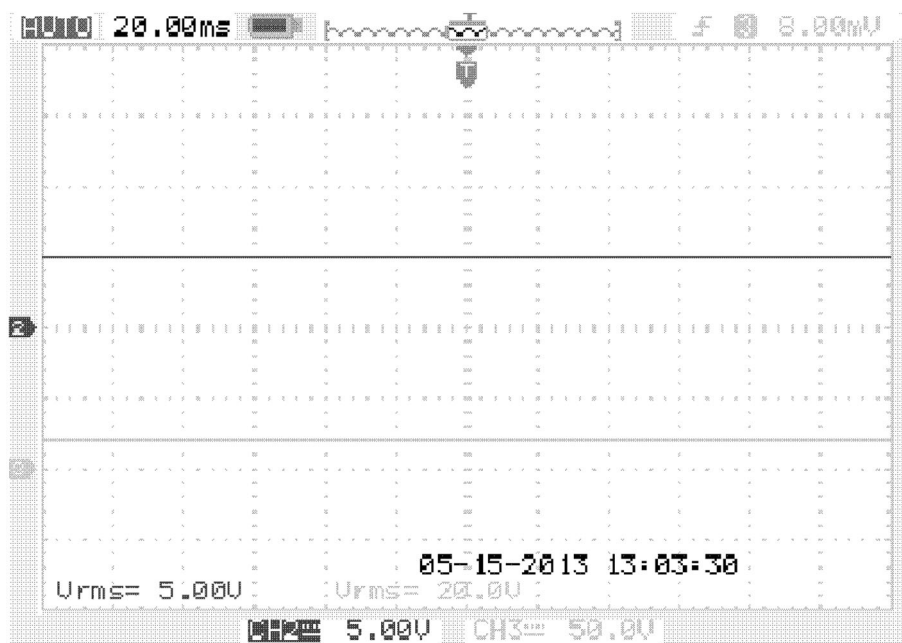
Full integration of SMPS systems requires further advances in technologies including power semiconductor processing, inductor fabrication process, transformer winding, capacitor and resistor manufacturing processes. Present manufacturing processes of the different types of discrete

components and their packaging as used in power electronics are not compatible with integration into one production line. Compatible processes that can be incorporated into one integrated production line are needed [16].

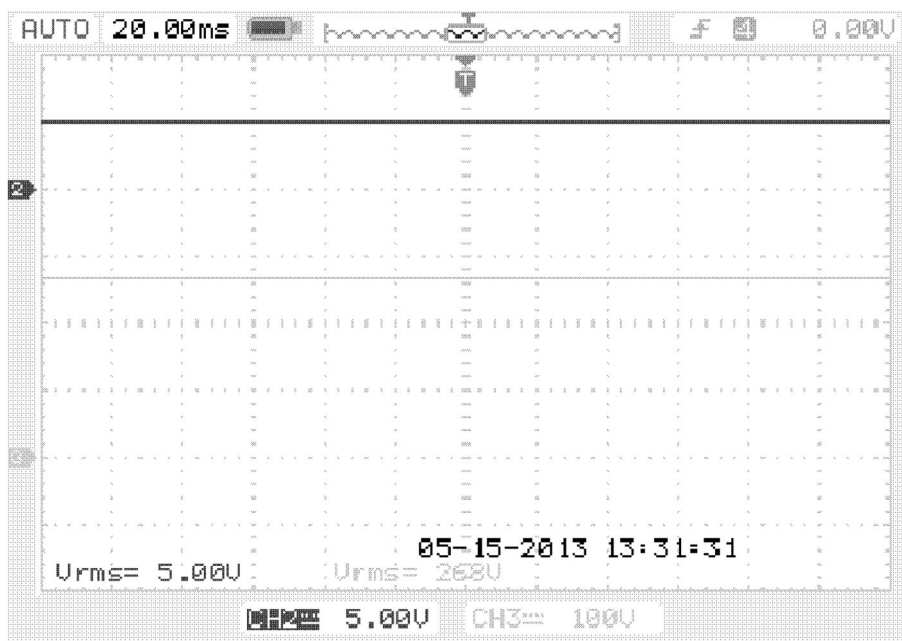
Several CMOS process technologies for power supply ICs, enabling the cost-effective integration of the high-voltage n-channel transistors with industry standard CMOS and bipolar components on the same monolithic IC, have

been developed by different manufacturers [13, 17]. For low-power applications, the trend is to focus on the CMOS implementation of low-power converters such that power management solutions and mixed-signal circuitries can be fabricated on the same chip [18]. Power density and efficiency requirements have led to different packaging integration levels strictly related to applied power levels of power supply systems. At higher power levels package-on-

**Fig. 6** 5 V/4 W output a 20 V DC input b 268 V DC input

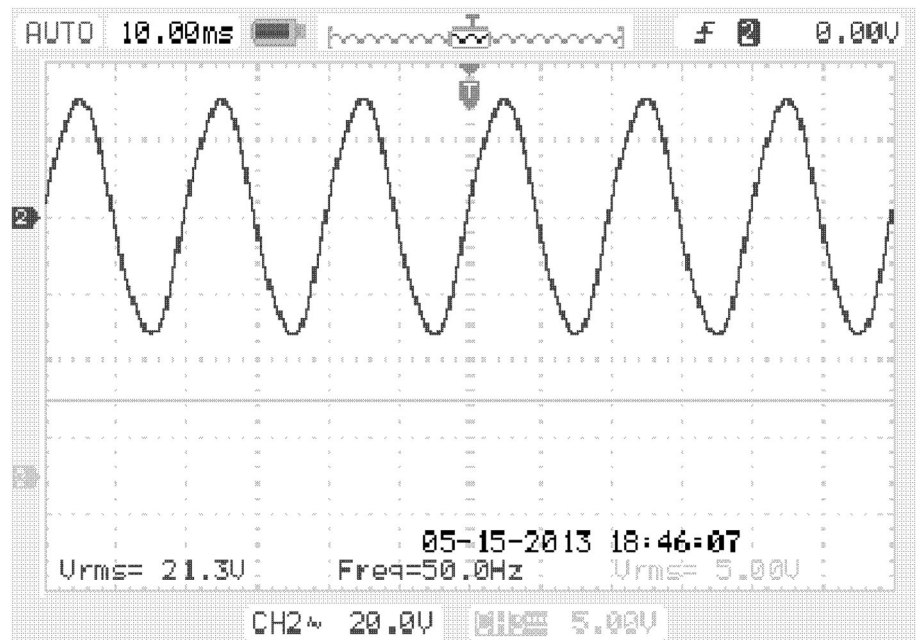


(a)

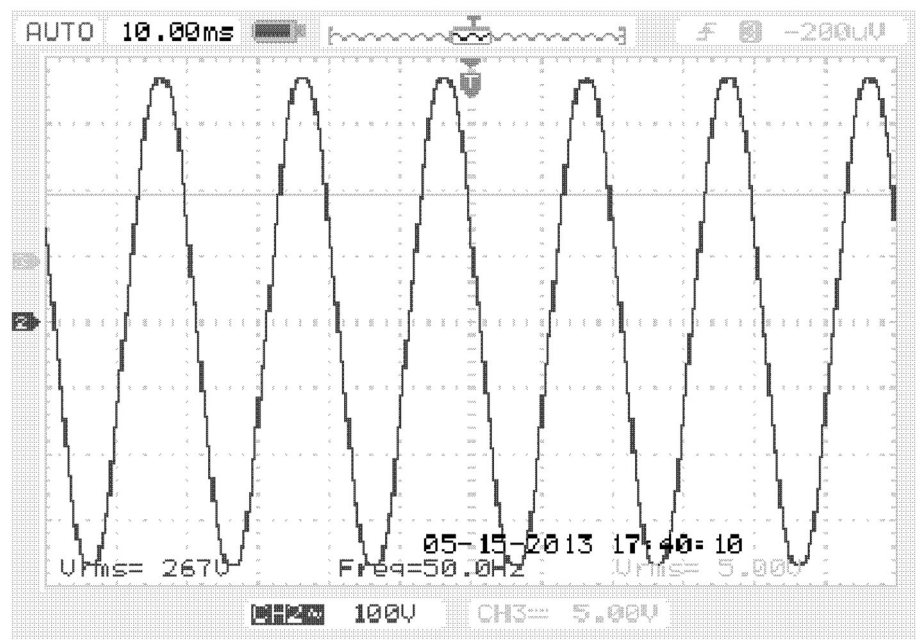


(b)

**Fig. 7** 5 V/4 W output  
**a** 21.3 V AC input **b** 267 V AC input



(a)

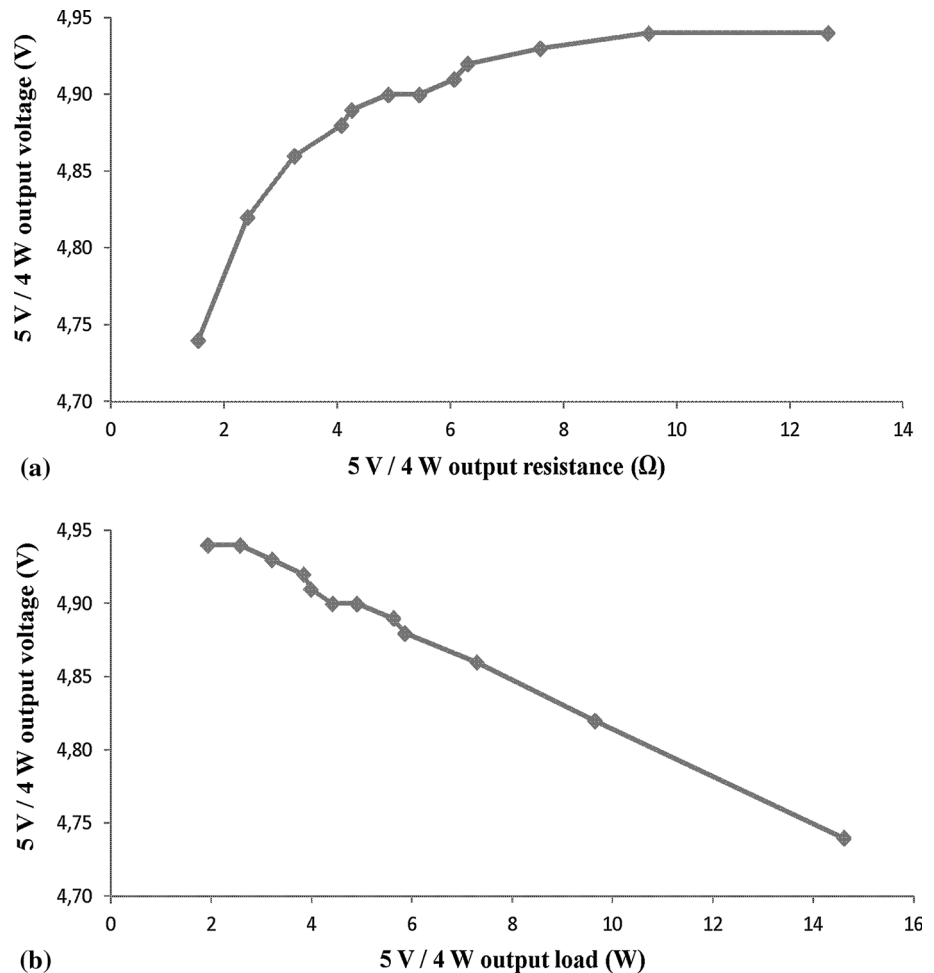


(b)

package approach is used, while at low and intermediate power levels monolithic integration and multi-chip-module (MCM) packaging techniques are employed [19]. Monolithic integration incorporates power devices, digital and analog functional blocks (drivers, control circuits, etc.) on a single chip [5, 8, 13, 17, 18]. It must be noted that power devices manufactured using CMOS compatible processes like SiC and GaN power device technologies can also be monolithically integrated [19, 20]. MCM packaging

technique incorporates highly integrated power electronics modules (IPEMs) that can be categorized in three main groups: active switching stage, electromagnetic interference (EMI) filter, and electromagnetic power passives [16]. Active switching stage comprises monolithic chip mentioned above i.e. power devices, DC–DC stages, control circuitry, etc. EMI filter and power passives stages comprise electromagnetic passive components including transformers, inductors, bulk and DC blocking capacitors.

**Fig. 8** 5 V/4 W output voltage versus **a** output resistance **b** load



Conventionally, these stages are implemented by using discrete components that account for a critical increase in the physical size of the system. However, raising the frequency of the system in the levels that can still be handled by the power stage and applying advanced technologies like planar passive integration technology and planar integrated magnetic technology power density and form factor of the system can be improved [6, 16, 21]. Replacement of all discrete active and passive devices with integrated modules results in a hybrid fully integrated MCM.

Similarly, the SMPS shown in Figs. 1 and 2 can be realized as a fully integrated MCM as shown in Fig. 5. Three integrated modules are required: EMI filter module comprising common mode choke filter; power stage module comprising power devices, rectifiers, shunt regulators, PWM control digital and analog circuitry; magnetic and capacitors module comprising flyback transformer, bulk and filtering capacitors.

Obviously, fully integrated MCM SMPS satisfies major requirements of today's power management solutions including less space and less power consumption,

high efficiency and high reliability, and wide input voltage.

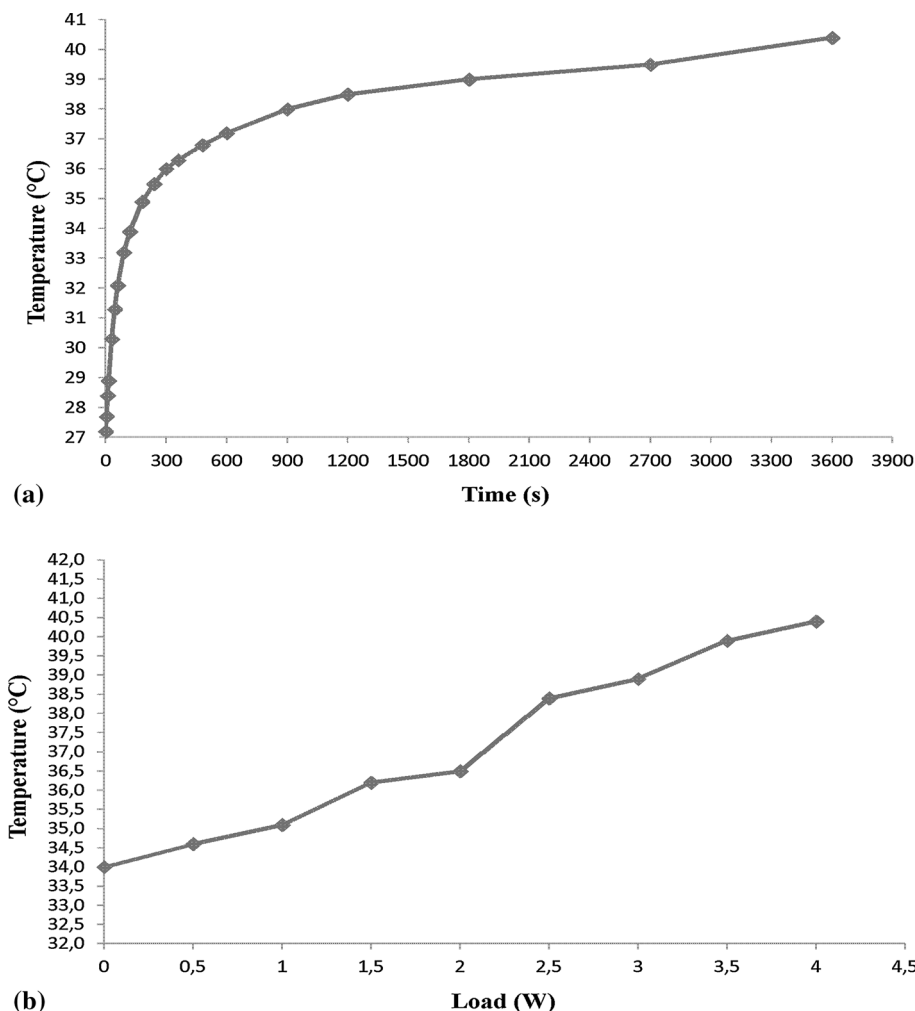
## 5 Experimental results

Functionality and characterization of the designed SMPS is obtained by performing various experimental measurements on the assembled PCB shown in the Fig. 4. Measurements are performed for all regulated and unregulated outputs under wide DC/AC input voltage range and different load values. Figure 6 presenting input (channel 3: CH3) and output (channel 2: CH2) voltage waveforms versus time, illustrates the workability limits for the 5 V/4 W isolated output of SMPS excited with different DC input voltage signals. Similarly, Fig. 7 presenting input (channel 2: CH2) and output (channel 3: CH3) voltage waveforms versus time, illustrates the workability limits of the same output excited with different AC input voltage signals.

It must be noted that the measurement tests are obtained with the output fully loaded i.e. under full 4 W load



**Fig. 9** Temperature measurements **a** time-dependent **b** load-dependent



condition. Similar results are acquired from the measurements performed for other regulated outputs i.e. 5 V/0.4 W and 12 V/0.4 W outputs. From Figs. 6 and 7 it can be seen that for efficient operation the DC and AC input voltage ranges are 20–268 V and 21.3–267 V, respectively. Obviously, the designed SMPS satisfies 22–265 V wide input range design specification.

The performance of the designed SMPS is also tested for output open/short circuit behavior and the dependency on the output load. In Fig. 8(a) variation of the 5 V/4 W output’s voltage with output resistance excited with 100 V AC input voltage, is shown. When output is open circuited the output voltage remains constant with a 0.6 % error at 4.97 V. When output resistance decreases toward short circuited state the output voltage drops significantly, for example when  $R_o = 1.5 \Omega$  output voltage drops at 4.74 V introducing a 5.2 % error. The variation of output voltage with output load denoted in watts is shown in Fig. 8(b). As expected, when the output load exceeds the limit of the prescribed power for the given output, the voltage starts decreasing.

Some basic temperature measurements are realized to observe normal operating range and load effect on the designed SMPS. For SMPSs the main source of temperature variations are determined by the environment temperature and power dissipation of the components of the device. Figure 9(a) shows time-dependent temperature measurement of the maximum loaded device excited with 100 V DC input signal. Figure 9(b) shows the load-dependent temperature measurement of the device excited by the same input for different loads within the maximum power limit, each remaining connected for 1 h. Duly, increase of the load i.e. decrease of the SMPS’s output resistance, causes the current flowing through the components to increase. As a result, power dissipation is increased causing the temperature to rise up.

Measurements performed for 9 V/0.4 W (positive terminal of  $C_7$ ) and 18 V/0.4 W (positive terminal of  $C_{18}$ ) show that unregulated output voltages are not stable and are directly dependent on the current drawn by load at 5 V/4 W output. For the 5 V/4 W output loaded from 0 up to

6 W, unregulated output voltages vary in range from 8.37 to 11.12 V and from 17.75 to 24.88 V, respectively. However, unregulated voltage outputs are useful to obtain regulated outputs different from available outputs by supplementing the existing SMPS externally with voltage regulator ICs. For example to achieve 3.3 V/0.4 W and 15 V/0.4 W regulated output voltages that are essential in several low power applications, linear voltage regulator ICs (fixed or adjustable) with output voltages of 3.3 and 15 V can be connected to the unregulated 9 and 18 V outputs, respectively.

A nominal efficiency of 84 % at maximum load is achieved from the designed TOP258PN-based SMPS. Manufactured prototype has a PCB size of  $5.3 \times 4.9$  inches. The prototype was designed and optimized for high performance without paying attention to PCB size.

## 6 Conclusion

The implementation of a multiple output switched mode power supply is reported and detailed design is provided to satisfy specifications. Features such as ultra-wide AC/DC input voltage range, high efficiency, and high-frequency isolation are achieved. The elementary benefit of this TOP258PN-based SMPS unit is that it regulates switching frequency according to the load changes. By doing this, the SMPS unit keeps its efficiency maximum under all operation conditions. Consequently, it can operate under maximum load condition without using any heat sink.

The performance of the realized prototype SMPS is evaluated through experimental measurements. The results obtained show that the implemented SMPS has many advantages over the existing implementations, i.e. ultra-wide input range, high operating efficiency, and multiple regulated/unregulated outputs necessary for low power applications available in industry such as analyzers, GPRS modems, communication converters, electricity meters, etc.

Also, potential full integration issues that can improve the efficiency and power density of the presented SMPS are briefly considered.

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**Indrit Myderrizi** received the B.Sc., M.Sc. and Ph.D. degrees in electronics and communications engineering from Istanbul Technical University (ITU) in 1999, 2002 and 2009, respectively. He joined the Department of Electronics and Communications Engineering at Dogus University, Istanbul in 2005, where he is currently an Assistant Professor. His research interests include data converters, analog and digital IC design, low power industrial

electronics and RF microelectronics. Dr. Myderrizi is a Member of IEEE Industrial Electronics and Circuit and Systems societies. He is author/co-author of several papers in international journals and conference proceedings.



**Emre Ozbey** was born in Istanbul, Turkey, in 1989. He received the B.S. degree in electronics and communications engineering from the Dogus University, Istanbul, in 2013. He is currently pursuing the M.Sc. degree in management information systems and engineering in the Institute for Graduate Studies in Pure and Applied Sciences, Marmara University. His research interests include PLC systems and relay test equipment.