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# Optimal *LC*-VCO design through evolutionary algorithms

**P. Pereira · M. Helena Fino · M. Ventim-Neves**

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**Abstract** The need for implementing low cost, fully integrated RF wireless transceivers has motivated the widespread use CMOS technology. However, in the particular case for voltage-controlled oscillators (VCO) where ever more stringent specifications in terms of phase-noise must be attained, the design of the on-chip *LC* tank is a challenging task, where fully advantage of the actual technologies characteristics must be pushed to nearly its limits. To overcome phase-noise limitations arising from the low quality factor of integrated inductors, optimization design methodologies are usually used. In this paper a model-based optimization approach is proposed. In this work the characterization of the oscillator behaviour is guaranteed by a set of analytical models describing each circuit element performance. A set of working examples for UMC130 technology, aiming the minimization of both VCO phase noise and power consumption, is addressed. The results presented, illustrate the potential of a GA optimization procedure design methodology yielding accurate and timely efficient oscillator designs. The validity of the results is checked against HSPICE/RF simulations.

**Keywords** *LC*-VCO · Design methodology · Discrete-variable optimization · Evolutionary algorithms

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## 1 Introduction

The progressive scaling of CMOS technology towards nanometre sizes has made possible the implementation of fully integrated systems for the wireless communication applications. As result of the progress in technology development and the use of deep submicron CMOS processes, digital circuits have become faster, more precise, and with decreased of the implementation area. This technological improvement enforces more stringent specifications in terms of gain, phase noise and size for the analog/RF counterparts. Consequently, the design of analog/RF devices becomes more challenging, as recent technologies carry two major difficulties: firstly, due to the reduction of the oxide thickness, parasitic capacitances increase; secondly, smaller output resistances are obtained, enforced by short channel-effects. Thus, the challenge of analog/RF design task nowadays is to design a circuit to meet the required specifications, at low supply voltage, (for low power consumption) and showing low phase noise, in spite of the fact that transistors have more parasitic effects and less intrinsic gain. Moreover, the need for implementing fully integrated circuits renders imperious the design of passive devices where the technology characteristics are pushed to its limits.

In the particular case of *LC*-VCOs the use of integrated inductors brings several issues, such as the degradation of the phase noise or the increase in the power consumption due to low on-chip *LC* tank quality factor (Q). As a matter of fact the inductor Q in the GHz range of operation is in the order of 5–15, due to the thin metal thickness and to the substrate losses [1]. Yet, as the process technology improves and the number of metal layers increases, the passive elements Q is improving [2]. Furthermore, technology scaling down has lead to a decrease in the supply

voltage, thus making the analog design more challenging, since neither a wide range of linearity nor full output voltage swing are easily guaranteed [3].

In the particular case for *LC* voltage controlled oscillators (VCO) several design methodologies have been proposed in the literature. An automated and layout-aware RF *LC*-VCO design tool, entitled CYCLONE is described in [4]. The proposed tool combines in the design process both the device-level simulation for granting the accuracy of the tool and the advantage of evolutionary algorithms (EA), for the search of the best feasible solution. As a tremendous effort is put on the design accuracy, electromagnetic finite-element simulators are used, in particular for the inductor characterization, as its parasitics can easily jeopardize expected performances. In [5] a methodology for reducing the phase noise of a cross-coupled *LC*-VCO is proposed. Results for an operating frequency of 2 GHz in 0.18 μm CMOS technology are presented. This methodology, however, suffers from being based in fundamental relationships between the phase noise and the channel length, without exploring other optimization opportunities. Another VCO design methodology is proposed in [6]. In this work design trade-offs are considered in a graphic representation of the design space, offering the designer a deep insight into the *LC* tank key parameters. This methodology presents a very straight design methodology, based on bifurcation analysis, but is difficult to adapt to new design strategies. In [7] a heuristic algorithm that seeks to determine optimal designs for inductors, bias current and transistors channel widths, aiming to minimize VCO phase noise is considered. However, the analytical models that characterize the elements behaviour, do not account for parasitics, which have to be subsequently obtained through simulations. In [8], another *LC*-VCO model-based design methodology is proposed, where bias controllability is introduced. Yet, the analytical models used are very simple, restricting its use to the proof of concept. More recently, the design of *LC*-VCOs based on the $g_m/I_D$ approach was proposed in [9]. Although it offers the possibility for exploring all inversion regions of the MOS transistors, the $g_m/I_D$ technique is not easily extended for the characterization of the varactor. Concerning the optimization procedure, a complete description of an integrated *LC*-VCO design is presented in [10], where the complexity of the optimization design, regarding the number of variables involved, is focused. A graphical optimization methodology using nonlinear programming is proposed, providing essential intuition in finding the optimum solution.

The main goal of the work proposed in this paper, relies on the identification the most suitable analytical models that accurately characterize the behaviour of each single element in the *LC*-VCO. These models, which must rely on technological parameters, are a fundamental key for an optimization based design procedure that aims to be simulation independent. Such kind of analytical models, allow the designer to understand the device key parameters and to successfully apply this knowledge in the design of the analog/RF circuits.

Regarding the optimization engine EA, are used. Due to the specificity of the problem under analysis, the optimization engine is able to deal with discrete and continuous variables as well as constrained search space. Furthermore, the optimization engine considered allows designers to deal with design trade-offs, such as phase noise and power consumption, avoiding the blind believe in simulators. The main advantage of the methodology proposed in this work is twofold. In one hand the use of accurate device models, makes the determination of design parameters very rapid. On the other hand as the model parameters are mostly based on technological parameters, the adaptability of the design process to new technologies is extremely easy [11].

Besides the Introduction, this paper comprises four additional sections. Section 2 presents the design approach, supported in analytical models, which allows characterizing the oscillator performance. Then, in Sect. 3, the *LC*-VCO optimization strategy used in the proposed work is presented. A set of *LC*-VCO design examples is presented in Sect. 4, where the solutions obtained with the proposed methodology are compared against HSPICE/HSPICE RF simulation results. Finally, conclusions are offered.

## 2 *LC*-VCO design approach

One of the main challenges in designing a VCO using a model-based methodology is to obtain results that prove to be sufficiently accurate when compared to the corresponding chip measurements. For this propose, accurate models are essential for each of the circuit blocks, where parasitics must be accounted for. For the sizing of *LC*-VCOs the design methodologies usually adopted, rely on the accuracy of models of each element. Although designers may use very accurate models, for predicting the VCO performance, there will always be a certain error due to some parasitic effects that appear in the manufacturing process [12]. The tunable feature that characterizes a VCO, is of major importance, since it can compensate the parasitics effects of the manufacturing process. In Fig. 1 a cross-coupled *LC*-VCO with two main blocks is represented: the *LC* tank responsible for the oscillation frequency, and the negative transconductance amplifier, which accounts for reducing the circuit losses by introducing a negative resistance. Most *LC*-VCO designs aim at achieving both minimum phase noise and power consumption for a certain oscillation frequency. In Fig. 2 the typical design trade-offs for *LC*-VCO design are depicted.

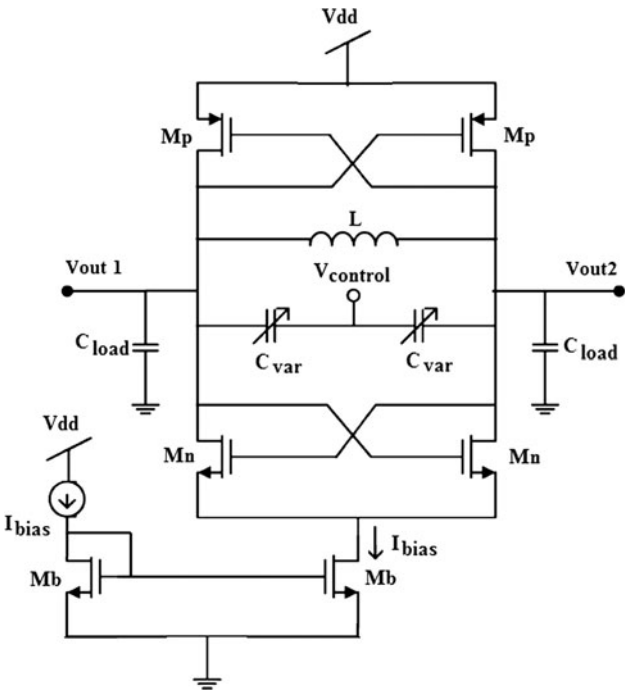


**Fig. 1** Cross coupled *LC*-VCO topology

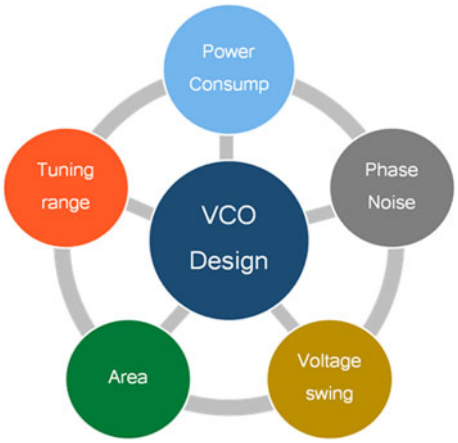


**Fig. 2** *LC*-VCO design trade-offs

For instance, if low-power consumption is a major concern, then a low bias current is usually considered. Yet, this strategy may increase the parasitic effects yielding to the degradation of the VCO phase noise. On the other hand, if low phase noise is envisaged, high output voltage swing should be considered. To achieve this goal o different strategies may be followed. The designer may opt to increase the bias current, resulting in an increase in the power consumption. On the other hand, higher inductance may be considered but this will reduce the VCO tuning range [13]. The necessity for coping with correlated design parameters makes the VCO design a candidate for optimization based design methodologies.

Besides the design trade-offs pointed out, designers have also to decide between accuracy versus efficiency in the optimization methodology. For high accuracy of results simulation based optimization methodologies are usually adopted. Yet for the particular case of integrated inductors the necessity for using electromagnetic simulators makes them extremely inadequate for being integrated into optimization methodologies for their prohibitive lengthy simulation times. On the other hand, analytical-based systems usually run faster, are able to deal with complex circuit design, provide useful insight into circuit behaviour and are easily adaptable to new "realities", such as new technology processes. Therefore, analytical models capable to characterize the behaviour of each element of a circuit are needed. In the next subsection, an introduction to the *LC*-VCO circuit analytical model is offered.

### 2.1 Circuit modelling

As previously presented, the efficiency of the design process is guaranteed through the use of analytical models for the characterization of both passive and active circuit elements. For the clarity of exposure, and due to space constraints, just a brief description of the analytical models used will be done. The characterization of the CMOS transistors is based on the well know EKV2.6 [14], yielding a good accuracy of the results for low-voltage circuit design.

The EKV MOS transistor model has been developed to facilitate the compact modelling and simulation of low voltage devices for application in low power semiconductor technologies. The main advantage of using the EKV model in the characterization of the MOS transistor behaviour relies on the fact that a single accurate expression, valid from weak to strong inversion and from linear to saturation region, is used [15]. This characteristic makes the EKV model suitable for analytical design and simulation of analog circuits, allowing a deep insight into the device behaviour.

The EKV model has been derived considering the charges in the transistor, and an expression for the drain/source current, $I_{ds}$, was proposed, where

$$I_{ds} = I_s\left(i_f - i_r\right), \tag{1}$$

with $I_s$, $i_f$, $i_r$ as the specific, forward and reverse current respectively, and given by

$$i_{f(r)} = \left[\ln\left(1 + \exp\left[\frac{V_P - V_{s(d)}}{2U_T}\right]\right)\right]^2, \tag{2}$$

$$I_s = 2nU_T^2\frac{\beta_0}{1 + \Theta\, V_P'}, \tag{3}$$

where $U_T$ is the thermal voltage, $\beta_0$ is a transconductance parameter and $n$ is the slope factor. The charges mobility reduction is taken into account by means of $\Theta$, which is the

mobility reduction coefficient and $V'_P$ which is a function of the pinch-off voltage, $V_P$.

The characterization of the varactor behaviour is also supported by EKV MOS model equations, which are based on process and technological parameters, avoiding the undesired empirical/fitting factors granting the accuracy of the results. The EKV transistor model is suitable to perform the CV-characterisation of varactors, when integrated in a computer design process, due to the continuity of the model and the reduced number of model parameters. According to [16], the intrinsic capacitances of a varactor, are obtained through the relative variation of the nodes charge to the node voltage

$$C_{xy} = \pm \partial Q_x / \partial V_y \text{ with } x, y = G, D, S, B \tag{4}$$

In a varactor, the total capacitance is usually referred as the gate capacitance, since the drain, source and bulk are connected to a fixed voltage, which allows neglecting the drain/source—bulk capacitance. Additionally, overlap and fringing capacitances—extrinsic capacitances—must be accounted for. The varactor total capacitance can be obtained through

$$C_{total} = C_{GB} + C_{GD} + C_{GS} + C_{S(D)B} + C_{extrinsic}. \tag{5}$$

In [16, 17] simplified expressions to determine each of the intrinsic capacitances are proposed. The varactor intrinsic capacitances are obtained through the set of equations

$$C_{GS} = \frac{2}{3} C_{ox} \left[ 1 - \left( I_{rev}^2 + I_{rev} + 0.5 I_{for} \right) / \left( I_{rev} + I_{for} \right)^2 \right], \tag{6}$$

$$C_{GD} = \frac{2}{3} C_{ox} \left[ 1 - \left( I_{for}^2 + I_{for} + 0.5 I_{rev} \right) / \left( I_{rev} + I_{for} \right)^2 \right], \tag{7}$$

$$C_{GB} = C_{ox} \left[ \left( n_q - 1 \right) / n_q \right] \times \left[ 1 - C_{GS}/C_{ox} - C_{GD}/C_{ox} \right], \tag{8}$$

$$C_{SB} = \left( n_q - 1 \right) \times C_{GS}, \tag{9}$$

$$C_{DB} = \left( n_q - 1 \right) \times C_{GD}, \tag{10}$$

where $I_{rev}$ and $I_{for}$ are the normalised reverse and forward current, respectively; $n_q$ is the slope factor, $\gamma$ is the body effect parameter, $V_P$ is the pinch-off voltage, and $\phi$ the Bulk Fermi potential, obtained by

$$I_{rev} = \sqrt{0.25 + i_r} \tag{11}$$

$$I_{rev} = \sqrt{0.25 + i_r} \tag{12}$$

$$n_q = 1 + \frac{\gamma}{2\sqrt{V_P + \phi + 10^{-6}}} \tag{13}$$

For more details regarding the CV-characterization of the varactor, please see Ref. [18].

Regarding the inductor modeling, there are three major sources of losses that must be accounted for. Namely, the series resistance of the inductor, which depends on geometric and technological parameters, such as the inductor length, eddy currents and the skin effect at high frequencies; the capacitive coupling between metal and substrate; and the power losses due to eddy currents in the substrate.

With respect to the inductor, the double pi-model is adopted, where the model component values are obtained through analytical expressions based on both technology parameters and device geometric characteristics [19]. Although more accurate but more complex models might have been adopted, for the range of frequency of a few GHz, the double pi-model yields quite accurate results.

Concerning the full *LC-VCO* characterization, the fundamental equations for the oscillation frequency and oscillation condition are given by

$$f_0 = \frac{1}{2\pi\sqrt{L_{\text{tank}}\, C_{\text{tank}}}} \tag{14}$$

$$\alpha \times g_{\text{tank,max}} \leq g_{\text{active}}, \tag{15}$$

where $\alpha$ in the range of 2–3 assures the start-up condition. The tank and active conductances, $g_{tank}$ and $g_{active}$, respectively, are obtained through

$$g_{\text{tank}} = g_{\text{ind}} + g_{\text{var}} + \frac{g_{\text{ds,p}}}{2} + \frac{g_{\text{ds,n}}}{2} \tag{16}$$

$$g_{\text{active}} = \frac{g_{\text{m,p}}}{2} + \frac{g_{\text{m,n}}}{2} \tag{17}$$

where $g_m$ is the transistor transconductance.

The differential output voltage, $2 \times V_{tank}$, is determined as in

$$V_{\text{tank}} = \frac{4}{\pi} \frac{I_{\text{bias}}}{g_{\text{tank}}} \tag{18}$$

In order to garantee enough voltage swing to the following circuit, $V_{tank}$ can be limited to $V_{tank,min}$. The oscillation tuning range is given by

$$\frac{1}{\sqrt{L\, C_{\text{tank,max}}}} \leq \omega \leq \frac{1}{\sqrt{L\, C_{\text{tank,min}}}} \tag{19}$$

where the $C_{tank}$ takes into account the both the varactor capacitance, and the active elements output capacitance.

Phase-noise is an elementary characteristic of a VCO that depicts the purity of the oscillation signal in the vicinity of the oscillation frequency $f_0$. In this work, the VCO phase-noise is obtained through [20]

$$L\{\Delta_f\} = 10 \log \left[ \frac{1}{16\pi^2 \Delta_f^2} \times \frac{L_{\text{tank}}^2 (2\pi f_0)^4}{V_{\text{tank}}^2} \cdot \frac{1}{2K_B T \left[ g_L + g_{\text{var}} + \gamma \left( g_{\text{d0,p}} + g_{\text{d0,n}} \right) \right]} \right] \tag{20}$$

where $\Delta_f$ is the frequency in the vicinity of $f_0$, $g_{d0}$ is the drain conductance when $V_{DS} = 0$, $K_B$ is the Boltzmann

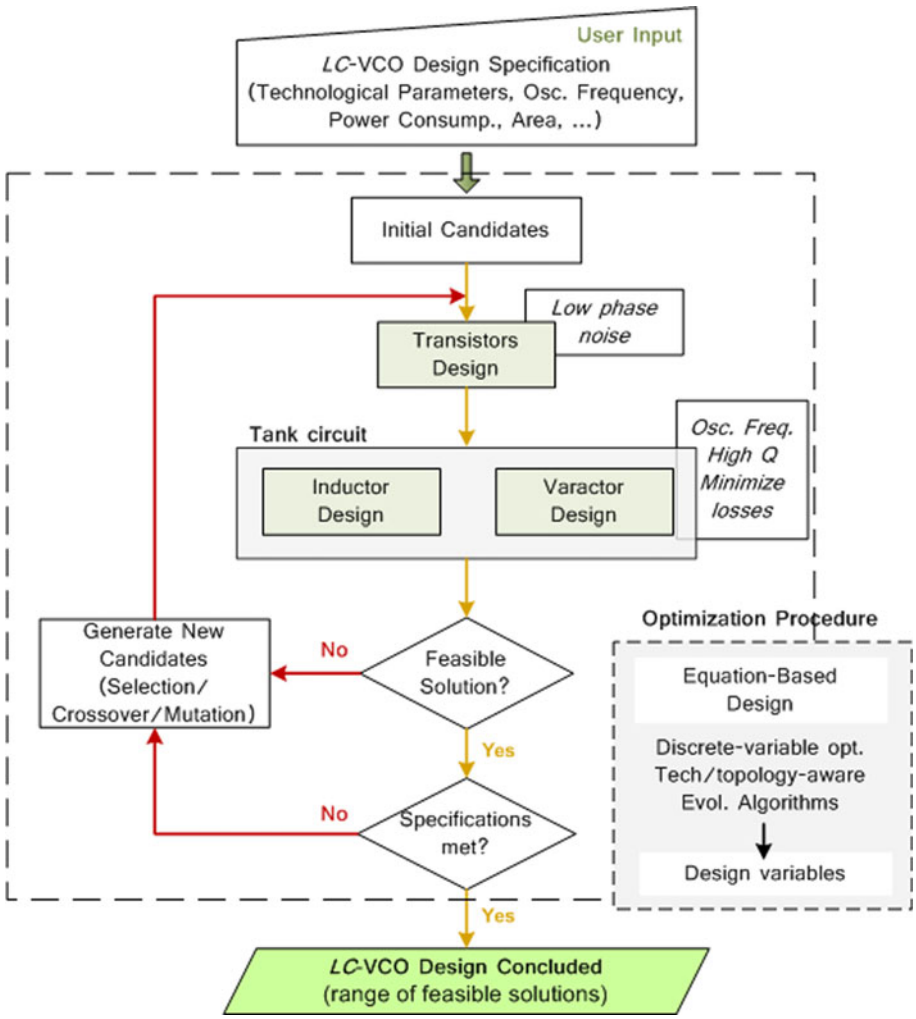


**Fig. 3** *LC*-VCO optimization design flowchart

constant, $T$ is the temperature in Kelvin, and $\gamma$ is the excess noise factor. Finally, a figure of merit is used to compare circuits' performance, given by

$$FoM = L\{\Delta_f\} - 20\log\left(\frac{f_0}{\Delta_f}\right) + 10\log\left(P_{\mathrm{dc\,(mW)}}\right) \qquad (21)$$

## 3 *LC*-VCO optimization strategy

The design flow for the proposed optimization based *LC*-VCO methodology is represented in Fig. 3. Considering the *LC*-VCO topology illustrated in Fig. 1, the design process starts with the design of the active elements, since the drain current in each transistor is the dominant contributor to the phase noise. The following step addresses the optimization of the *LC* tank, by maximizing both the corresponding Q, and tank tuning range. Therefore, the overall optimization procedure main goal consists on the minimization of both the circuit power consumption and phase noise. To deal with both criteria, the figure of merit, FoM, (21) will be adopted.

Concerning the optimization engine, EA are used. EA have been widely used, since they have proved to be a quite reasonably alternative to classic search methods, such as Fibonacci, Dynamic programming or the branch & bound. In the next subsection, a brief introduction to EA, is offered.

### 3.1 Evolutionary algorithms

EA have been proposed as an attempt to mimic of the processes in natural evolution. Despite some lack of explanation regarding the details of biological evolution, there are some interpretations are supported by experimental observation [21]:

- Evolution is a process operating over chromosomes rather than over organisms;
- Natural selection is the mechanism that relates chromosomes with the efficiency of the entity they represent;
- The evolutionary process takes place during the reproduction phase.

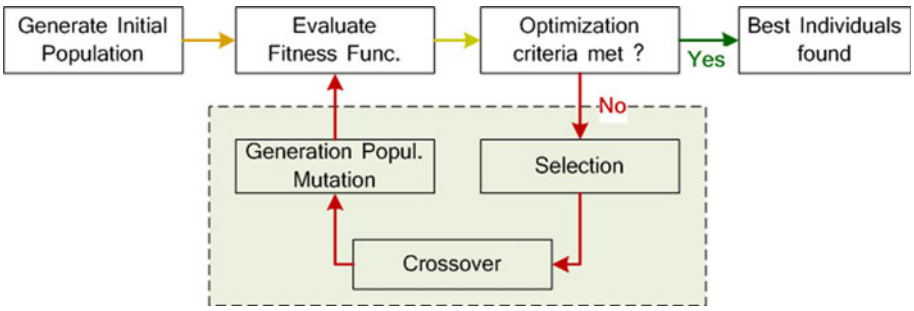


**Fig. 4** Genetic algorithm procedure flowchart

Based on the three mentioned features, the development of EA took place. An EA is an iterative and stochastic process that operates on a set of individuals, which forms a population, where each individual represents a probable solution to the problem under consideration. Every single individual that belongs to the population is evaluated by means of a fitness function, and its value represents a measure of its quality, regarding the problem in analysis. This value that characterizes the individual is the valuable information that the algorithm uses, to go into the next step in the search procedure.

Among several evolutionary techniques, the genetic algorithms (GAs) are the most extended group that applies the evolutionary tools: selection, crossover, mutation and generation of new individuals. GAs use only the results obtained through the fitness function in the search space process—search a population of points in parallel instead of a single point, thus making results less sensitive to the point chosen in order to go towards the best solution. Continuity or discontinuity of the problem functions is neither required nor used in calculations of the algorithm loop, Fig. 4. This feature makes GAs very general and suitable for all kind of problems: discrete, continuous, non-differentiable, or even mixed search spaces. Furthermore, GAs do not require derivative information or previous knowledge, as well as the algorithm determines global optimum solutions, avoiding getting trapped in local maximum/minimum, as frequently happen with continuous variable optimization algorithms [22].

Stochastic optimization algorithms such as GAs have shown to be effective and robust methods for solving difficult optimization problems. These algorithms typically converge to one final solution because of the global selection scheme used. However, in the particular case of the design problem under consideration, due to its complexity, it is important to guarantee that the multiple satisfactory solutions generated, in terms of devices sizes, converge to a close solution.

### 3.2 Optimization algorithm robustness

To evaluate the robustness of the optimization tool, a performance test was made. As the full optimization of an

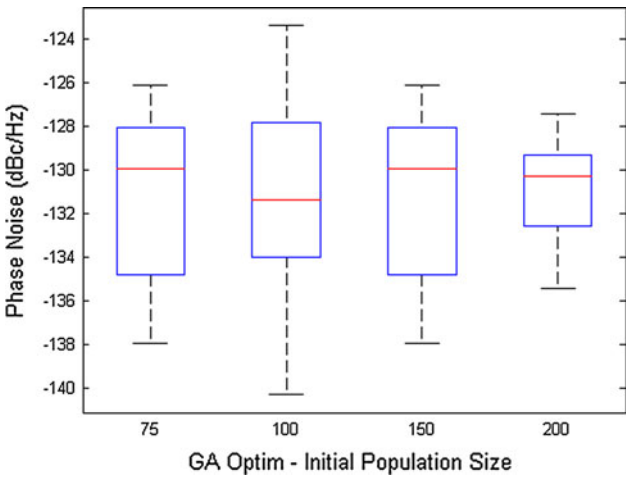


**Fig. 5** Boxplot of phase noise

*LC*-VCO involves thirteen variables, the bias current value was imposed as a way of minimizing the number of design variables. Basically, on this performance test, the circuit performance will mostly depend on the tank circuit. Thus, the design tool will consider the optimization of seven independent parameters: four regarding the inductor, plus three concerning the varactor. For the inductor design the track width, the number of turns, the inductor shape, and the internal diameter were considered. The varactor optimization comprises the transistor width, length and number of gate fingers. The current through the oscillator, $I_{bias}$, was fixed to 1.2 mA, and the envisaged oscillation frequency was 1.5 GHz.

For the performance test of the optimization algorithm a variation in the population size was considered, as this number strongly influences the running time of the tool. Four different population sizes were assumed, 75, 100, 150 and 200 individuals, and for each case the design tool ran for 15 times. The results are expressed by means of boxplots (or *whisker* diagram), which illustrate the spread of a set of data, thus indicating the convergence of the optimization results. In Figs. 5 and 6, boxplots for both the phase noise and the figure of merit, respectively, are presented.

In Figs. 5 and 6, the boxes represent the range of values of 50 per cent of the total data, called the inter-quartile range,

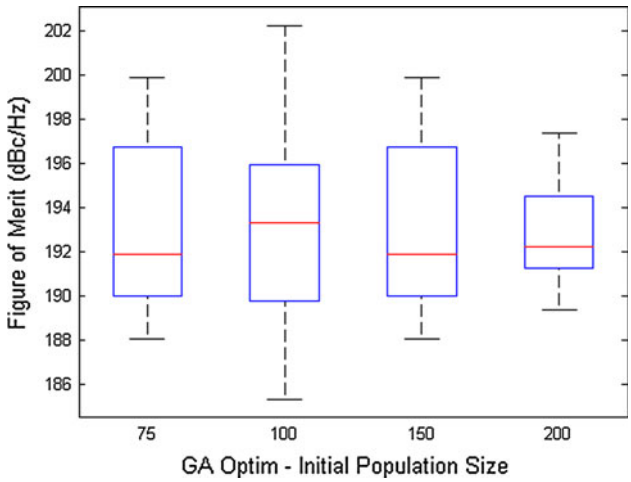


**Fig. 6** Boxplot of figure of merit

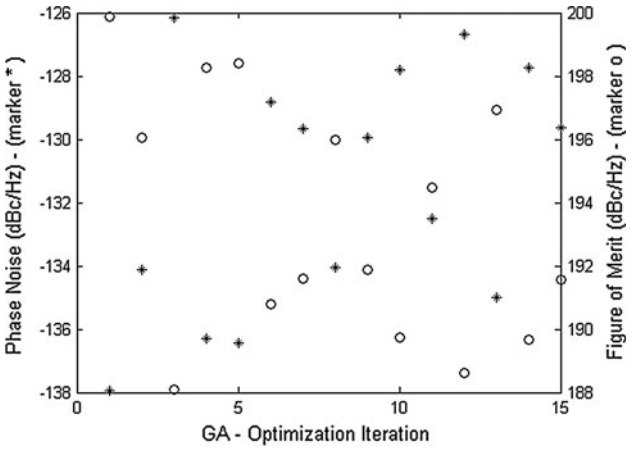


**Fig. 7** Phase noise and figure of merit—population with 75 individuals

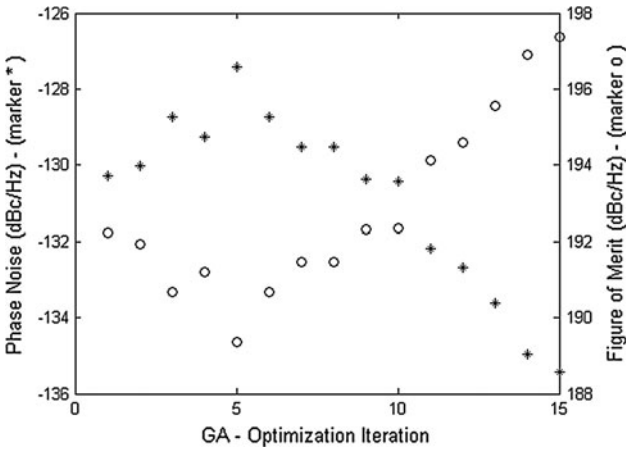


**Fig. 8** Phase noise and figure of merit—population with 200 individuals

where the line inside the box is the median value. The upper quartile represents the highest 25 per cent of the data, and is represented in the *whisker* above the box. Finally, the lowest 25 per cent of the data, the lower quartile, is shown under the box limits. As expected, as the population increases, except for the case of the population with 100 individuals, the range of results gets tighter, i.e., the convergence of the optimization values is more unequivocal. In Fig. 5, it is possible to observe that for the first case, a population with 75 individuals, the range for phase noise goes from −126 to −138 dBc/Hz, which means a variation around 10 per cent. However, it is also possible to conclude that 50 per cent of the results are between −126 and −130 dBc/Hz, which represents a very short variation. The same analysis can be done for the data of the figure of merit represented in Fig. 6. It is also possible to observe that the median value is approximately the same in all cases. With respect to the running time, the proposed tool for the design of the *LC*-VCO spent 5, 6, 9 and 14 min to perform each one of the 15 design processes, for the four examples with different population sizes, respectively.

In Figs. 7 and 8 the results of each one of the 15 design iterations for the cases of a population with 75 and 200 individuals, correspondingly, are depicted in more detail.

By analysing the results represented in the previous figures, it is possible to conclude that optimization approach by means of GAs is a suitable candidate for the design of a *LC*-VCO.

## 4 *LC*-VCO optimization and simulation results

The present work describes an *LC*-VCO design methodology implemented in Matlab using the GAs toolbox. In this section the design of three *LC*-VCOs for operating frequencies of 1.0, 2.4 and 2.8 GHz in UMC130 technology is addressed. The design objective function aims to minimize the oscillator figure of merit (21). The envisaged VCO characteristics and parameters range are given in Table 1.

Concerning the full *LC*-VCO design optimization, as mentioned before, three cases for different operation frequencies were considered. Additionally to the inductor and varactor parameters, each of the transistors (Mp, Mn and Mb, see Fig. 2) width was also considered. The transistors length was fixed to three times the technological minimal length. For the optimization procedure, a population of 150 individuals was assumed. The results obtained with the proposed methodology as well as those obtained through HSPICE and HSPICE RF simulations, are presented in Table 2. In all the VCO characteristics the error is always less than 10 %, showing a quite good agreement between predicted and simulations results. Yet, the use of a tunable capacitor provides the VCO with the possibility of reducing this error. In Table 3 the size of all the *LC*-VCO elements is offered. Table 4 presents a comparison between results obtained with the present design methodology, and results published in

**Table 1** *LC*-VCO characteristics and parameters limits

| Center frequency $-f_0/\Delta_f$ | 1.0, 2.4, 2.8 GHz/1 MHz |
|---|---|
| Bias current (mA) | 0.5–3 |
| Output voltage swing | $V_{DD}/8$–$V_{DD}/2$ |
| Transistor width | $3 \times L_{min}$–500 μm |
| Tank inductance—L (nH) | 1–15 |
| Tank capacitance—$C_{var}$ (pF) | 1–20 |
| $C_{Load}$ (pF) | 1 |

related work, showing similar results for phase noise and FoM. Furthermore, and regarding the power consumption, the proposed design is placed in lowest half part, due to a smaller $I_{bias}$ that corresponds to smaller active elements, and consequently with lower implementation area.

In Fig. 9 the VCO output signals for an oscillation frequency of 1.0 GHz are presented. With the proposed design, after 10 ns the VCO reaches to oscillation stability. The output signal oscillates between 0.66 and 1.04 V, which represents a tank output swing of 0.38 V, as shown in Fig. 10. Also, at the centre frequency, 1.0 GHz, the oscillator phase noise reaches to −116.2 dBc/Hz.

From the simulations performed through HSPICE/RF simulator, the VCO output signal for an oscillation frequency of 2.4 GHz is presented in Fig. 11, where it is possible to observe after 4 ns the VCO reaches to oscillation stability. The simulated circuit reaches a oscillation frequency of 2.2 GHz, representing an error around 8 per cent of the desired frequency. The output signal oscillates between 0.59 and 1.11 V, which represents a tank output swing of 0.52 V, as shown in Fig. 12. Also, at the centre frequency, 2.2 GHz, the oscillator phase noise reaches to −116.2 dBc/Hz.

## 5 Conclusions

This paper introduces a model based *LC*-VCO design methodology based on EA. The oscillator analytical model is supported by a set of equations based in technology parameters. The optimization design tool presented in this work has two main advantages: (i) as the VCO model is based in technological parameters, it may be adapted to new technologies in a straightforward way; (ii) reduced computation time, if compared with electromagnetic simulator based optimization procedure.

Furthermore, in this work the design of *LC*-VCO is supported by a GA optimization methodology, which is able to deal with both continuous and discrete variables,

**Table 3** *LC*-VCO elements size

| Parameter | 1.0 GHz | 2.4 GHz | 2.8 GHz |
|---|---|---|---|
| Active elements (transistors) | | | |
| $W_p$ (μm) | 217.8 | 326.8 | 272.3 |
| $W_n$ (μm) | 88.6 | 132.9 | 110.8 |
| $W_b$ (μm) | 78.6 | 117.9 | 98.3 |
| Inductor | | | |
| w (μm) | 9.00 | 14.25 | 9.25 |
| $d_{in}$ (μm) | 97.75 | 152.75 | 101.50 |
| N turns | 5.5 | 2.5 | 2.5 |
| Shape | 4 | 6 | 4 |
| Varactor | | | |
| W (μm) | 387.3 | 112.3 | 129.8 |
| L (μm) | 0.79 | 0.79 | 0.74 |
| N*f* | 100 | 70 | 83 |

**Table 4** Comparison of Published VCO Performances

| Ref. | Tech. | *fo* (GHz) | Pdc (mW) | L {1 MHz} (dBc/Hz) | FoM (dBc/Hz) |
|---|---|---|---|---|---|
| Prop. work | CMOS 0.13 μm | 2.4 | 1.50 | −109.4 | 174.4 |
| [7] | CMOS 0.35 μm | 2.6 | 8.20 | −124.9 | 184.1 |
| [23] | SiGE-BJT process | 2.4 | 41.2 | −128.0 | 179.5 |
| [24] | CMOS 0.18 μm | 2.2 | 5.17 | −119.0 | 179.0 |
| [25] | CMOS 0.13 μm | 2.4 | 1.25 | −117.1 | 187.0 |
| [26] | CMOS 90 nm | 2.4 | 1.00 | −119.7 | 190.0 |

**Table 2** Optimization design results versus simulation

| | 1.0 GHz | | 2.4 GHz | | 2.8 GHz | |
|---|---|---|---|---|---|---|
| | Optim | Hspice | Optim | Hspice | Optim | Hspice |
| $I_{bias}$ (mA) | 1.00 | 1.05 | 1.50 | 1.58 | 1.25 | 1.31 |
| $L_{tank}$ (nH) | 7.0 | – | 2.0 | – | 1.5 | – |
| $C_{var}$ (pF) | 4.40 | 4.44 | 1.28 | 1.32 | 1.36 | 1.39 |
| $V_{outAmp}$ (V) | 0.16 | 0.18 | 0.23 | 0.26 | 0.18 | 0.21 |
| $P_{dc}$ (mW) | 1.20 | 1.25 | 1.80 | 1.86 | 1.50 | 1.56 |
| $f_0$ (GHz) | 1.01 | 0.95 | 2.40 | 2.20 | 2.81 | 2.60 |
| L {1 MHz} (dBc/Hz) | −115.5 | −116.2 | −109.4 | −121.5 | −105.8 | −122.6 |
| FoM (dBc/Hz) | 174.7 | 174.8 | 174.4 | 185.6 | 173.0 | 188.9 |

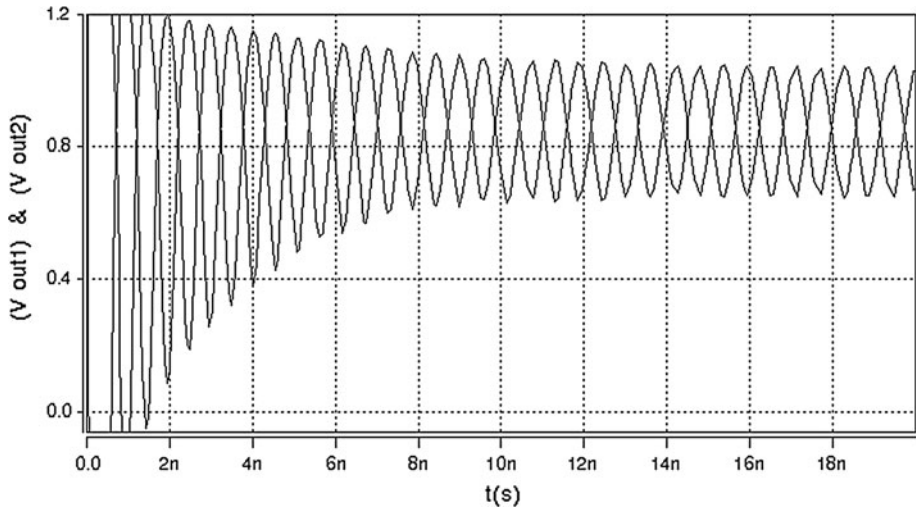


**Fig. 9** *LC*-VCO output signal (Vout1 and Vout2) @ 1.0 GHz

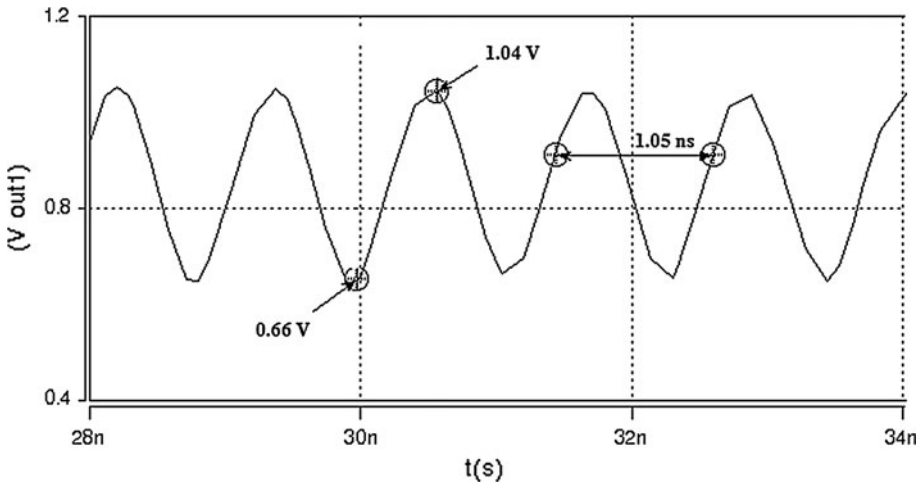


**Fig. 10** Vout1 @ 1.0 GHz with indication of signal period and output swing

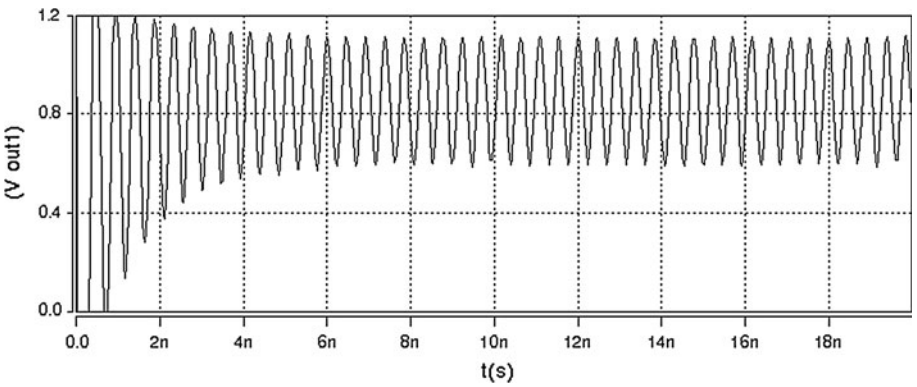


**Fig. 11** *LC*-VCO output signal Vout1 @ 2.4 GHz

making possible to satisfy both technological and layout constraints, avoiding the rounding-off problem of the classic continuous optimization design [27]. A set of design examples showing the design of three VCOs for different oscillation frequencies is shown. The results presented, duly validated against HSPICE/RF simulations, point out the potential of proposed work, when integrated in a top-level design tool.

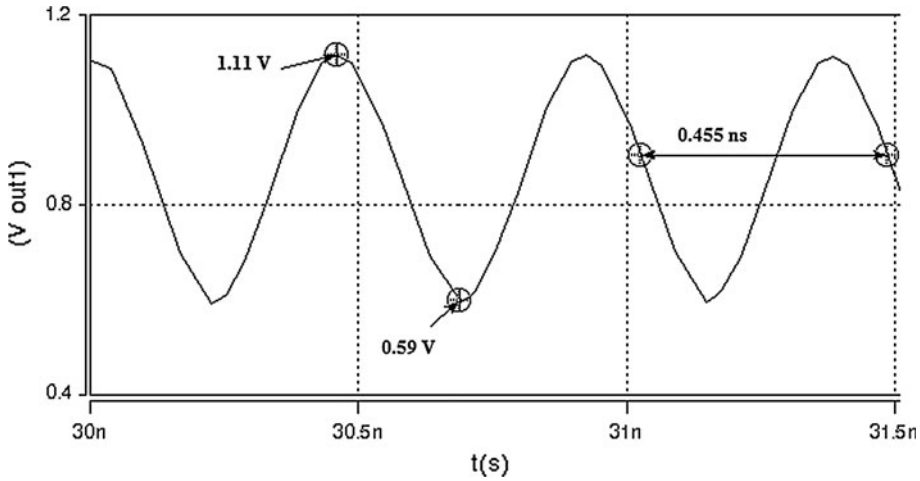


**Fig. 12** Vout1 @ 2.40 GHz with indication of signal period and output swing

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