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An ultra-low power energy-efficient microsystem for hydrogen gas sensing applications

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Abstract This paper presents a fully integrated power management and sensing microsystem that harvests solar energy from a micro-power photovoltaic module for autonomous operation of a miniaturized hydrogen sensor. In order to measure H_2 concentration, conductance change of a miniaturized palladium nanowire sensor is measured and converted to a 13-bit digital value using a fully integrated sensor interface circuit. As these nanowires have temperature cross-sensitivity, temperature is also measured using an integrated temperature sensor for further calibration of the gas sensor. Measurement results are transmitted to the base station, using an external wireless data transceiver. A fully integrated solar energy harvester stores the harvested energy in a rechargeable NiMH microbattery. As the harvested solar energy varies considerably in different lighting conditions, the power consumption and performance of the sensor is reconfigured according to the harvested solar energy, to guarantee autonomous operation of the sensor. For this purpose, the proposed energy-efficient power management circuit dynamically reconfigures the operating frequency of digital circuits and the bias currents of analog circuits. The fully integrated power management and sensor interface circuits have been implemented in a 0.18 μm CMOS process with a core area of 0.25 mm^2. This circuit operates with a low supply voltage in the 0.9–1.5 V range. When operating at its highest performance, the power management circuit features a low power consumption of less than 300 nW and the whole sensor consumes 14.1 μA.

Keywords Analog integrated circuits · Solar energy harvesting · Ultra-low power circuits · Power management circuits · Sensor interface circuits · Wireless sensor networks

1 Introduction

There is an increasing demand for energy-efficient wireless sensor networks (WSN) in different sensing and monitoring applications. Many autonomous WSN solutions have been deployed in different areas, including health and lifestyle, automotive, smart buildings, predictive maintenance (e.g. of machines and infrastructure), and active RFID tags [1]. These emerging autonomous ultra-low power (ULP) sensors incorporate energy harvesting source, energy storage device and electronic circuits for power management, sensing and communication into a miniaturized system. Solar energy is the most abundant and practical form of ambient energy and miniaturized solar cells are already available in the custom sizes as small as 1 mm^2 [2]. Solar cells can be good energy sources for millimeter-scale autonomous wireless sensor nodes, thanks to their high efficiencies. However, as energy harvested from solar cells is intermittent and the maximum power that it can provide may be much less than the required peak power during data transmission, a rechargeable microbattery or a supercapacitor, should store the harvested energy for reliable operation of the electronic circuits. Successful implementation of energy harvesting for WSN applications depends on meeting size, autonomy and cost constraints.

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Meeting these constraints in millimeter-scale wireless sensors can be quite challenging and highly depends on the chosen application and how the measurement results are processed and sent to a base station or other target sensors. In [3], an autonomous wireless intraocular pressure monitor microsystem has been presented that incorporates a photovoltaic (PV) module, a thin film Li-Ion battery and the electronic circuits for energy harvesting, sensor readout and data communication in a 1.5 mm^3 biomedical implant. Since the sensor is implanted in the eye, meeting the size constraint is crucial. As miniaturized solar cells can provide only a few tens of microwatt under low illumination level, the power management circuit (PMC) should be very low power to have a high efficiency. In addition to harvesting solar energy, the PMC should dynamically reduce power consumption of the sensor under reduced light intensity, to avoid complete discharge of the battery. As a result, even when the harvested solar energy is less than the power consumption of the microsystem, the microsystem can continue its autonomous operation at a lower speed.

The target sensor is a miniaturized autonomous hydrogen sensor. In fact, as the use of hydrogen fuels becomes more common, an increasing demand for miniaturized hydrogen sensors is expected. Miniaturized Palladium (Pd) nanowires have good sensitivity to H_2 concentration and can be used in the room temperature [4]. These sensors are good candidates for realizing millimeter-scale ULP hydrogen sensors, as they are very low power and their size is smaller than 1 mm^2. However, these nanowires have an undesired thermal cross-sensitivity and for accurate measurement of H_2 concentration, temperature should be measured and further compensated during sensor calibration [5]. A grid of 14 Pd nanowires, fabricated on a silicon wafer, has been used for gas sensing [6]. Half of these sensors are only sensitive to temperature and have been used as reference nanowires. The remaining sensors are sensitive to both temperature and H_2 concentration and have been used as sensing nanowires. In order to measure H_2 concentration, the readout circuit measures and converts to digital the conductance change of sensing nanowires in comparison with reference nanowires. The proposed area- and energy-efficient solar energy harvester circuit harvests energy from a PV module consisting of nanowire solar cells in series [7] and stores the harvested energy in a Varta V6HR NiMH microbattery [8]. This circuit measures the remaining charge of the target microbattery and scales the power consumption of the microsystem up or down according to the energy stored in the battery. The resolution and power consumption of the analog-to-digital converter (ADC) is reconfigured according to the remaining charge of the battery.

This paper makes the following contributions: (a) a new PMC has been proposed that not only harvests solar energy from the PV module with very high efficiency, but also scales the power consumption and performance of the target sensor, based on the energy stored in the battery; (b) A new sensor interface with reconfigurable performance has been proposed. In this circuit, a novel incremental ADC with reconfigurable speed and power consumption has been used to convert the measured temperature and H_2 concentration; the remainder of this paper is organized as follows. Section 2 presents the system architecture, including the realized integrated circuit and the required external components. System level design parameters that affect autonomous operation of the sensor, including selection of the appropriate energy storage device and wireless data transceiver, will be discussed thoroughly in this section. Sections 3 and 4 present the circuit implementation of the power management and sensor interface circuits (SICs). In Sect. 5, measurement and simulation results have been discussed to evaluate the performance and autonomous operation of the proposed hydrogen sensor, and finally, Sect. 6 concludes the paper.

2 System architecture

The system level design of a solar energy harvesting system starts by selecting an appropriate energy harvesting source and energy storage device; After that the energy harvester circuit should be designed according to the selected energy source and energy storage device. In order to realize a millimeter-size autonomous sensor, not only the size and power consumption of the sensor and the wireless data transceiver should be minimized, but also the power delivered to the sensor should be maximized. The power that the PV module provides at its maximum power point (P_{mpp}) is the most important parameter, while other characteristics, such as open circuit voltage (V_{oc}) and short circuit current (I_{sc}), should be also considered to design a highly efficient solar energy harvester. These parameters depend on the environmental conditions, including illumination level and temperature. As the DC voltage that the PV module provides may differ from the voltage of the target battery, different DC–DC converters have been proposed to harvest energy from a miniaturized PV module to charge a battery, including switched-capacitor (SC) [9] and inductive DC–DC converters [10]. These DC–DC converters either operate at high frequencies or use external capacitors or inductors to have high efficiency. However, by using higher frequencies, the power consumption of the energy harvester circuit increases and a high efficiency is not achievable under a reduced illumination level when harvested power is not more than a few micro-watts.

The systems targeted for micro-power energy harvesting applications typically have stringent constraints on die area

and usage of external components to meet size, autonomy and cost specifications. Although the proposed H_2 sensor consumes less than 15 μA on average for sensing and wireless data transmission, the peak power consumption during data transmission is much higher. The battery should have enough energy capacity to provide enough power for a few hours' operation of the sensor, even without energy harvesting. In addition to capacity, other characteristics such as size, peak discharge current, nominal operating voltage, end-of-discharge voltage (V_{EOD}), end-of-charge voltage (V_{EOC}), cycle life and leakage, are very important factors to design an energy-efficient sensor that relies on rechargeable batteries. Although miniaturized supercapacitors can provide higher peak discharge currents and have longer cycle lives in comparison with the rechargeable batteries, they have some disadvantages that make them inappropriate for our application. First of all, they have high leakage currents that can be even larger than the current provided by the PV module under reduced illumination level. In addition, they have much lower energy capacity compared with rechargeable batteries of similar sizes. Either a NiMH or a lithium battery can be used as the target rechargeable battery. Among lithium batteries, state-of-the-art thin film lithium batteries, such as MEC125 of Infinite Power Solutions [11], are the best candidates for micro-power energy harvesting applications thanks to their low leakage currents, long cycle lives and high discharge currents. The main disadvantage of these batteries is their high nominal voltage levels. As thin film lithium batteries have nominal voltages of more than 3.8 V, additional DC–DC converters are required to use these batteries for ULP applications. NiMH batteries are more suitable for our application, thanks to their lower nominal voltages.

The block diagram of the target H_2 gas sensor is depicted in Fig. 1. The target V6HR microbattery has a nominal voltage of 1.2 V and can provide a peak discharge current of 18 mA that is much higher than the required current during wireless data transmission. This battery has a large nominal capacity of 6 mAh, while its diameter and height are 6.8 and 2.15 mm, respectively. As in the target sensor, all electronic circuits including the external wireless transceiver can work with a sub-1.2 V supply voltage, additional step-down or step-up circuits are not required. The main disadvantage of this NiMH battery is its lower cycle life compared to supercapacitors and thin film lithium batteries. In addition, this battery has higher leakage current, comparing to thin film Li-Ion batteries. Four miniaturized nanowire solar cells [7] have been connected in series to be used as the PV module. The PMC, not only charges the battery with very high efficiency, but also reconfigures the speed and power consumption of the sensor to guarantee autonomous operation of the sensor in different lightning conditions. The SIC, measures H_2 concentration and temperature. The measurement results are sent to an external wireless transceiver through an embedded serial peripheral interface. The wireless transceiver can communicate the measurement results with the other sensors through establishing a wireless link.

Selecting an appropriate wireless transceiver highly affects autonomous operation of the sensor. In fact, in micro-power energy harvesting applications, minimizing peak and standby power of the transceiver is very important. Low peak power ensures that a miniaturized battery with limited peak discharge current can be used to power up the circuit. Ultra-low standby current guarantees that the average power consumption of the sensor can be minimized by heavily duty cycling of data transmission. The main factors impacting power consumption of a wireless transceiver are supply voltage, carrier frequency and receiver sensitivity. The power consumption of the transceiver can be reduced by operating at a lower supply voltage. Although most of the wireless transceivers work with at least 1.8 V supply voltage, UIP wireless transceivers with sub-1.2 V voltage, such as TZ1053 [12] or ZL70250 [13], are more suited to our application. These transceivers operate at sub-1 GHz frequency bands and have much lower peak-power and standby power, compared with the state-of-the-art 2.4 GHz transceivers. The second important factor is the carrier frequency. Sub-1 GHz wireless transceivers have less power consumption for the same operating range, thanks to reduced attenuation rates and blocking effects at the lower frequencies. Finally, a narrower bandwidth in TZ1053 leads to a higher receiver sensitivity and allows efficient operation at a lower transmission rate. In summary, although sub-1 GHz transceivers have some disadvantages, such as larger size of antennas and lower data rates, they are more suitable for our application.

3 Power management circuit

The proposed energy harvester is based on the direct charging scheme, in which the battery is connected to the PV module using a PMOS switch. A dynamic comparator compares V_{bat} with V_{pv} in a timely manner to avoid discharge of the battery through the PV module when V_{pv} is less than V_{bat}. As the operating voltage of the PV module is determined by the battery, end-to-end efficiency from the PV module to the battery is reduced when the battery voltage diverges from the maximum power point voltage (V_{mpp}) of the PV module during battery charging. As the V_{mpp} of the PV module varies with incident light conditions, an efficient maximum power point tracking (MPPT) scheme can be deployed to ensure that the maximum power

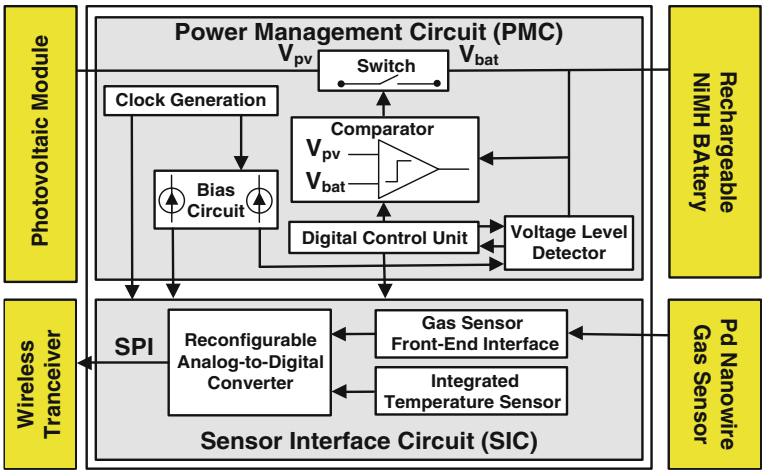

Fig. 1 Block diagram of the proposed hydrogen gas sensor

is extracted from a PV module at any given time. When the PV module is small and can only provide a few microwatts under reduced light intensity, only low-overhead schemes that incur very little power overhead can be good candidates. In [14], several low-overhead MPPT approaches, including fractional open-circuit voltage, fractional short circuit current and hill-climbing techniques, have been discussed that can be deployed in inductive and SC DC–DC converters. In direct charging, as V_{pv} always follows V_{bat}, only design time component matching approach can be used. Nevertheless, by careful selection of the PV module and the battery, PV module will always operate close to its V_{mpp}. In fact, although P_{mpp} and I_{SC} of the PV module change considerably in different lightning conditions, V_{oc} and V_{mpp} of the PV module do not change significantly [15]. In order to achieve high efficiency, the V_{mpp} of the PV module should be close to the V_{EOC} of the battery [16]. For example, in Heliomote [17] two NiMH batteries have been used in series, and the PV module has a V_{mpp} that varied between 2.5 and 3 V depending on the illumination level. Therefore, the PV module is always operated close to its V_{mpp} and a high efficiency is achievable. However, this method is not applicable if the V_{oc} of the PV module is lower than the nominal voltage of the battery.

The second task of the PMC is reconfiguring the performance and power consumption of the sensor, based on the available energy. Since, under the reduced light intensity, the power delivered by the PV module may be lower than the average power consumption of the sensor, the energy harvester circuit should reduce the power consumption of the microsystem to avoid complete discharge of the battery during this period. Under the reduced light intensity, the microsystem continues its autonomous operation at a lower speed and with a lower duty cycle. The battery voltage changes from its nominal voltage during battery charging and discharging. The voltage of the target NiMH battery reaches to the V_{EOD} voltage of 0.9 V when the battery is fully discharged and reaches to the V_{EOC} voltage of 1.5 V when the battery is fully charged, at room temperature. When the target V6HR NiMH microbattery is discharged by a low current, V_{bat} remains almost constant, up to getting close to the fully discharged state. However, if the battery is discharged by a high current, V_{bat} drops immediately and voltage drop depends on the remaining charge of the battery [8]. During wireless data transmission, the battery is discharged by a high current, close to 5 CA (C being the 1 h charge or discharge current). According to the discharge curve of the V6HR NiMH microbattery, if the remaining charge of the battery is more than 80 %, V_{bat} is higher than 1.1 V during this period; however, if it is less than 80 %, V_{bat} drops from 1.1 V down to 900 mV, depending on the remaining charge of the battery. The proposed energy harvester circuit detects the battery voltage during this period to accurately estimate the energy stored in the battery and the power-performance of the sensor is reconfigured to guarantee autonomous operation of the sensor. If V_{bat} is high enough, the power management and SICs work at their highest speed, and the measurement results are sent to the base station every 15 s. If V_{bat} is not high enough, the SIC and the wireless transceiver are activated with a lower duty cycle to minimize the total power consumption of the sensor. In order to reduce the power consumption and speed of the digital circuits, the operating frequency is scaled down and data transceiver is activated by a lower duty cycle. Meanwhile, bias currents are also scaled down to reduce the power consumption and speed of the analog circuits. Finally the last task of the energy harvester circuit is protecting the battery against overcharge and overdischarge. In order to avoid overcharge or overdischarge that reduces the cycle life of the battery, V_{EOC} and V_{EOD} voltage levels are detected. The battery is disconnected from the PV module when V_{bat} reaches to the V_{EOC} limit to avoid overcharge.

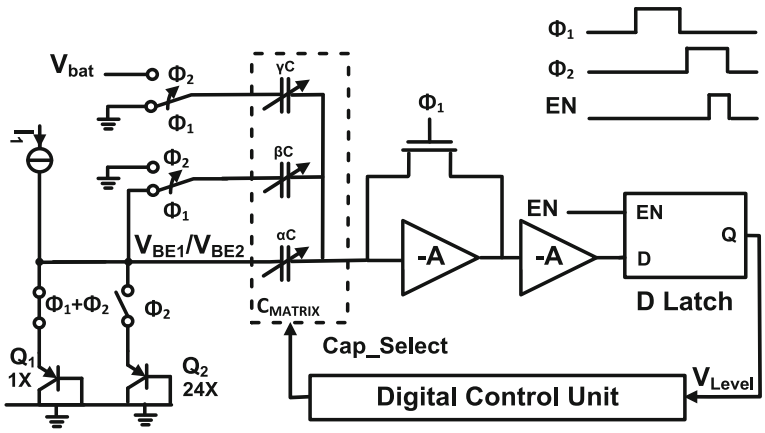

Fig. 2 Circuit diagram of the voltage level detector

When V_{bat} reaches to the V_{EOD} limit, the SIC and the wireless transceiver are deactivated temporarily to avoid overdischarge.

The voltage level detector (LD) in Fig. 2 is used to determine the battery voltage level [5]. After circuit startup, battery voltage is checked to make sure that it is more than V_{EOD} and can power up the circuit. If V_{bat} is less than V_{EOD}, it means that the battery is fully discharged and cannot provide enough power for the electronic circuits. In this situation, the PV module continuously charges the battery by keeping the switch closed. As soon as the V_{bat} passes V_{EOD}, LD starts its normal operation, comparing the V_{bat} with the target threshold voltages in a timely manner and updating the V_{Level} as a result. In order to generate a bandgap reference voltage, 25 substrate PNP transistors have been used as Q_1 and Q_2 in a common-centroid layout. These transistors are biased with a 100 nA current source to generate V_{BE1} and V_{BE2} voltages in non-overlapping Φ_1 and Φ_2 clock phases, and the SC circuit sums up V_{BE1} and $(V_{BE1} - V_{BE2})$ with appropriate coefficients. When V_{bat} reaches V_{EOC}, the switch between the PV module and the battery is turned off to avoid overcharge of the battery. This SC circuit detects when V_{bat} passes the V_L specified in Eq. (1) by setting the V_{Level} output. By using a variable γC capacitor, different voltage levels between V_{EOD} and V_{EOC} can be detected to estimate the remaining charge of the battery. In Eq. (1), α, β and γ coefficients are the ratios of tunable αC, βC and γC capacitors that are determined by Cap_Select signals from digital control unit.

$$V_L = [\alpha \times (V_{BE1} - V_{BE2}) + \beta \times V_{BE1}]/(\gamma) \quad (1)$$

As can be seen in Table 1, by modifying αC, βC and γC capacitors, different battery voltages, starting from V_{EOD} of 0.9 V up to V_{EOC} of 1.5 V, can be detected by this circuit. As V_{BE1} is complementary to absolute temperature (CTAT) and $(V_{BE1} - V_{BE2})$ is proportional to absolute temperature (PTAT), different CTAT, PTAT or temperature-independent voltage levels can be built by proper selection of αC and βC capacitors. In order to have a temperature-independent V_L, αC should be modified according to the selected βC capacitor. After fixing αC and βC capacitors, different voltage levels can be detected by modifying the γC capacitor. By detecting the battery voltage between 900 mV and 1.1 V, the remaining charge of the battery can be estimated according to the discharge curve of the target battery [15]. These variable capacitors have been implemented using a matrix of 10 fF metal–insulator–metal (MIM) capacitors that have been used as unity capacitors.

Table 1 Detected voltage levels in the voltage level detector

Voltage level (V_L)	αC capacitor (fF)	βC capacitor (fF)	γC capacitor (fF)
907 mV (V_{EOD})	170	1,230	230
947 mV (V_{L0})	170	1,230	220
1,002 mV (V_{L1})	180	1,300	220
1,051 mV (V_{L2})	180	1,300	210
1,104 mV (V_{L3})	190	1,370	210
1,509 mV (V_{EOC})	160	1,160	130

After measuring the V_{bat} and estimating the energy stored in the battery, the operating frequency of the digital circuits and the bias currents of the analog circuits are reconfigured according to the remaining charge of the battery. In the current-starved ring oscillator in Fig. 3(a), the frequency is determined by R_L and C_L and can be specified as Eq. (2). In Eq. (2), K_1 is a constant value that depends on the number of inverter stages in the ring oscillator [13]. By using a digital resistive trimming network to modify the R_L, F_{osc} is reconfigured by an energy harvesting circuit, according to the measured V_{bat}. When the V_{bat} is low, R_L is increased to decrease F_{osc}. Four target operating frequencies have been considered, corresponding to four voltage levels that are detected by the LD block as shown in Table 1. The minimum operating frequency is 125 kHz which corresponds to the V_{L0}, and the maximum frequency is 1 MHz which corresponds to the V_{L3}.

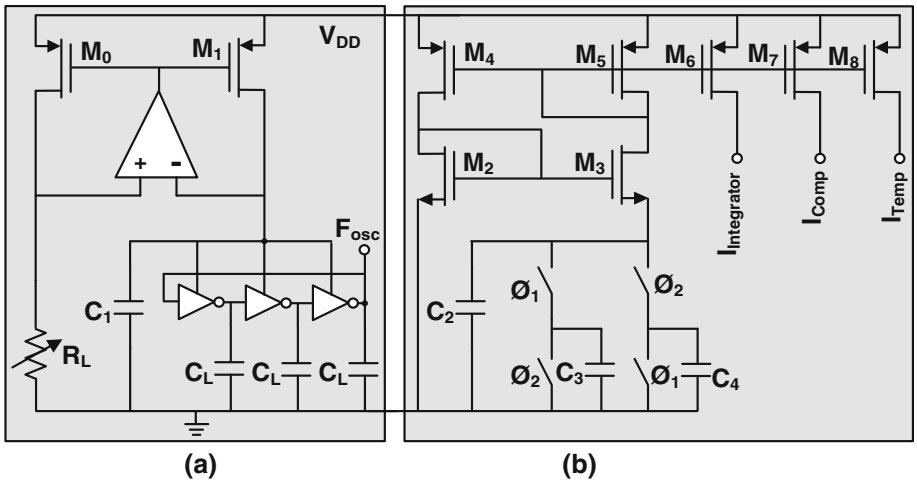

Fig. 3 **a** Reconfigurable current-starved ring oscillator. **b** Switched-capacitor beta-multiplier (SCBM) current source

$$F_{osc} = K_1/(R_L \times C_L) \quad (2)$$

In addition to a fixed 10 nA beta-multiplier (BM) current reference that has been used to provide the required bias currents for PMC, a switched-capacitor beta-multiplier (SCBM) current source has been designed to generate frequency-proportional bias currents for SIC. In this circuit, which can be seen in Fig. 3(b), SC resistors have been used instead of regular resistors to generate frequency-proportional bias currents [18]. For example, $I_{Integrator}$ can be specified as in Eq. (3):

$$I_{Integrator} = K_1 \times K_2 \times F_{osc} \times (C_3 + C_4) \quad (3)$$

In Eq. (3), K_1 and K_2 are constant values that depend on the ratio between the widths of transistors in Fig. 3(b). K_1 depends on the ratio between M_7 and M_4, and K_2 depends on the ratio between M_5 and M_6. The clock frequency F_{osc} is applied to a non-overlapping clock generator to generate non-overlapping $Ø_1$ and $Ø_2$ clock phases. The current ripple of generated bias currents is minimized by using two complementary branches charging and discharging C_3 and C_4 capacitors and using a large decoupling capacitor which is shown as C_2 in Fig. 3(b). As F_{osc} is determined by the oscillator, generated bias currents scale dynamically by changing the frequency of the oscillator. In addition, these bias currents can be easily deactivated by turning off the $Ø_1$ and $Ø_2$ clocks. In the low power analog circuits, such as the discrete time incremental ADC that has been used here, bias currents should be high enough to guarantee correct operation at the target operating frequency. In Fig. 3(b), generated bias currents ($I_{Integrator}$, I_{Comp} and I_{Temp}) have been used for the SIC. When the LD block detects that the V_{bat} is low, the F_{osc} is decreased by modifying the R_L through the digital control unit to reduce the power consumption of the digital circuits. By using these frequency-proportional bias currents, the power consumption of the analog circuits is reduced dynamically when the F_{osc} is decreased.

Table 2 Die area and power consumption of the main blocks in the solar energy harvester circuit

Block	Die area (μm^2)	Active power (nW)	Average power (nW)
Clock generator	14,400	165	165
Digital control unit (DCU)	38,115	90	90
Bias circuit (10 nA)	2,832	35	35
Comparator	759	55	<1 nW
Level detector	31,960	520	<1 nW
SCBM	6,300	640	<1 nW

The digital control unit (DCU) activates the dynamic comparator and LD blocks in a timely manner and updates operating state of the energy harvester circuit according to the received results from these blocks. DCU reconfigures the clock frequency according to the detected battery voltage by LD block. In addition, it turns off the switch between the PV module and the battery when the comparator detects that V_{pv} is less than V_{bat} or LD detects that the battery voltage has reached V_{EOC}. As neither V_{bat} nor V_{pv} change rapidly, these blocks are activated every few seconds and the power consumption of the DCU is mainly determined by the low frequency 20-bits counter that activates the comparator and LD blocks in a timely manner. Table 2 presents the die area and the simulated power consumption of individual blocks, when V_{bat} is high and the system operates at 1 MHz. As can be seen in this table, total power consumption of the circuit is mainly determined by the clock generator, bias circuit and digital control unit, which are always active. Although comparator and LD blocks consume considerable power during their active time, nevertheless, as they are activated every 15 s, their average power consumption is less than 1 nW. When V_{bat} is low, the average power consumption of the clock generator and DCU blocks is reduced by operating at a

Table 3 System performance and power consumption in different system operation modes

System operation modes	S_{L3}	S_{L2}	S_{L1}	S_{L0}
Main characteristics				
Detected V_{bat} during 5CA discharge (mV)	1,104	1,051	1,002	947
Remaining charge of the battery (%)	>80	>50	>35	>25
Battery threshold voltage (v)	1.114	1.055	1.003	0.955
Operating Clock frequency (KHz)	980	502	257	132
Time interval of sensing and data transmission (s)	15	30	60	120
Average power consumption (nW): PMC circuit				
Clock generator	165	85	44	23
Digital control unit	90	46	24	13
Whole PMC circuit	293	169	106	74
Average power consumption (nW): SIC circuit				
Temperature sensor and V_{CM} generator	330	243	198	176
First order incremental ADC	1,030	545	295	180
SAR ADC	5,900	2,840	1,510	790
Average current consumption (μA): whole system				
Sensor bias circuit	4.67	2.34	1.17	0.58
Wireless transceiver	9.4	7.7	6.6	5.55
Complete system	14.1	10.1	7.8	6.2

lower frequency. For example, by reducing the clock frequency to 125 kHz, simulated power consumption of the clock generator and DCU is reduced roughly linearly, reaching to 23 and 13 nW respectively. The power consumption of these two blocks at different target frequencies can be seen in Table 3.

4 Sensor interface circuit

The system level block diagram of the proposed SIC is depicted in Fig. 4. As Pd nanowires are very sensitive to temperature variation, a differential approach has been deployed, in which passivated reference nanowires have been used in addition to sensing nanowires [6]. These nanowires have been represented by NW_{ref} and NW_{sense} in Fig. 4. Individual Pd nanowires have between 7 and 9 KΩ resistances and after getting exposed to hydrogen should be biased with a minimum bias voltage of 50 mV for 10 s, before measuring their conductivity change. A 7 μA current source has been used to bias these sensors. The conductance of NW_{sense} may change by 20 % in comparison with NW_{ref} as H_2 concentration varies from zero to 30 % [4]. The voltage around the reference nanowire ($V_R = V_1 - V_2$) has been used as the reference voltage, while the voltage around the sensing nanowire (V_2) has been used as the input voltage for the following incremental ADC. Although this differential approach eliminates the first order temperature dependence of these nanowires, the second order temperature dependence still exists as the temperature coefficient of these Pd nanowires is temperature-dependent. In order to eliminate these second order effects, temperature is measured after measuring H_2 concentration to be used for further calibration of the sensor. In the proposed integrated temperature sensor, substrate PNP transistors have been used to generate proportional to absolute temperature (V_{ptat}) and temperature-independent reference (V_{ref}) voltages. The ADC converts (V_{ptat}/V_{ref}) to a digital value to measure the temperature. In Fig. 5, by using a 50 fF MIM capacitor as C_1 and a 360 fF MIM capacitor as C_2, a temperature-independent reference voltage of approximately 310 mV has been generated [5]. The accuracy of temperature sensing is mainly limited by mismatch between Q_1 and Q_2 and nonlinearity in temperature dependence of V_{BE1} and ($V_{BE1} - V_{BE2}$). Although these errors can be minimized to reach ±0.1 °C accuracy by using dynamic methods presented in [19], such power-consuming techniques are not needed here. The proposed low power temperature sensor can achieve ±1 °C accuracy by only calibrating C_2 and I_{Temp} at the room temperature [5]. When the whole system operates at a lower frequency, Q_1 and Q_2 transistors are biased with a lower I_{Temp} bias current to reduce the average power consumption of the temperature sensor.

The first order incremental ADC measures H_2 concentration and temperature at different times. The circuit level block diagram of this fully differential ADC has been shown in Fig. 5 for the negative input of the integrator (V_{i-}). In order to measure H_2 concentration, V_2 is used as the input voltage $V_R = V_1 - V_2$ and is used as the reference voltage for the integrator. After initial reset of the integrator and the ADC counter, analog to digital conversion is done in three periods to calculate V_2/V_R. In the first period, $2^{(n-1)}$

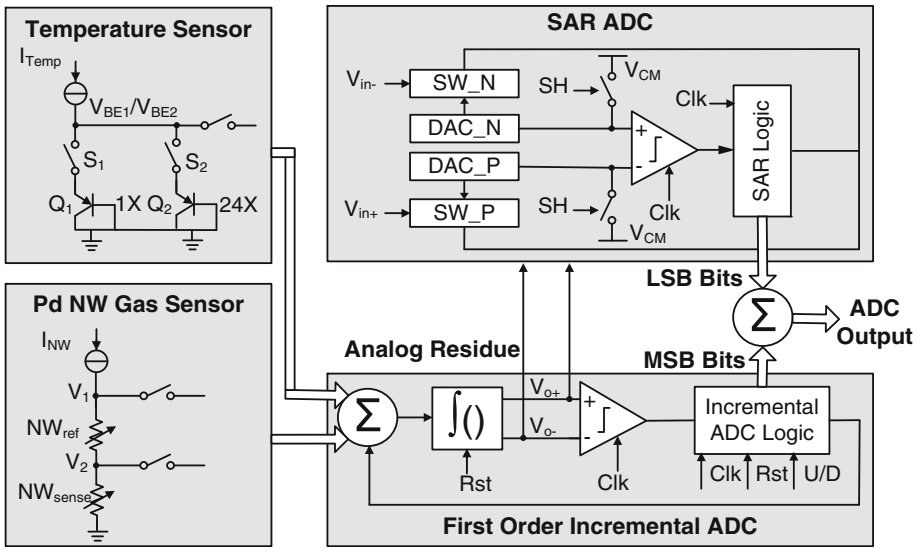

Fig. 4 Circuit diagram of the proposed sensor interface

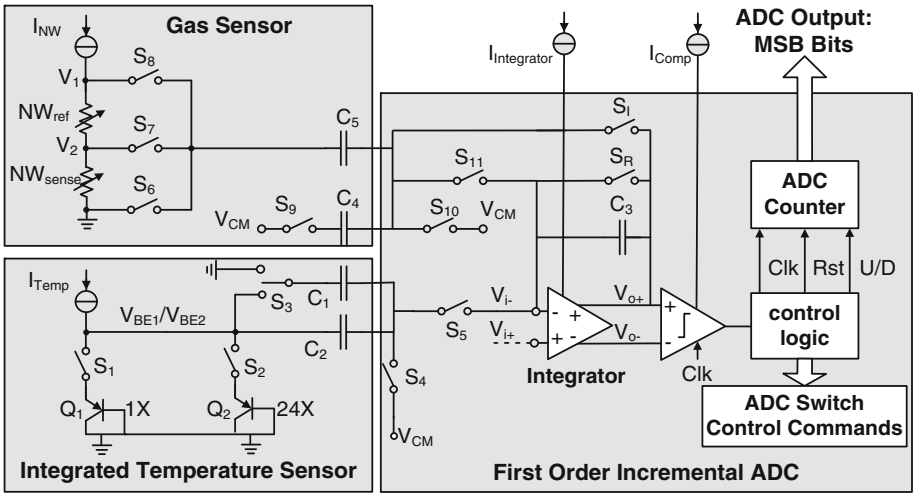

Fig. 5 Circuit diagram of the first order incremental ADC

integration steps are performed, adding $V_2 \times (C_5/C_3)$ to V_{o+} in each integration step. Meanwhile $V_2 \times (C_5/C_3)$ is subtracted from V_{o-} in each integration step and V_{o+} is compared with V_{o-} using a latched comparator. If the output of the comparator becomes 1, $V_R \times (C_5/C_3)$ is subtracted from V_{o+} in the next step and the ADC counter is increased by 1. Similarly, if the output of the comparator becomes 0, $V_R \times (C_5/C_3)$ is added to V_{o+} and the ADC counter is decreased by 1. After these $2^{(n-1)}$ steps, V_{o+} noted as V_{o1+} at the end of the first conversion period will be as Eq. (4) [5]:

$$(V_{o1+} - V_{CM}) = \Delta V_{o1} = (C_5/C_3)[2^{(n-1)} \times V_2 - (N_{S1} - N_{A1}) \times V_R + 2^n \times V_e] \quad (4)$$

In (4), N_{S1} indicates the number of subtractions of V_R and $N_{A1} = (2^{(n-1)} - N_{S1})$ indicates the number of additions of V_R. ADC counter in Fig. 5 is an up/down counter that will contain $N_{S1} - N_{A1}$ at the end of this conversion period. Error introduced by the offset of opamp and charge injection of switches is shown by V_e. In the second period, V_{o1+} is converted to $V_{o2+} = V_{CM} - \Delta V_{o1}$ in 3 steps. V_{o2+} shows V_{o+} at the end of the second conversion period. In the first step, only S_I and S_9 switches are closed, to store $C_4 \times \Delta V_{o1}$ on C_4. Next S_I is opened and S_R is closed to discharge C_3. Finally S_{10} and S_{11} are closed and S_R is opened. Meanwhile S_9 is still closed to connect bottom plate of C_4 to V_{CM}. By closing S_{10} and S_{11}, the top plate of C_4 will be connected to V_{CM} and $-C_4 \times \Delta V_{o1}$ charge will be transferred to C_3. By transferring $-C_4 \times \Delta V_{o1}$ charge to C_3 and using matched capacitors for C_3 and C_4, $V_{o1+} = V_{CM} + \Delta V_{o1}$ is converted to $V_{o2+} = V_{CM} - \Delta V_{o1}$. The third period is similar to period 1, but instead of V_2, $-V_2$ is applied in each integration step, subtracting $V_2 \times (C_5/C_3)$ from V_{o+} in each integration step. Similar to the first conversion period, If the output of the comparator becomes 1, $V_R \times (C_5/C_3)$ is subtracted from V_{o+} in the next step, but this time the ADC counter is decreased by 1 unlike the first conversion period. Similarly if the output of the

comparator becomes 0, $V_R \times (C_5/C_3)$ is added to V_{o+} and the ADC counter is increased by 1. In addition, the initial value V_{o+} is V_{o2+} instead of V_{CM}. After $2^{(n-1)}$ steps, the output voltage of the integrator changes by ΔV_{o2} from initial value of V_{o2+} as can be seen in Eq. 5. V_{o3+} shows V_{o+} at the end of the third conversion period. As can be seen in the Eq. 6, the error term does not appear in the V_{o3+}. In fact as $(C_5/C_3) \times [2^n \times V_e]$ is present in both ΔV_{o1} and ΔV_{o2}, it does not appear in the V_{o3+}. Similarly V_{o-} noted as V_{o3-} at the end of the third conversion period, is calculated for the negative output of the integrator.

$$(V_{o3+} - V_{o2+}) = \Delta V_{o2} = (C_5/C_3)[-2^{(n-1)} \times V_2 - (N_{A2} - N_{S2}) \times V_R + 2^n \times V_e] \quad (5)$$

$$V_{o3+} = V_{o2+} + \Delta V_{o2} = V_{CM} - \Delta V_{o1} + \Delta V_{o2} = (-C_5/C_3)[2^{(n)}.V_2 - (N_{S2} + N_{S1} - N_{A2} - N_{A1}) \times V_R] \quad (6)$$

$$(V_2)/V_R = \left(\frac{N_{S1} + N_{S2} - N_{A1} - N_{A2}}{2^n}\right) - \left(\frac{(V_{o3+} \times C_3}{V_R \times C_5}\right) \times \left(\frac{1}{2^n}\right) \quad (7)$$

The value stored in the ADC counter at the end of the third period is $N_{OUT} = (N_{S1} + N_{S2} - N_{A1} - N_{A2})$. As the difference between (V_2/V_R) and $(N_{OUT}/2^n)$ in Eq. (7) is less than $(1/2^n)$, N_{out} is the n-bit digital representation of (V_2/V_R). Conversion accuracy of this ADC is affected by noise, finite opamp gain and nonlinearity of the capacitors [9]. This ADC can achieve 13 bits resolution by using 200 fF MIM capacitors, as C_3, C_4 and C_5, and a conventional two-stage amplifier with at least 85 dB gain for the integrator [9]. A resistive divider has been used to generate the required V_{CM} for ADC that consumes 150 nW during conversion. As a 1 MHz clock has been used for this first order incremental ADC, a 13-bit conversion takes nearly 8 ms [20].

The main disadvantage of this first order incremental ADC is its long conversion time that further increases the energy per conversion of the ADC. In order to reduce the conversion time, either higher order delta-sigma modulators can be used or additional bits can be extracted from the analog residue of this first order incremental ADC [20]. V_{o3+} and V_{o3-} are analog residues of the first order incremental ADC that are sent to the SAR ADC to extract additional bits. In fact, as the analog residue in the first order incremental ADC is the quantization error that has been multiplied by 2^N, additional bits can be extracted from this analog signal by an additional ADC. For example, in [21], the same comparator and integrator have been reused as an algorithmic ADC to extract additional bits from the analog residue of this ADC. In [22], not only a higher order modulator delta-sigma has been used, but also an additional successive approximation register (SAR) ADC has been deployed to extract additional bits from the analog residue.

In the proposed circuit, an additional SAR ADC has been used besides the initial first order incremental ADC to improve energy consumption per conversion of the ADC. In this circuit, the original first order incremental ADC is used to extract 5 most significant bits in 32 clock cycles and the analogue residue of this fully differential incremental ADC $(V_{o+} - V_{o-})$ is applied as the V_{in+} and V_{in-} inputs of the following SAR ADC to extract additional 8 least significant bits (LSB). This ADC can be an ideal candidate for sensing applications as it can achieve high accuracy, close to delta-sigma and dual-slope ADCs and low energy per conversion, close to SAR ADCs. In addition, the die area is reduced by scaling down the capacitors thanks to oversampling. Although SAR ADCs have the best performance in terms of energy per conversion, they are not appropriate for high resolution applications. SAR ADCs enable energy-efficient analog-to-digital conversion for applications with moderate speed and resolution demands thanks to using a few number of active circuit elements. As these active elements do not consume static power, power consumption scales linearly with the frequency. The main blocks of the proposed SAR ADC can be seen in Fig. 6 for the negative input of the ADC. DAC_N and SW_N refer to the DAC and the switches that have been used for the negative input. Similar blocks have been used to realize SW_P and DAC_P blocks for the positive input of the SAR ADC. The mismatch of the capacitors in the charge distributed DAC is the main limiting factor for the resolution and the unit capacitor of the DAC is defined by the matching property of the target MIM capacitors. By increasing the resolution, not only a larger unit capacitor is required to satisfy the matching requirements, but also the size of the biggest capacitor in the DAC should be doubled for an additional resolution bit. As the size of the capacitors in the DAC block highly affects the die area and power consumption of the SAR ADC, different DAC topologies including split array DACs have been proposed to minimize the die area [23]. In fact, for relatively low resolutions (6–8 bits), the area of the SAR ADC can be quite small as a split capacitor array can be deployed to realize the DAC. As can be seen in Fig. 6, two sub-DACs, each with 4-bit resolution and a fractional bridge capacitor has been used to implement an 8-bit DAC. In this architecture the total sizes of the capacitors have been reduced, but on the other hand, the achievable resolution is limited as the attenuation capacitor is floating with non-equal parasitic capacitors at top and bottom plates. However in modern technologies, the parasitic capacitors of the top and bottom plates have better matching and 8-bit resolution is achievable with modest area and power consumption. By using 100 fF MIM capacitor as capacitor C in Fig. 6 and careful layout of the capacitor array to avoid linearity degradation

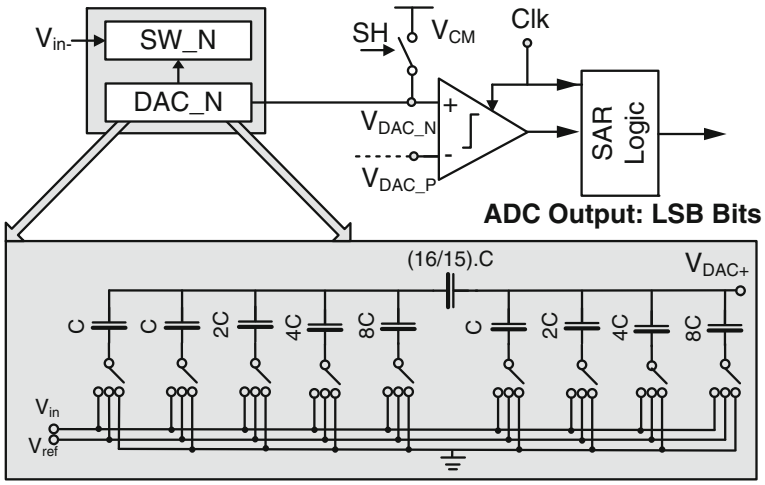

Fig. 6 Circuit diagram of the implemented SAR ADC

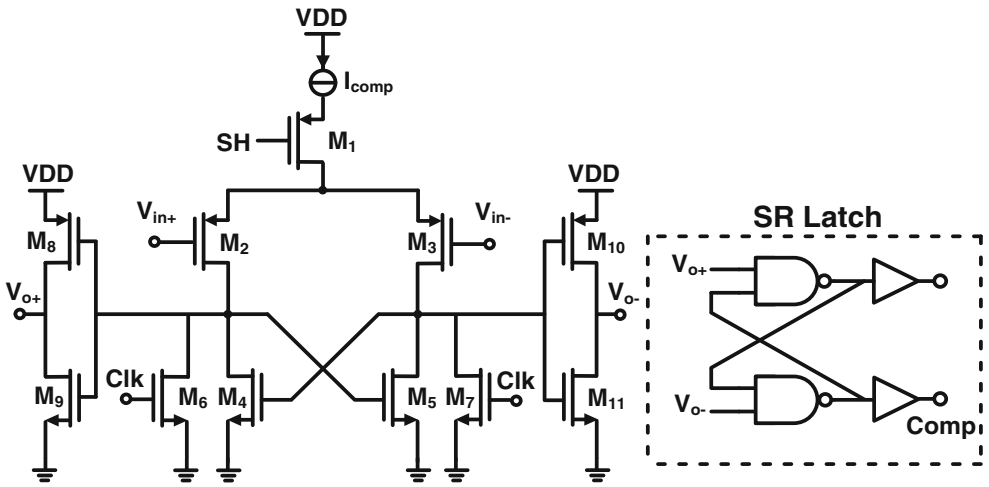

Fig. 7 Circuit diagram of the latched comparator

due to non-equal parasitic capacitors at the bottom and top plates of the attenuator capacitor, an 8 bits SAR ADC has been implemented that consumes 5.9 μW operating at 1 MHz clock frequency.

In this SAR ADC, initially SAR Logic block sets the SH signal to sample the differential input signal on the bottom plate of the DAC capacitors. During this sampling phase, the inputs of the dynamic comparator are reset to the common-mode voltage. Conversion starts at the falling edge of the SH and last for eight clock cycles. After these 8 cycles the SAR logic output is ready and it can be used as 8 LSB bits of the ADC output. The circuit schematic of the dynamic voltage comparator is shown in Fig. 7. This latched comparator has been used for both first order incremental and SAR ADC blocks in Fig. 4. The SH signal is high during the sampling phase and the outputs of the comparator that are shown as V_{o+} and V_{o-} in Fig. 7 are pre-charged to the supply voltage. The SR latch located at the output of the comparator preserves the last decision result. The bias current is disabled during the sampling phase that SH signal is high. The preamplifier's outputs are discharged to ground to initiate the next conversion cycle. On the falling edge of clock, positive feedback in the preamplifier stage updates V_{o+} and V_{o-}, depending on the difference between V_{in+} and V_{in-}. As the comparator is the only active building block in the SAR ADC, in low speed applications the power consumption of the comparator is the dominant factor. As frequency-proportional current source from SCBM has been used for the comparator, by operating at lower frequencies, the bias current of comparator is reduced to minimize the power consumption of both incremental and SAR ADC.

5 System integration and performance

The circuit has been implemented in a 0.18 μm CMOS process with 0.25 mm^2 total area, as can be seen in Fig. 8. The main blocks, including the digital blocks and the analog blocks of the solar energy harvester and the SICs

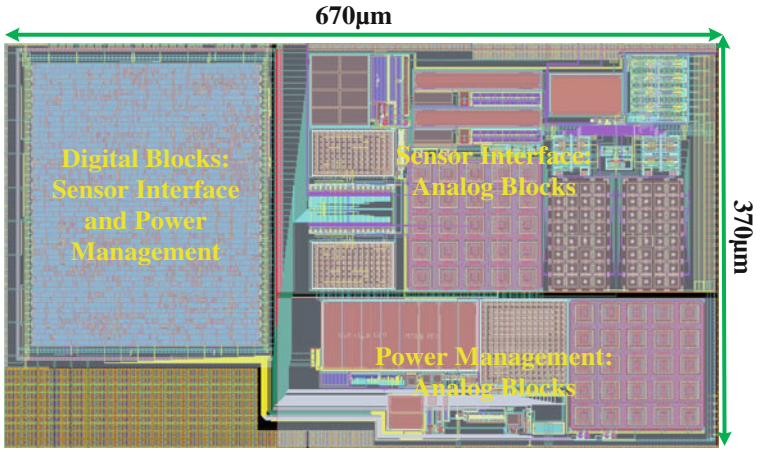

Fig. 8 Circuit layout of the whole microsystem

have been specified separately in this layout. Highly resistive poly resistors have been used as embedded resistors in the beta multiplier current source and oscillator. As these embedded resistors are sensitive to process variations, they are trimmed initially.

Table 3 presents simulation results for power consumption of the power management and the SICs in different system operation modes. These operation modes have been defined according to the remaining charge of the battery. In order to accurately estimate the remaining charge of the battery, the V_{bat} is detected when the battery is discharged by a high current during wireless data transmission. After detecting the V_{bat}, Battery discharge capacity is determined according to the discharge curve of the battery [8]. In S_{L3} mode, the system operates at 1 MHz and the wireless transceiver sends the measurement results for H_2 concentration and temperature to a base station every 15 s. In this operation mode, the average power consumption of the energy harvester is less than 300 nW. By detecting a lower battery voltage, the system is switched to a lower clock frequency to decrease the average power consumption of the whole system. For example, in S_{L0} mode that the remaining charge of the battery is low, the circuit operates at 125 kHz frequency instead of 1 MHz and the average power consumption of the energy harvester drops to less than 110 nW thanks to reduction in the power consumption of the clock generation and DCU blocks. By operating at 125 kHz frequency, the average power consumption of the incremental and SAR ADC is reduced almost linearly as can be seen in Table 3. In addition, in this mode, measurement results are sent every 120 s instead of every 15 s in S_{L3} mode, to further reduce the total average power consumption of the whole sensor. An additional 330 nW is used for biasing the BJT transistors in the integrated temperature sensor and generating V_{CM} common mode voltage for ADC in S_{L3} mode that is reduced to 173nW in S_{L0} mode. As a resistive divider has been used to generate V_{CM}, the power consumption of the V_{CM} generator is almost constant; however as a frequency-proportional current source has been used to bias BJT transistors in the temperature sensor, the power consumption is reduced in S_{L0} mode.

In order to estimate the total power consumption of the sensor, the average power consumption of the sensor biasing circuit and the wireless transceiver should be calculated. Pd nanowires should be biased with a 7 µA bias current for 10 s, before measuring H_2 concentration. As the ADC conversion takes less than 1 ms, even when operating at 250 kHz, total power consumption of the SIC is mainly determined by the power consumption of the sensor bias circuit. TZ1053 consumes 5 µA during standby and consumes 3.3 mA during a period of 20 ms to send a sample with the minimum payload size of 55 bytes [12]. In S_{L3} mode, samples are sent every 15 s, and the average current consumption of the Pd nanowires and the wireless transceiver are 4.67 and 9.4 µA, respectively. By sending the samples every 120 s in S_{L0} mode, these values will be reduced to 0.58 and 5.6 µA, respectively. The average current consumption of the whole sensor is 14.1 µA in S_{L3} mode that is reduced to 6.2 µA, operating in S_{L0} mode.

Four nanowire solar cells presented in [7] have been connected in series to provide an appropriate V_{mpp} voltage, close to the V_{EOC} of the Varta V6HR NiMH battery. The power delivered to the battery by the PV module can be simulated using the equivalent circuit model of the PV module. This PV module, with the total area of 28 mm^2, can provide a maximum power of 2.88 mW at its V_{mpp} under AM1.5 illumination level [7]. In order to evaluate autonomous operation of the sensor, end-to-end efficiency from the PV module to the battery has been evaluated in different illumination levels. In 100 % illumination level, 2.24 mW is delivered to the battery and 82 % efficiency is achievable [15]. As V_{mpp} does not change significantly, efficiency remains high, even under reduced illumination levels. In order to evaluate autonomous operation of the sensor, the power that can be delivered to the battery in

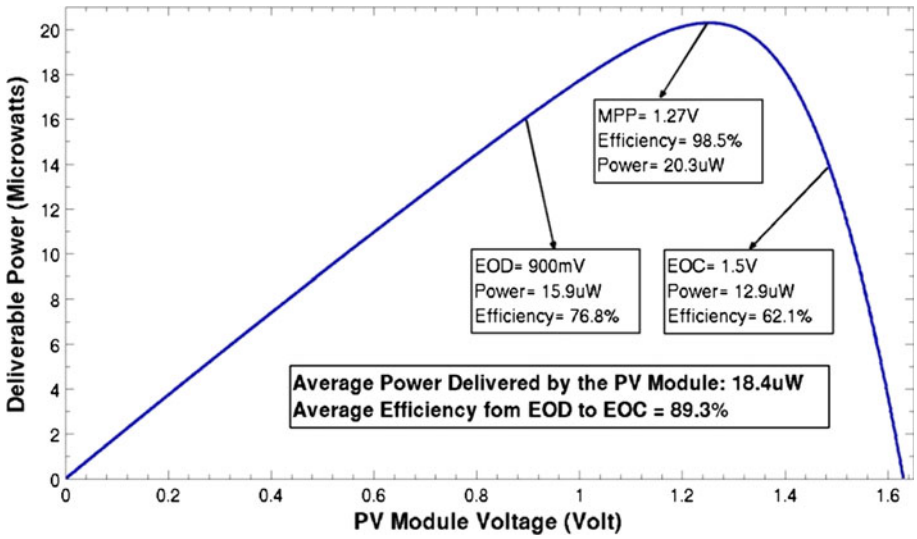

Fig. 9 Power delivered to the battery under simulated 1 % of AM1.5 illumination

1 % illumination level has been simulated and shown in Fig. 9. During battery charging, the PV module delivers an average power of 18.4 μW to the battery with 89.8 % average efficiency. When the battery is almost fully discharged, V_{bat} is close to V_{EOD} and the system is operating in S_{L0} mode. During this period, 15.9 μW is delivered to the battery with 76.8 % efficiency as can be seen in Fig. 9, while the average power consumption of the complete system is only 6.2 μW. As a result the battery gets charged and V_{bat} increases gradually. By increasing the battery voltage, efficiency is improved and more power is delivered to the battery. So even in 1 % light intensity, the harvested energy is enough for autonomous operation of the complete system. Meanwhile, as the whole sensor consumes 14.1 μA for sensing and data transmission, the target 6 mAh battery can provide enough power for approximately 425 h operation, even without energy harvesting.

6 Conclusions

An UIP energy-efficient solar energy harvesting and sensing microsystem has been proposed to realize an autonomous wireless hydrogen sensor. The circuit has been implemented in a 0.18 μm CMOS process with 0.25 mm^2 active die area. An area- and power-efficient solar energy harvester has been proposed that stores the energy harvested from the PV module in a NiMH microbattery. In addition, this PMC scales the power consumption and performance of the complete system to guarantee autonomous operation of the sensor when the remaining charge of the battery is low. This circuit scales up or down the operating frequency of digital circuits and bias currents of the analog circuits to reconfigure the active power consumption of the individual blocks. In addition, by scaling the clock frequency, the time interval of sensing and data transmission is reconfigured dynamically. The PMC consumes only 300 nW, when operating at 1 MHz as its highest speed, which is further reduced to less than 110 nW when the clock frequency is reduced to 125 kHz. A fully integrated SIC measures H_2 concentration by measuring the conductance change of a miniaturized palladium nanowire sensor. As these Pd nanowires have temperature cross-sensitivity, temperature is also measured using an integrated temperature sensor for further calibration of the sensor. An innovative incremental ADC converts the measurement results to 13-bit digital values and the measurement results are transmitted to the base station, using an external wireless transceiver. Simulation results show that even under 1 % light intensity, the harvested energy is enough for autonomous operation of the whole system. Meanwhile, as the sensor consumes 14.1 μA for sensing and data transmission, the target 6 mAh battery can provide enough power for approximately 425 h operation, even without energy harvesting.

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