

An ultra low-voltage low power PSK backscatter modulator for passive UHF RFID tags compatible with C1 G2 EPC standard protocol

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Received: 29 January 2013 / Revised: 5 May 2013 / Accepted: 3 September 2013 / Published online: 24 September 2013
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Abstract Reducing the power consumption of a passive radio frequency identification (RFID) tag is the key in many applications. As the modulator is usually the most power-hungry block in an RFID tag, this paper proposes a power-saving modulator. The proposed modulator uses phase shift keying (PSK) backscatter modulation which allows tag to communicate data from its memory to a reader by PSK modulation. The proposed modulator uses a MOSCAP as a variable impedance and is designed in a new one-inverter structure in compare to the conventional varactor-based modulators designed in two-inverter structure, as this modulator needs just a low voltage swing to drive its MOSCAP. Using MOSCAP as the variable capacitance leads to a low voltage design. Also, the fundamental equations required for determination of the capacitive impedance seen by the antenna is presented. This impedance is the master key in modulator design. The modulator has been designed, simulated and optimized in 0.18 μm CMOS technology. All possible simulation results are presented to approve its compatible operation with C1 G2 EPC global standard. The power consumption of less than 46 nW is achieved in all process corner cases at 0.8 V power supply.

Keywords Passive UHF RFID tag · Phase shift keying (PSK) · Backscatter modulation · Power reflection coefficient · MOSCAP driver · Miller encoding

1 Introduction

Nowadays, applications of radio frequency identification (RFID) technology are extended from simple ones, such as monitoring and management systems for buildings, through more sophisticated ones, such as open-air events or logistics [1]. All of those are wireless sensing applications, and need ultra low power IC design, wide system reading range, and a small tag size [2].

In some applications, which operating range is of prime importance compared to power consumption and tag size, active tags are used. As the power is provided by an external battery, the tag size is large. Passive tags have less operating range compared to active ones. However, they are very power efficient and can be built in small sizes. To overcome the problem of short operating range, passive tags are usually used at high frequencies, such as UHF band, which are available worldwide. High frequency operation results in reducing antenna length and allows tags to be designed in very small sizes. The main concern in passive UHF RFID tag design is reducing the power consumption to increase the operating range as much as possible. As a passive tag obtains its power from the incoming reader RF carrier signal, and not a battery, designing some simple and low power circuits, which can work with such small power, is an important but complicated issue. To achieve a low power design, many researches are done on RF-to-DC block, or on some different technologies, such as silicon on sapphire (SOS) [2], organic thin film transistor (OTFT) [3], or silicon on isolator (SOI) [4]. However, those technologies are expensive, and therefore, low power circuit design techniques in CMOS technology are usually considered for power reduction in power hungry blocks. One of the most power consuming blocks in a passive tag is modulator, which is transmitter of

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the system that sends the tag information to the reader [5]. It typically consumes more than 50 % of the total available power.

Passive tags use different types of modulation for the downlink (tag to reader). They use load modulation when the distance between the tag and the reader is short. In such a modulation type, tag and reader are coupled by an electromagnetic inductance. Current of the reader coil generates a magnetic field, which induces current in the tag's antenna coil, so data is sent by the carrier signal. This type of modulation is suitable for low frequencies up to 13.56 MHz. However, to increase the frequency range and subsequently operating range, that is the distance between tag and reader, backscatter modulation is used. This technique is based on the variation of the reflection coefficient at the input of the tag [6] which can vary either in amplitude or in phase. As a result, by varying the amplitude, amplitude shift keying (ASK) modulation is achieved and varying the phase leads to phase shift keying (PSK) modulation. In backscatter modulation, load impedance seen by the tag's antenna varies, and therefore leads to transmit data. Ideally, in one state, for example off state, this impedance is totally matched with the antenna impedance, which means that the load impedance is complex conjugate of the antenna's impedance, and no power is reflected back to the reader. In the other state, i.e. on state, there is an impedance mismatch between tag's antenna and load, so some part of power comes back to the reader and just a small part is absorbed. Therefore, reader can distinguish data by the amount of the reflected power.

According to the above explanations, realization of backscatter modulation is almost equivalent to design variable impedance. A simple RFID tag with ASK/PSK modulator is shown in Fig. 1. By varying the real part of the impedance, amplitude of reflection coefficient will change and data will be modulated on the signal amplitude. This leads to ASK modulation, which can be easily achieved by a MOS switch in series or in parallel with a resistor [1]. Moreover, by varying the imaginary part of the impedance seen by the antenna, phase variation is created between incoming and reflected signals, which results in phase variation of reflection coefficients and consequently, PSK modulation is achieved.

PSK modulation realization is more complex than ASK, as it changes the imaginary part of the impedance, which typically obtained by varying a capacitive impedance [7]. Varying inductive impedance is not a good option as inductors occupy large die area which is not compatible with RFID aim as a cost-efficient technology. Therefore, a voltage variable capacitance is a good choice to implement the PSK backscatter modulator, as most of the previous works used it [1, 7, 9].

Although PSK modulators need driver circuits to produce required voltage for variable capacitance, which leads

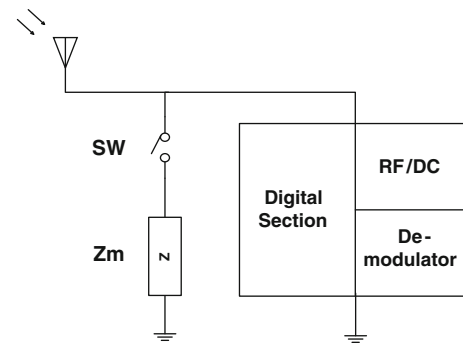


Fig. 1 ASK modulated passive RFID system [8]

to more power consumption than ASK modulators, there is two important issues which give PSK modulation an advantage over ASK. First, the delivered power to the tag is constant during the two modulation states in PSK modulation; therefore, power management is more convenient. Also, for a given modulation depth, a larger power is transferred to the tag during PSK modulation compared to ASK [7], and this power is the critical quantity limiting the range of passive systems.

Therefore, this paper presents a low-voltage low-power PSK backscattering modulator for passive tags. To design and analysis such modulator, a comprehensive circuit-mathematical method is also presented. The rest of paper is organized as follows. In Sect. 2, the proposed method is presented in details and based on that, the required capacitance variation at the antenna end is obtained. In Sect. 3, MOS-varactor as the most prevalent variable capacitance and MOSCAP are compared and the best is chosen for our desired application. The proposed structure for required variable capacitance and its driver circuit as the modulator is discussed in Sect. 4. Different simulation results of the proposed PSK modulator are shown in Sect. 5, and finally, the conclusions are given in Sect. 6.

2 PSK modulator design

One of the most prevalent methods in impedance analysis for backscattering modulation and modulator design is power reflection coefficient method using Kurokawa method. To find the power reflection coefficient between two complex impedances in this method, the combination of an impedance function and Smith chart is used [10] and to design a PSK modulator, a suitable reflection coefficient, exact tag input impedance and the antenna impedance is required. The exact amount of tag input impedance is related to RF-to-DC block structure specially rectifier; so, the complete designed RF-to-DC block is needed.

In this section, a simple method is proposed to find the required impedance in two different modulation states

without any need to know the RF-to-DC block configuration. This new method is based on basic characteristics of PSK modulation and the result is totally compatible with the result of Kurokawa method. However, it has no complexity and no need to know the tag input impedance or power reflection coefficient.

2.1 Proposed method

One of the PSK modulation advantages compared to ASK modulation is more power transmission to the tag. To have maximum power transmission in a network, source and load impedances should be totally matched. In an RFID tag, source and load impedances are the antenna and the tag input impedances, respectively. The modulator is used as the matching circuit. A simplified equivalent circuit of tag, antenna and the modulator is shown as Fig. 2.

The Thevenin equivalent voltage source E_a and impedance Z_a are the equivalent circuit of the antenna [11]. The Z_a is composed of the radiation resistance R_a in series with the inductance L_a . The tag chip is represented as a resistor (R_T) in parallel with a capacitance (C_T). This impedance is approximately the rectifier input impedance, as other blocks are off in transmitting data mode. C_T is the rectifier capacitance in parallel with parasitic capacitance of demodulator and other blocks which can be neglected in comparison to the modulator variable capacitance. Modulator is also shown as a black box.

To receive and extract data more easily in reader end, the modulation angle should be as much as possible (180° in ideal). This means that phase variation between transmitted power to the reader in two modulation states should be 180° . Therefore, the impedance seen by the antenna in two modulation states (Z_1, Z_2 in on and off states, respectively) should be complex conjugate as (1);

$$Z_1 = Z_2^* \tag{1}$$

So, Z_1 and Z_2 should have the same magnitude as (2);

$$|Z_1| = |Z_2| \tag{2}$$

To have two complex conjugate impedances, inductive impedance is required, but inductive elements occupy more

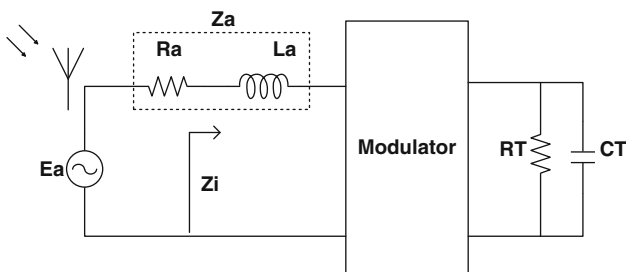


Fig. 2 A simplified equivalent circuit of an RFID tag

die area. Fortunately, inductance could be obtained by suitable antenna design (L_a in Fig. 2). Therefore, L_a and modulator impedance are considered as the matching circuit to match real part of the antenna impedance (R_a) to the complex tag antenna (Z_T). Based on this consideration, four different configurations for matching circuit and modulator implementation are provided which shown in Fig. 3 [6].

The use of PSK has another advantage that power delivered to the tag is approximately independent of modulation state, simplifying power management (6). This means that the magnitude of power reflection coefficient should be the same in two modulation states as (3);

$$|\Gamma_1| = |\Gamma_2| \tag{3}$$

Power reflection coefficient is the ratio of backscattered power to the antenna and the scattered power from the antenna, and is defined as (4);

$$\Gamma = \frac{Z_i - Z_s^*}{Z_i + Z_s} \tag{4}$$

Z_s is the source impedance (the antenna impedance) and Z_L is the load impedance (the tag impedance) in a network. By knowing two requirements for PSK modulator design, it is just needed to choose the best configuration from Fig. 3 for modulator structure. In PSK modulation, the imaginary part of the impedance is changed. However, it is obvious from (3) that it should not change the input signal amplitude, in order to deliver constant power to the tag in two different modulation states. Investigating (2) in Fig. 3 shows that the configurations (3a) and (3d) do not fulfill these requirements. Therefore, (3b) and (3c) are the possible configurations for the implementation. For more simplicity, series-series configuration is chosen. The final equivalent circuit of the tag, antenna and the modulator is shown in Fig. 4. The tag input capacitance (C_T) is combined with modulator for simplicity, as it is totally negligible compared to modulator capacitance.

2.2 Series-series configuration

In the following, the required variable capacitance is calculated using series-series configuration, as shown in Fig. 4. When the modulator is in off state, the capacitance is C_1 and in on mode, it is C_2 . The difference between capacitances during the two modulation states is shown by ΔC . Input impedance seen by the antenna is;

$$Z_i = L_a j\omega + \frac{1}{C_j \omega} + R_T \tag{5}$$

Fig. 3 Possible backscatter modulator schematics [6]

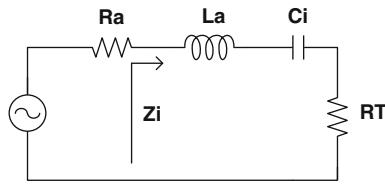
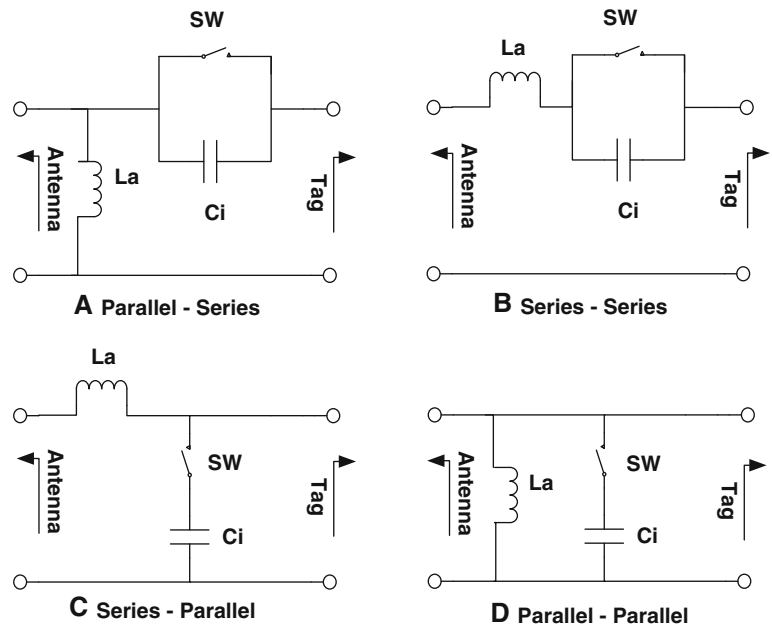


Fig. 4 The series-series configuration of a PSK modulator

To fulfill (2);

$$\left| L_a j\omega + \frac{1}{C_1 j\omega} + R_T \right| = \left| L_a j\omega + \frac{1}{C_2 j\omega} + R_T \right| \tag{6}$$

This equation has two different responses. One of them is equality of C_1 and C_2 , which is not desirable. The desirable answer is (7);

$$2L_a j\omega^2 = \frac{C_1 + C_2}{C_1 C_2} \tag{7}$$

To have a constant reflection coefficient in the two modulation states as (3), it is assumed that capacitance in on state is ΔC and there is no capacitance in off state. It just simplifies the equations and has no effect on circuit operation. By using (4) and (5) and this simplified assumption, ΔC is obtained as (8);

$$\Delta C = \frac{1}{2L_a \omega^2} \tag{8}$$

By assuming a 100 nH inductor, which is achieved easily by antenna design at frequency of 900 MHz, the required capacitances are calculated as, 252 and 408 fF, respectively. Therefore, designing this variable capacitance is the second design priority.

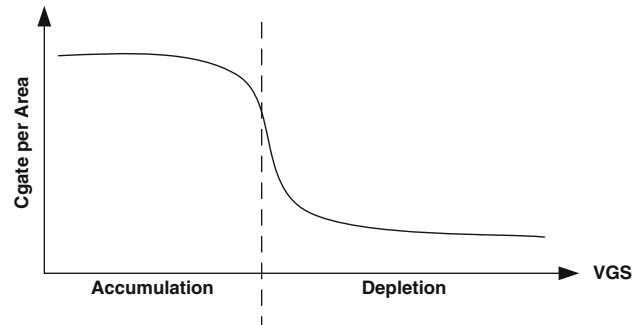


Fig. 5 C–V characteristics of a NMOS-varactor

3 MOS-varactor versus MOSCAP

In most of former reported PSK modulators, a MOS-varactor is used as the variable capacitance. Varactor is a voltage variable capacitance which has a C–V characteristic as shown in Fig. 5. MOS-varactor is an NMOS (PMOS) transistor made in Nwell (Pwell), with the source and drain terminals connected together, so there is no inversion mode in operational modes and it just works in accumulation or depletion region. This feature allows the varactor to achieve a wide range of capacitance.

MOSCAP is another type of voltage-variable capacitance. Generally, the MOSCAP is a normal NMOS (PMOS) transistor, made in Pwell (Nwell), and its source and drain terminals are also connected together; therefore, it has three operational regions. For an N-MOSCAP, positive voltage on the gate is corresponded to the inversion region. The gate voltage (V_G) less than the threshold voltage leads to depletion and negative voltages result in accumulation. An assumption is that the gate oxide has

only small numbers of trapped charges or defects [12]. The basic model of an N-MOSCAP is illustrated in Fig. 6.

As the substrate is P-type, by applying negative voltage to the gate, the majority carriers, i.e., holes, will be attracted to the silicon interface and accumulate under the gate oxide. Now, if the small signal capacitance of the structure is measured, it will be simply the gate oxide capacitance which is independent of the V_G . Positive voltage will repel the holes from the surface creating a depletion region under the gate oxide. Now the capacitance is the gate oxide capacitance in series with the capacitance of the depletion region. As positive voltage increases, the width of depletion region is increased, which leads to reduction of depletion capacitance. Therefore, the total capacitance is decreased, too [12]. Finally, in a definite voltage level, the width of depletion region and consequently, the total capacitance will be constant. For operation frequencies higher than 1 MHz, the minority carriers in common surface of Si/SiO₂ will not be modulated by small signals, as the minority carriers do not have enough time to reach the surface. Therefore, it is expected that by increasing the V_G , the gate capacitance will stay constant. However, something different will be happened and the MOSCAP will work in inversion mode and it is just because of the existence of carrier injection sources (drain and source) in the vicinity of the channel which inject electrons to the channel. Since, gate capacitance will back to the initial value, which is gate oxide capacitance. The same C–V characteristic will obtain in low frequencies. In such frequencies, the charge of channel will be obtained by the source and drain as well as by substrate. Therefore, the C–V characteristic of an N-MOSCAP is ideally shown in Fig. 7.

Although this capacitance is totally nonlinear in a range near the threshold voltage, it is usable for our design as we do not need a linear capacitance. It is just important to choose the drive voltage of MOSCAP far away from the nonlinear zone. Because of lower required amplitude voltage variation for MOSCAP than varactor for the same

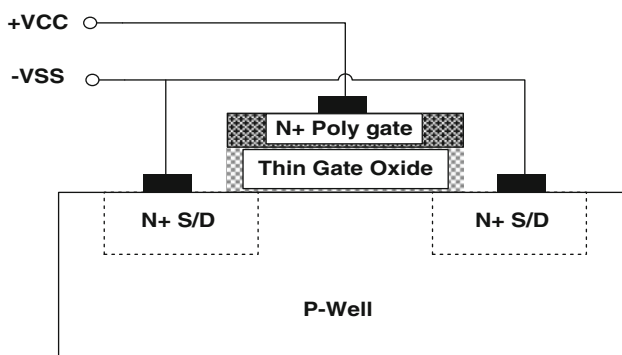


Fig. 6 The basic model of a N-MOSCAP

capacitance variation, we choose the MOSCAP as the required variable capacitance for modulator design, instead of varactor that is used in conventional modulators.

4 Proposed structure

To obtain the required capacitances with a low tolerance around the drive voltage, the drive circuit has to be designed in such a way that drives the MOSCAP in strong and weak inversion modes, which have almost constant capacitances (as Fig. 7) and have enough variation in this range to fulfill the required impedance variation. Therefore, the exact C–V characteristic of a reference-size MOSCAP is needed for the design.

A NMOS transistor with 160 μm^2 gate area is chosen as a reference and the C–V characteristic is plotted in all frequency ranges compatible with EPC global standard [12], 40–640 kHz. However, this characteristic is totally independent of the operation frequency, as explained in Sect. 3. The C–V characteristic of reference N-MOSCAP at 40 kHz is plotted in Fig. 8.

By driving the MOSCAP in weak and strong inversion regions at approximate voltages 0.2 and 0.7 V, respectively, the capacitance will change between 0.33 and 1.29 pF.

The capacitive equivalent circuit of the modulator and the antenna is shown in Fig. 9. C_1 is the variable modulator capacitance and C_a is the constant capacitance which connects modulator to the antenna. So, by knowing the amount of the capacitances seen by the antenna in two modulation states (Sect. 2.2), the amount of required constant capacitance (C_a), and the ratio of desired MOSCAP sizing to the reference MOSCAP are achieved 0.52 and 1.45 pF, respectively. So, the gate area of the required MOSCAP is 232 μm^2 and the capacitance of the MOSCAP should be changed between 0.48 and 1.88 pF.

To achieve these capacitances, a driver circuit is needed to produce desired voltage levels. In some former literatures such as [1], a 2-inverter structure is used to achieve two desired voltage levels, $\pm V_{DD}$, to drive a MOS-varactor. These voltage levels are high and lead to more power consumption (based on $P = CV^2f$). As this paper uses MOSCAP instead of varactor, needs just a low voltage signal that can be achieved by a simple inverter. So, the proposed structure uses an inverter, a very simple driver circuit, to produce the required voltage levels at the gate of MOSCAP to charge and discharge it. This low voltage signal is the advantage of MOSCAP in regards to MOS-varactor which leads to less power consumption of MOSCAP structure compared to the varactor structure. It is worth mentioning that as the driver circuit need just about 0.2 and 0.7 V signals to drive the MOS-capacitance, it can

Fig. 7 C–V characteristics of a N-MOSCAP

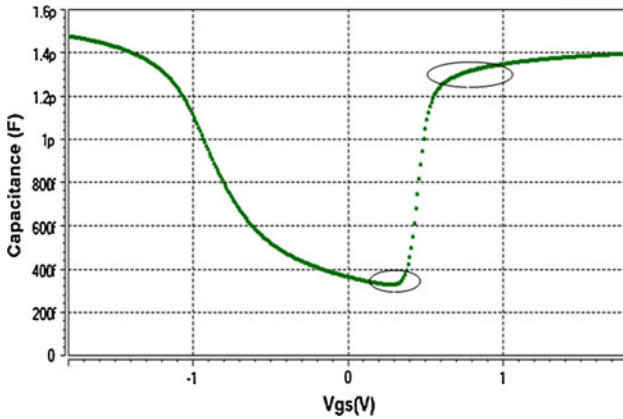
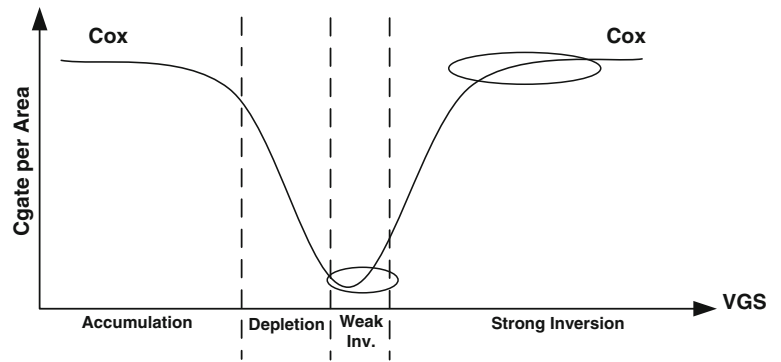


Fig. 8 C–V characteristics of reference N-MOSCAP

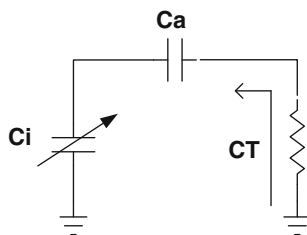


Fig. 9 Capacitive equivalent circuit of the modulator

be biased with a power supply lower than common power supplies in 0.18 μm CMOS technology. The power supply of the proposed modulator is 0.8 V, which leads to more power reduction.

Meanwhile, a level converter is needed to change the output signal levels of control logic (0, 0.4 V) to power supply levels (0, 0.8 V). Although, this level converter can be the conventional cross level converter, the proposed modulator uses two-transistor structure because of less occupied area than cross one.

In modulator design, it is necessary that in ideal, no fraction of the power at the antenna comes back to the modulator. It means that all available power at the antenna goes to the RF-to-DC converter in downlink (tag to reader) to have a higher efficiency and therefore better

performance. However, it is practically impossible because of the modulator output resistance. So, it is necessary to design the modulator with a large enough output resistance in comparison to the antenna radiation resistance; therefore, a negligible fraction of the power at the antenna goes to the modulator as required for the correct operation of the tag [7]. The schematic of the proposed modulator is shown in Fig. 10. M_R is an NMOS transistor biased in triode region and its drain–source resistance is the output resistance of the modulator.

Transistors MLC_p and MLC_n work as a level converter which standardizes the incoming digital signal, (0, 0.4 V), from the control logic. Therefore, a signal with level 0 and V_{DD} is achieved as the modulator input signal at node INV. M_1 is the MOSCAP. Inverter transistors, M_n and M_p , are the base of the modulator. The charging and discharging current of the output capacitance of the inverter and also the capacitance of MOSCAP are controlled by two diode connected transistors (MB_p and MB_n) at the source of M_n and M_p . These are the driver transistors which determine the effective resistance at the source of M_n and M_p . These elements determine the time constant of charging and discharging of the MOSCAP and also the output capacitance of the inverter. By neglecting the output capacitance of the inverter in comparison to the MOSCAP, it is enough to determine the resistance to find the delay and time constant. Increasing channel length of driver transistors results in higher resistance. The transistors' length should be large enough to be able to charge and discharge the MOSCAP at a wide data rate range, from 40 kb/s to 640 kb/s.

5 Simulation results

The whole circuit is simulated in a 0.18 μm CMOS technology. The proposed PSK modulator is evaluated using a data stream {000...} which is encoded by FM0 baseband encoding and coming from the control logic.

Fig. 10 Schematic of the proposed PSK modulator

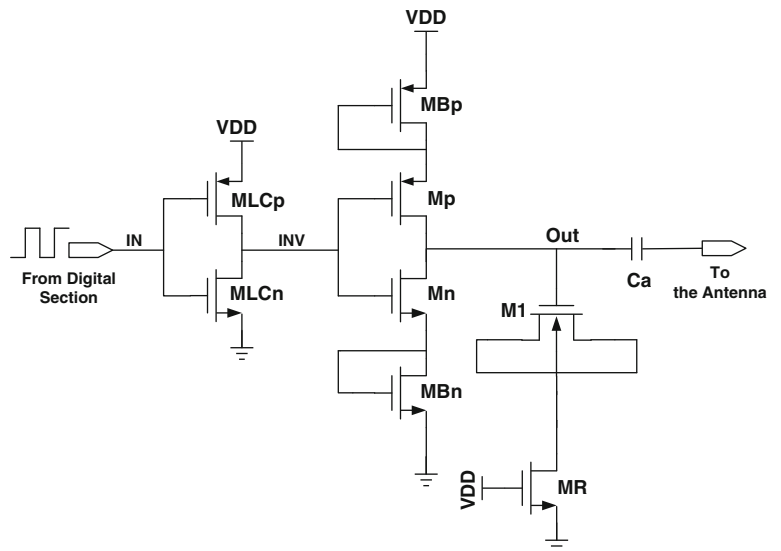


Figure 11 shows the simulation results of the proposed modulator in 40 kb/s data rate. Top waveform shows the input data stream {000...} sent by the control logic, presented just as a reference. Its amplitude is 400 mV. Second waveform shows the output signal of the level converter which doubles the control logic output voltage swing. The output voltage signal of the main inverter, driving voltage of MOSCAP, is shown as the third waveform. Although, it is not completely equal to voltage levels obtained in Sect. 4, the capacitance of MOSCAP at forth waveform, are approximately the same as Sect. 4. This correct functionality is because of suitable choice of driver voltage levels enough far away from the nonlinear operation region of MOSCAP. The amount of capacitance in low and high voltage levels is 0.52 and 1.92 pF, respectively which is approximately equal to the capacitances which obtained in Sect. 4. The difference between the calculated and the simulated capacitances is due to the output capacitance of the driver circuit which is neglected in calculations. This neglect is just because of the small amount of the diver capacitance in comparison to MOSCAP and C_a .

The capacitance seen by the antenna (C_{ant}) is the series capacitance of the constant capacitance, C_a , and the MOSCAP in parallel with the output capacitance of the inverter (C_{inv}) as (9). The simulated amount of this capacitance is 261 and 410 fF, respectively in low and high driving voltage levels, which is approximately equal to the desired capacitance which calculated in Sect. 2.2.

$$C_{ant} = \frac{C_a(C_{inv} + C_{MOS})}{C_a + C_{inv} + C_{MOS}} \quad (9)$$

5.1 Data rate test

EPC specification emphasizes that the tag shall support all data rates in the range of 40–640 kb/s in downlink (tag to

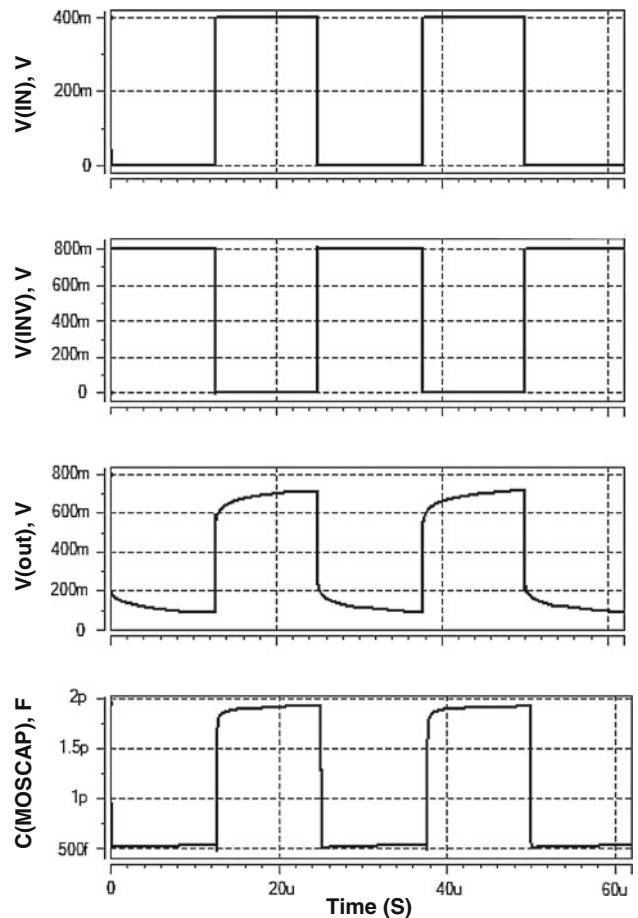


Fig. 11 Simulation results of the proposed PSK modulator

reader). By increasing data rate, the charging and discharging rate of MOSCAP should be increased. For highest data rate, the MOSCAP shall be charged in less than 780 nS to be able to accommodate EPC global specification. This

issue has considered in the determination of bias transistor sizes (MB_p and MB_n) in the design process. So, the proposed modulator, as an operational backward block, accommodates the required data rates. The capacitance seen by the antenna at data rate 640 kb/s is shown in Fig. 12. It is obvious that the capacitance is the same as the capacitance in 40 kb/s data rate mentioned earlier, which proves the correct operation of the proposed modulator in desired frequency range.

5.2 Encoding

In addition to the data rate, the standard has determined how the data to be encoded and sent. The tag compatible with EPC standard protocol shall encode the backscattered data as either FM0 baseband or Miller modulated subcarrier at the data rate [13]. FM0 inverts the baseband phase at every symbol boundary; a data-0 has an additional mid-symbol phase inversion. Miller inverts its phase between two data-0s in sequence. Miller also places a phase inversion in the middle of a data-1 symbol [13]. The basic functions of both encoding methods are shown in Fig. 13.

The modulator should be able to send backscattered data encoded by both data encoding method. The simulations have done for a data stream {000...} encoded by FM0 baseband, up to now. However, the proposed modulator is able to send data encoded by Miller as well as FM0. Figure 14 shows the capacitance seen by the antenna for a data stream {0010} encoded by Miller with two subcarriers. Although, miller encoding means higher charging speed of MOSCAP, the proposed modulator can tolerate this higher speed and works under this condition as well as more relax FM0 baseband condition.

5.3 Power supply variations

As the DC voltage of power supply is provided by RF-to-DC block, any change in output can affect other tag building blocks operation. To be sure about well operation of the proposed modulator under this condition, as it

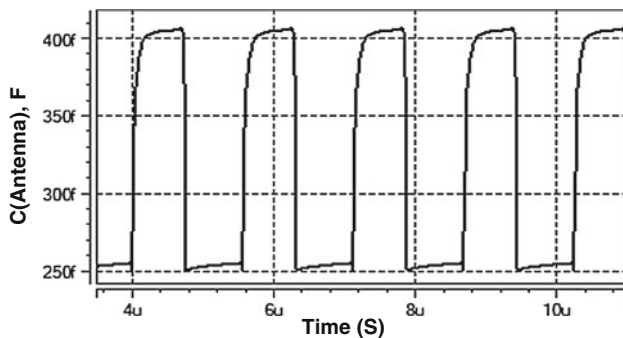


Fig. 12 The capacitance seen by the antenna at 640 kb/s data rate

depends on power supply voltage, the designed circuit is tested under $\pm 10\%$ supply voltage variation.

Voltages more than nominal value (0.8 V) has indeed just a small effect on MOS-capacitance and subsequently on the impedance seen by the antenna, as the MOSCAP works enough far away from non-linear region (based on Fig. 8). The higher voltage just leads to more power consumption and does not destroy the modulator operation.

However, smaller voltage supply affects more, since these voltages lead to smaller drive voltage and if this voltage be small enough, makes MOSCAP work in non-linear region which leads to more variation in capacitance and subsequently impedance. This effect can be more perceptible in low-voltage modulators. However, the proposed modulator can work successfully under these variations as its voltage supply is 0.8 V which is still far away from nonlinear region of MOSCAP. Figure 15 shows the capacitance seen by the antenna for three different power supply voltages, 0.72, 0.8 and 0.88 V.

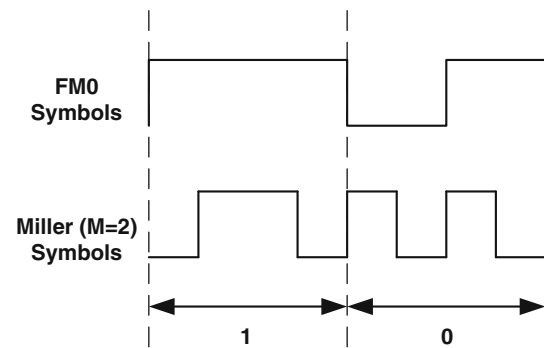


Fig. 13 FM0 and Miller encoded symbols {10} [13]

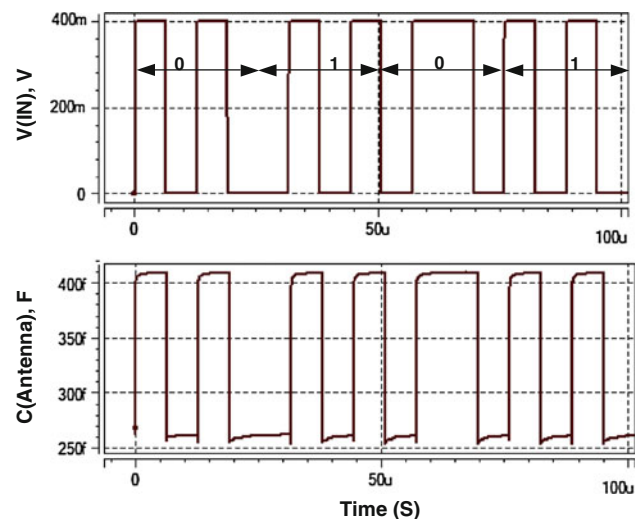
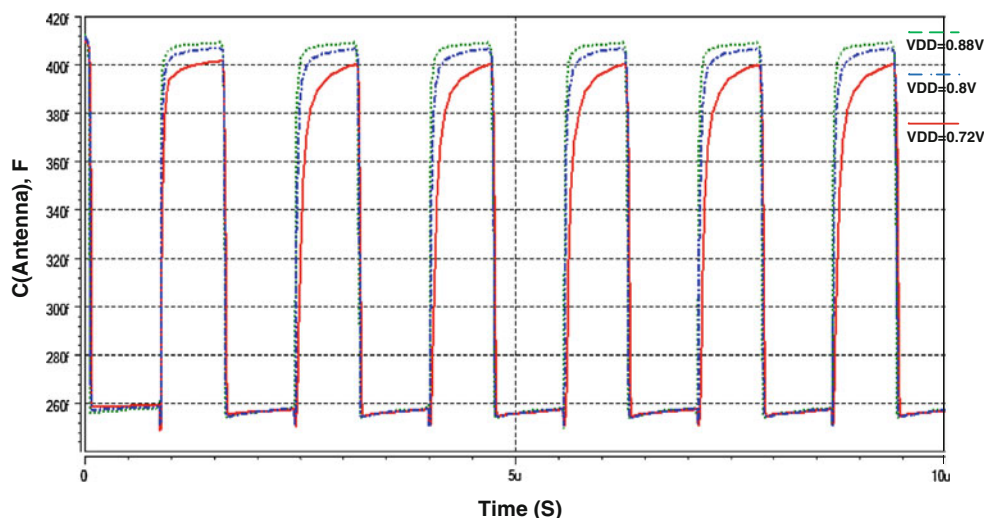


Fig. 14 Miller encoded data stream {0010} and the capacitance seen by the antenna

Fig. 15 The capacitance seen by the antenna at 640 kb/s data rate in three different power supply voltages, 0.72, 0.8 and 0.88 V



5.4 Monte Carlo simulation

A prevalent method of dealing with the large number of correlated and uncorrelated variables involved in circuit design is Monte Carlo simulation. Process parameters can be characterized as a distribution of transistor behaviors. Monte Carlo simulation allows all of these variables to be considered during simulation. These parameters are transistors width and threshold voltage.

To be sure about the well operation of the designed modulator in different process conditions, Monte Carlo simulation is done and the histogram of the MOSCAP capacitance variation is plotted in Fig. 16. Transistors widths and threshold voltages are the parameters which characterize the distribution of the circuit behavior. MOSCAP capacitance should be varied about 1.4 pF as it is derived in Sect. 4. However, there is a small difference between simulation and theoretical result which is due to the output capacitance of the main inverter that is neglected in comparison to the MOS capacitance in theoretical analysis.

5.5 Corner cases test

EPC global protocol defines the operational environment temperature which tag should work correctly over it. Nominal temperature range is (−25 to 40 °C) that in some cases extends to (−40 to 65 °C) [13]. The simulations have done over this temperature range for three critical process corner cases (FF, TT, and SS). Figure 17 shows the capacitance seen by the antenna for three temperature–process corner cases (FF at −40 °C, TT at 27 °C, and SS at 65 °C) at 40 kb/s data rate. Simulations confirm the proper operation of the modulator over these process and temperature variations. Variation of capacitance over different

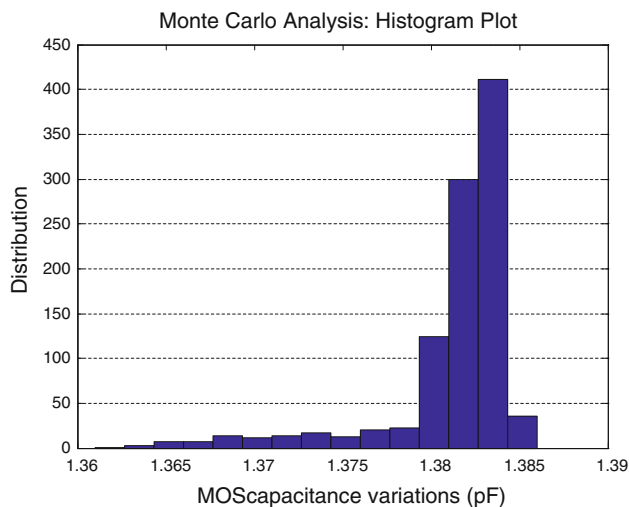


Fig. 16 Monte Carlo simulation result of MOSCAP capacitance variations

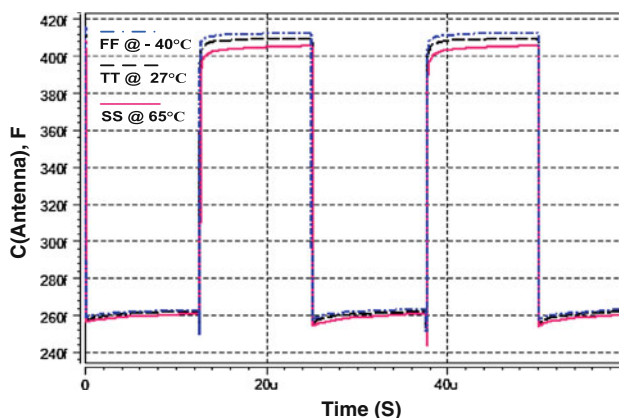


Fig. 17 The capacitance seen by the antenna at 40 kb/s data rate in three critical corner cases

Table 1 Power consumption of proposed modulator in critical process–temperature corner cases

	FF at $-40\text{ }^{\circ}\text{C}$	SS at $65\text{ }^{\circ}\text{C}$	TT at $27\text{ }^{\circ}\text{C}$
Power consumption at 40 kb/s (nW)	39.2	36.5	45.5
Power consumption at 640 kb/s (nW)	296	263	329

corner cases is less dependent of circuit design and is more due to the variation of MOSCAP capacitance over these cases.

Table 1 shows power consumption of the proposed PSK modulator for three critical cases. Operational data rate is in lowest and highest data rate defined by the standard, 40 and 640 kb/s, respectively. In comparison to traditional varactor-base modulators that consume power in micro watt order, the proposed modulator consumes just 45.5 nW power at 40 kb/s data rate and 329 nW power at 640 kb/s, both in worst cases. Therefore, it could be known as an ultra low power backscatter PSK modulator. This modulator leads to the longer reading range, as it has designed in such a way that most of available power at the antenna goes to the RF-to-DC rectifier instead of wasting in modulator.

6 Conclusion

This paper presents an ultra low power PSK backscatter modulator which allows tag to communicate with reader in long distances. As shown in the paper, the system complexity is principally less than previous work, as it just uses a simple inverter and two diode connected transistors as a driver circuit to vary the capacitance of a MOSCAP instead of a varactor. It also leads to low voltage and ultra low power operation which is desired in the passive UHF RFID tags. A new simple method for modulator analysis and design is also presented which leads to the required variable capacitances without any information about the RF-to-DC block circuit configuration.

This modulator is simulated in a $0.18\text{ }\mu\text{m}$ CMOS technology. Simulation results show the proper modulator functionality in compatible with C1 G2 EPC global standard for different encodings and data rates. This PSK backscatter modulator works under $\pm 10\%$ supply voltage variation and also in different process and temperature corner cases. The whole power consumption in all corner cases is less than 46 nW at 40 kb/s data rate.

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